I²C-bus compatible ICs
Types PCF8582A to UMA 1010T

BOOK IC12b 1989

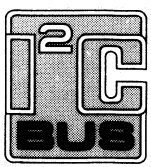
Philips Components

PHILIPS

I²C-BUS COMPATIBLE ICs

Part a

Part b



SELECTION GUIDE

Functional index
Numerical index

FUNCTIONAL INDEX

* Also available with extended and automotive temperature ranges.

NUMERICAL INDEX

DEVICE DATA

256 × 8-bit STATIC CMOS EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8582A is a 2 Kbits 5 Volt electrically erasable programmable read only memory (EEPROM) organized as 256 by 8-bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I²C-bus, an eight pin DIL package is sufficient. Up to eight PCF8582A devices may be connected to the I²C-bus.

Chip select is accomplished by three address inputs.

Timing of the Erase/Write cycle can be done in two different ways; either by connecting an external clock to the "Programming Timing Control", pin (7 or 13), or by using an internal oscillator. If the latter is used an RC time constant must be connected to pin 7 or 13.

FEATURES

- Non-volatile storage of 2 Kbits organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- power on reset
- 10,000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571, PCF8582 and PCD8572
- External clock signal possible.

PACKAGE OUTLINE

PCF8582AP; 8-lead dual in line; plastic (SOT97).
PCF8582AT; 16-lead mini-pack; plastic (SO16L; SOT162A).

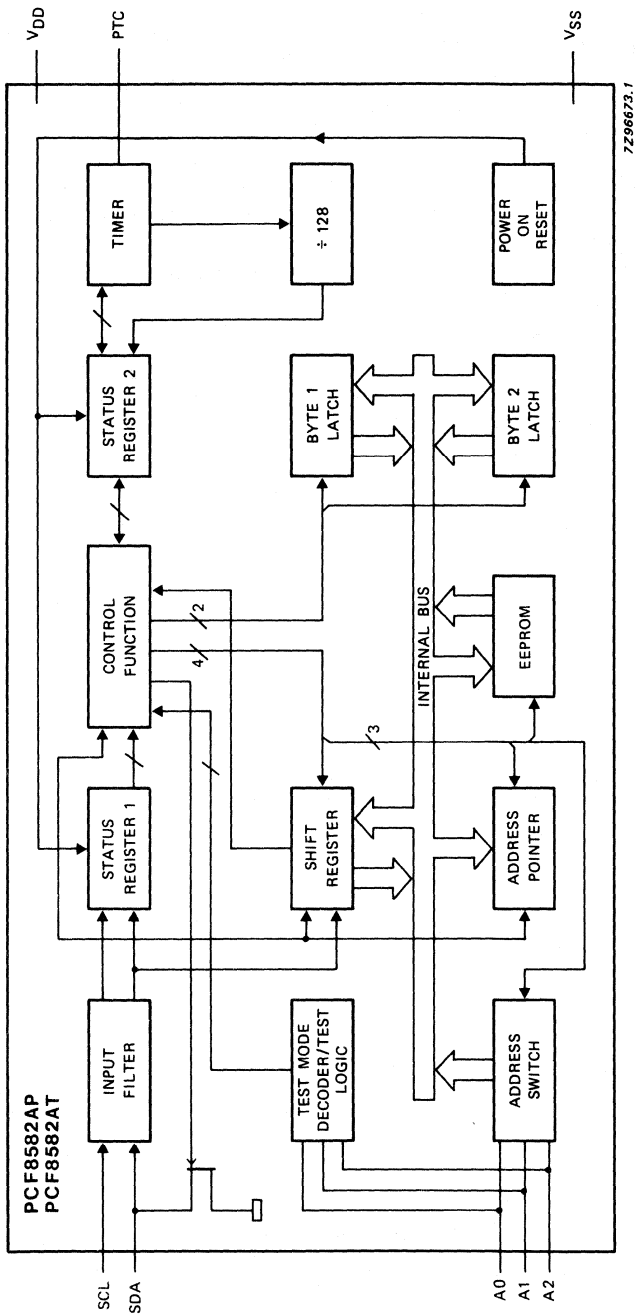
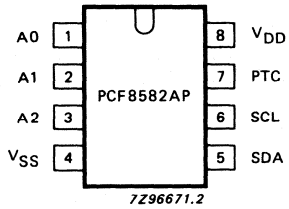
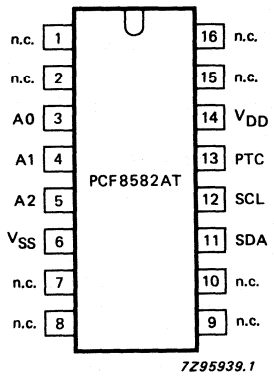


Fig. 1 Block diagram.



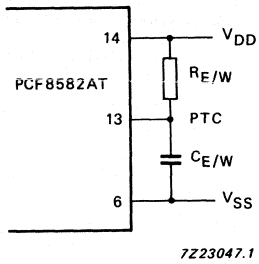
1	A0	address inputs/test mode select
2	A1	
3	A2	
4	V_{SS}	ground
5	SDA	I^2C-bus lines
6	SCL	
7	PTC	programming time control
8	V_{DD}	positive supply

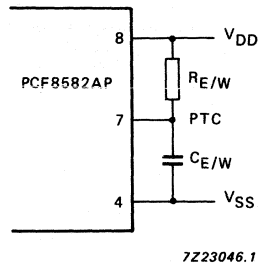
Fig. 2 (a) Pinning diagram.



1	n.c.	
2	n.c.	
3	A0	address inputs/test mode select
4	A1	
5	A2	
6	V_{SS}	ground
7	n.c.	
8	n.c.	
9	n.c.	
10	n.c.	
11	SDA	I^2C-bus lines
12	SCL	
13	PTC	programming time control
14	V_{DD}	positive supply
15	n.c.	
16	n.c.	

Fig. 2 (b) Pinning diagram.





Figs. 3 (a) and (b) RC circuit connections to PCF8582AP and PCF8582AT when using the internal oscillator

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy; both data and clock lines remain HIGH.
Start data transfer; a change in the state of the data line, from HIGH to LOW,
while the clock is HIGH defines the start condition. Stop data transfer; a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid; the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

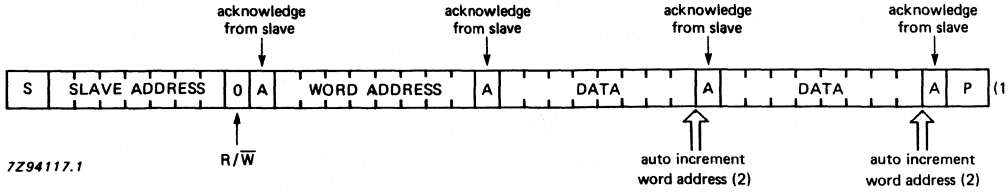
Within the I²C-bus specifications a low speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF8582A operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.
The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse in clock pulse.
Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this condition the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

I²C-Bus Protocol

The I²C-bus configurations for different READ and WRITE cycles of the PCF8582A are shown in Fig. 4, (a), (b) and (c).



(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission. The duration of the erase/write cycle is approximately 30 ms if only one byte is written and 60 ms if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

(2) The second data byte is voluntary. It is not allowed to erase/write more than two types.

Fig. 4(a) Master transmitter transmits to PCF8582A slave receiver (ERASE/WRITE mode).

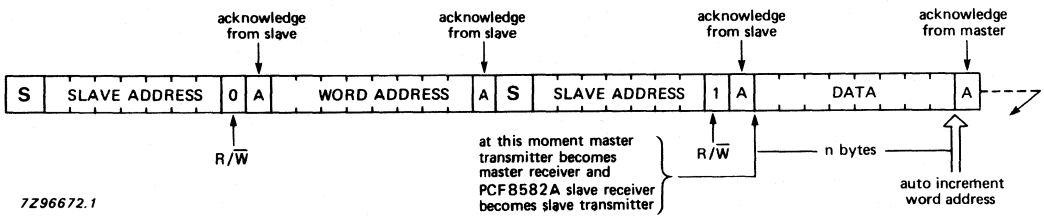
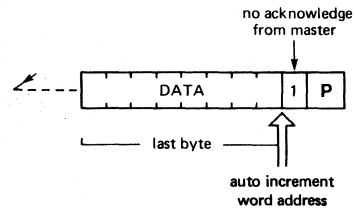


Fig. 4(b) Master reads PCF8582A slave after setting word address (write word address; READ data).



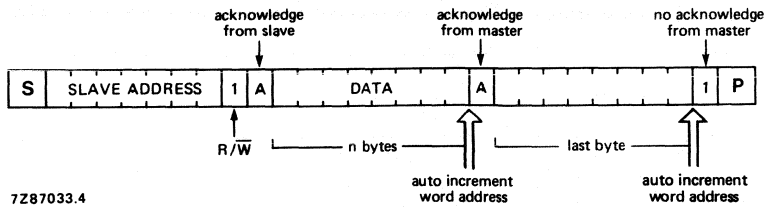


Fig. 4(c) Master reads PCF8582A slave immediately after first byte (READ mode).*

Note: the slave address is defined in accordance with the I²C-bus specification as:

1	0	1	0	A2	A1	A0	R/W

* The device can be used as read only without the programming clock.

DEVELOPMENT DATA

I²C-bus timing

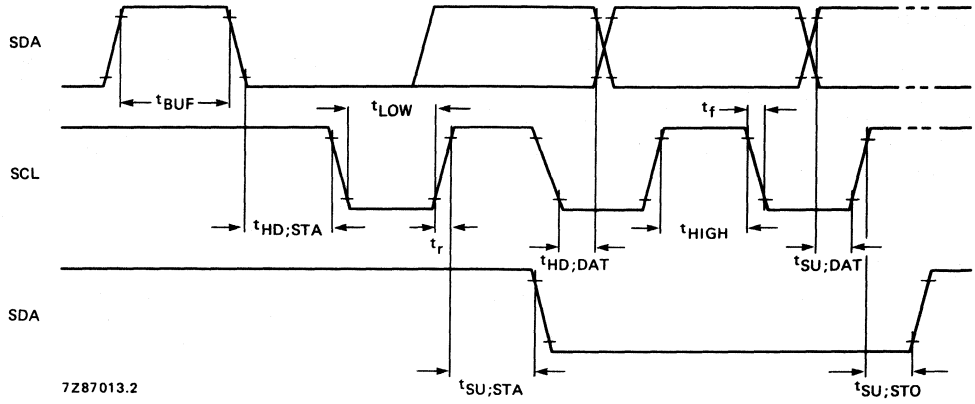
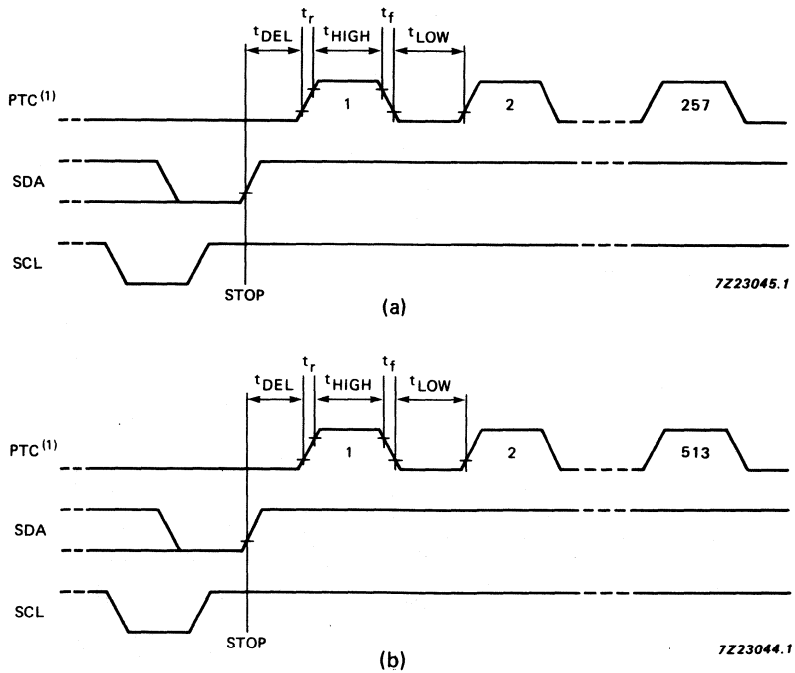


Fig. 5 I²C-bus timing.



(1) If external clock for PTC is chosen, this information is latched internally by leaving pin 7 LOW after transmission of the eight bit of the word address (negative edge of SCL). The state of PTC then, may be previously undefined.

Fig. 6 (a) One-byte ERASE/WRITE cycle; (b) two-byte ERASE/WRITE cycle.

Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.3	+7	V
Voltage on any input pin input impedance 500 Ω	V_I	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
Operating temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C
Current into any input pin	$\|I_I\|$	–	1	mA
Output current	$\|I_O\|$	–	10	mA

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_{DD}	4.5	5.0	5.5	V
Operating supply current READ	V_{DD} max. f_{SCL} = 100 kHz	I_{DD}	–	–	0.4	mA
Operating supply current WRITE/ERASE	V_{DD} max.	I_{DDW}	–	–	2.0	mA
Standby supply current	V_{DD} max.	I_{DDO}	–	–	10	μA
Input PTC						
Input voltage HIGH			V_{DD} − 0.3	–	–	V
Input voltage LOW			–	–	V_{SS} + 0.3	V
Input SCL and input/output SDA						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD} + 0.8	V
Output voltage LOW	I_{OL} = 3 mA V_{DD} = 4.5 V	V_{OL}	–	–	0.4	V
Output leakage current HIGH	V_{OH} = V_{DD}	I_{LO}	–	–	1	μA
Input leakage current (SCL)	V_I = V_{DD} or V_{SS}	I_{LI}	–	–	1	μA
Clock frequency		f_{SCL}	0	–	100	kHz
Input capacitance (SCL; SDA)		C_I	–	–	7	pF
Time the bus must be free before new transmission can start		t_{BUF}	4.7	–	–	μs
Start condition hold time after which first clock pulse is generated		$T_{HD;STA}$	4	–	–	μs

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
The LOW period of the clock		t_{LOW}	4.7	–	–	μs
The HIGH period of the clock		t_{HIGH}	4.0	–	–	μs
Set-up time for start condition	repeated start only	$t_{SU;STA}$	4.7	–	–	μs
Data hold time for I²C bus compatible masters		$t_{HD;DAT}$	5.0	–	–	μs
Data hold time for I²C devices	note 1.	$t_{HD;DAT}$	0	–	–	ns
Date set up time		$t_{SU;DAT}$	250	–	–	ns
Rise time for SDA and SCL lines		t_r	–	–	1	μs
Fall time for SDA and SCL lines		t_f	–	–	300	ns
Set-up time for stop condition		$T_{SU;STO}$	4.7	–	–	μs
Programming time control						
Erase/write cycle time		$t_{E/W}$	20	–	100	ms
Capacitor used for E/W cycle of 30 ms	max. tolerance ±10%; using internal oscillator (Fig. 3)	$C_{E/W}$	–	3.3	–	nF
Resistor used for E/W cycle of 30 ms	max. tolerance ±5%; using internal oscillator (Fig. 3)	$R_{E/W}$	–	56.0	–	kΩ
Programming frequency using external clock						
Frequency		f_p	2.57	–	12.85	kHz
Period LOW		t_{LOW}	10.0	–	–	μs
Period HIGH		t_{HIGH}	10.0	–	–	μs
Rise-time		t_r	–	–	300	ns
Fall-time		t_f	–	–	300	ns
Delay-time		t_d	0	–		ns
Data retention time	T_{amb} = 55 °C	t_S	10	–	–	years

Note to the characteristics

1. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

SUPERSEDES DATA OF JULY 1987

CLOCK CALENDAR WITH 256 X 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1.0 V to 6 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

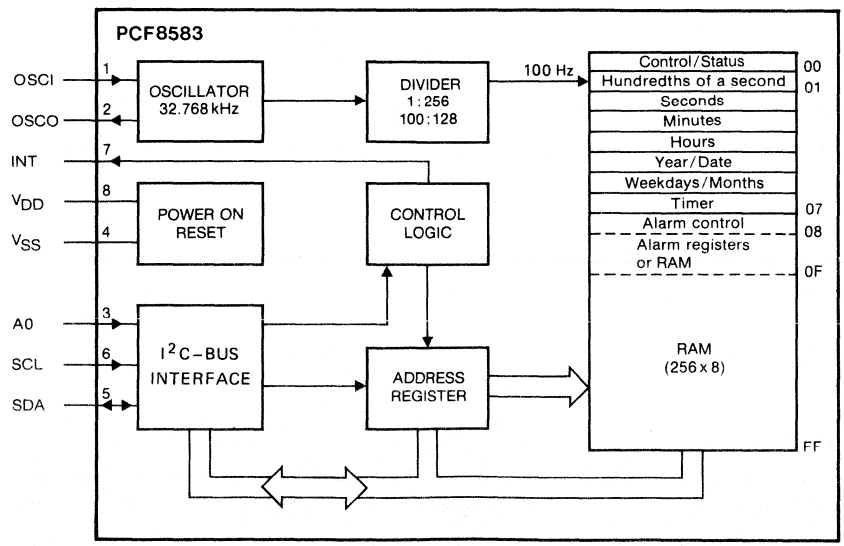


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT97).
PCF8583T: 8-lead mini-pack; plastic (SO8L; SOT176A).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input	
2	OSCO	oscillator output	
3	A0	address input	
4	V_{SS}	negative supply	
5	SDA	serial data line	I^2C-bus
6	SCL	serial clock line	I^2C-bus
7	INT	open drain interrupt output (active low)	
8	V_{DD}	positive supply	

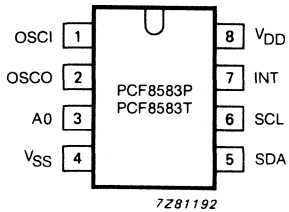


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 8)	V_{DD}	−0.8	+ 7.0	V
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	−	50	mA
Input voltage range	V_I	−0.8 to V_{DD}	+ 0.8	V
DC input current	I_I	−	10	mA
DC output current	I_O	−	10	mA
Power dissipation per package	P_{tot}	−	300	mW
Power dissipation per output	P_O	−	50	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C-bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I²C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

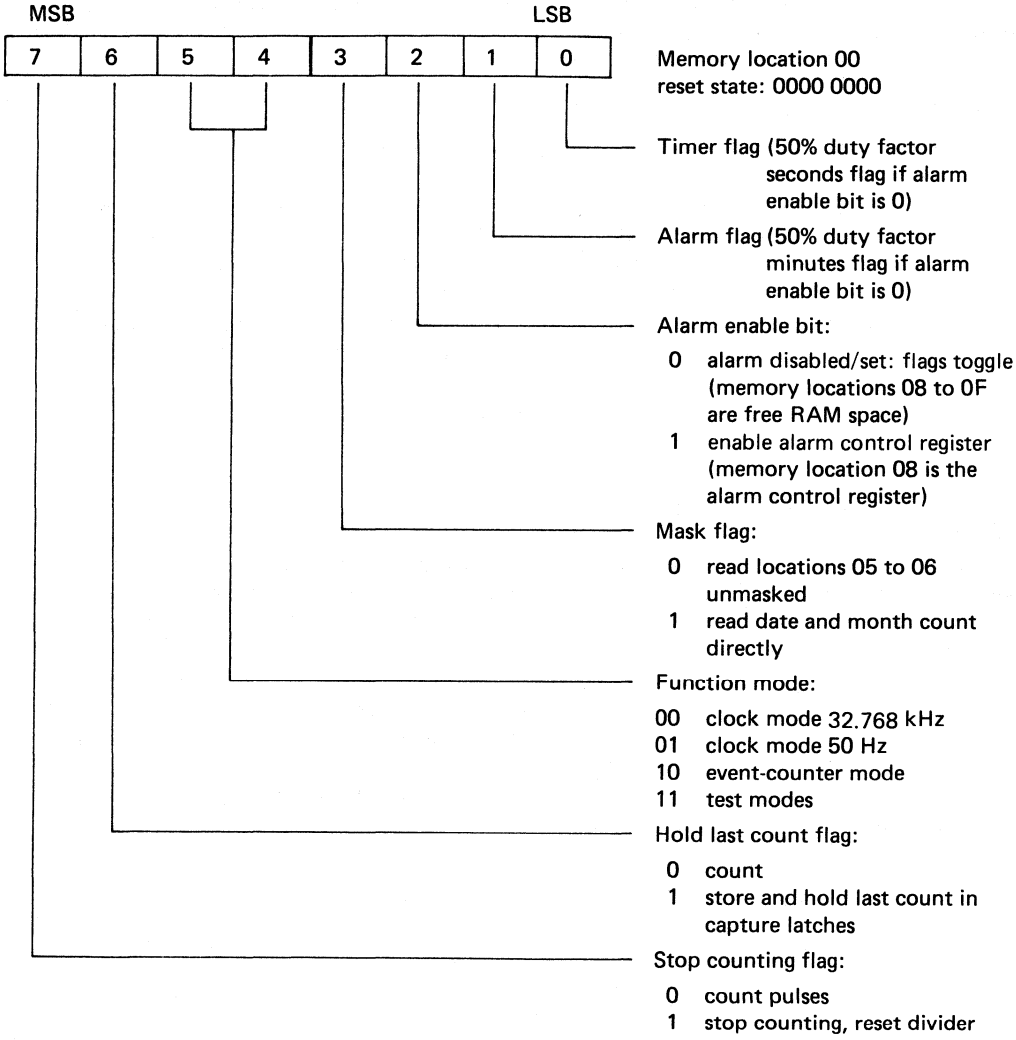


Fig.3 Control/status register.

Counter registers

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig.6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

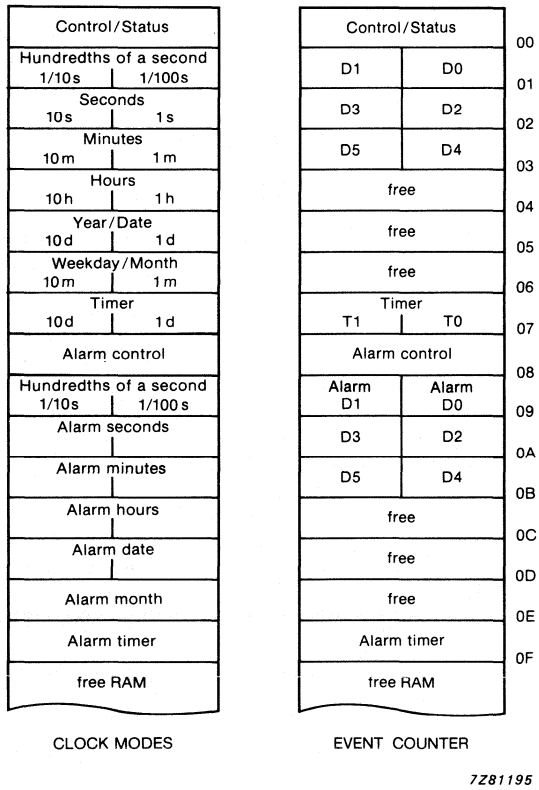
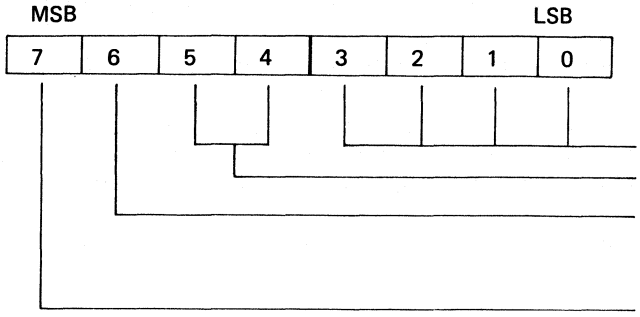


Fig.4 Register arrangement.

Counter registers (continued)



Memory location 04 (hours counter)
reset state: 0000 0000

Unit hours BCD

Ten hours (0 to 2 binary)

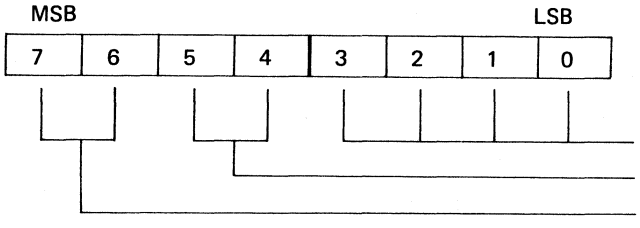
AM/PM flag:

0 AM
1 PM

Format:

0 24 h format, AM/PM flag remains unchanged
1 12 h format, AM/PM flag will be updated

Fig.5 Format of the hours counter.



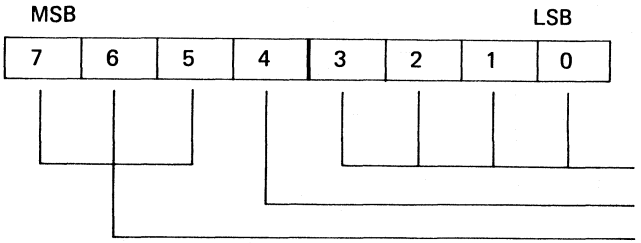
Memory location 05 (year/date)
reset state: 0000 0001

Unit days BCD

Ten days (0 to 3 binary)

Year (0 to 3 binary, read as 0 if the mask flag is set)

Fig.6 Format of the year/date counter.



Memory location 06 (weekdays/months)
reset state: 0000 0001

Unit months BCD

Ten months

Weekdays (0 to 6 binary, read as 0 if the mask flag is set)

Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10, 12
	01 to 30	30 to 01	4, 6, 9, 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer	00 to 99	no carry	

DEVELOPMENT DATA

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

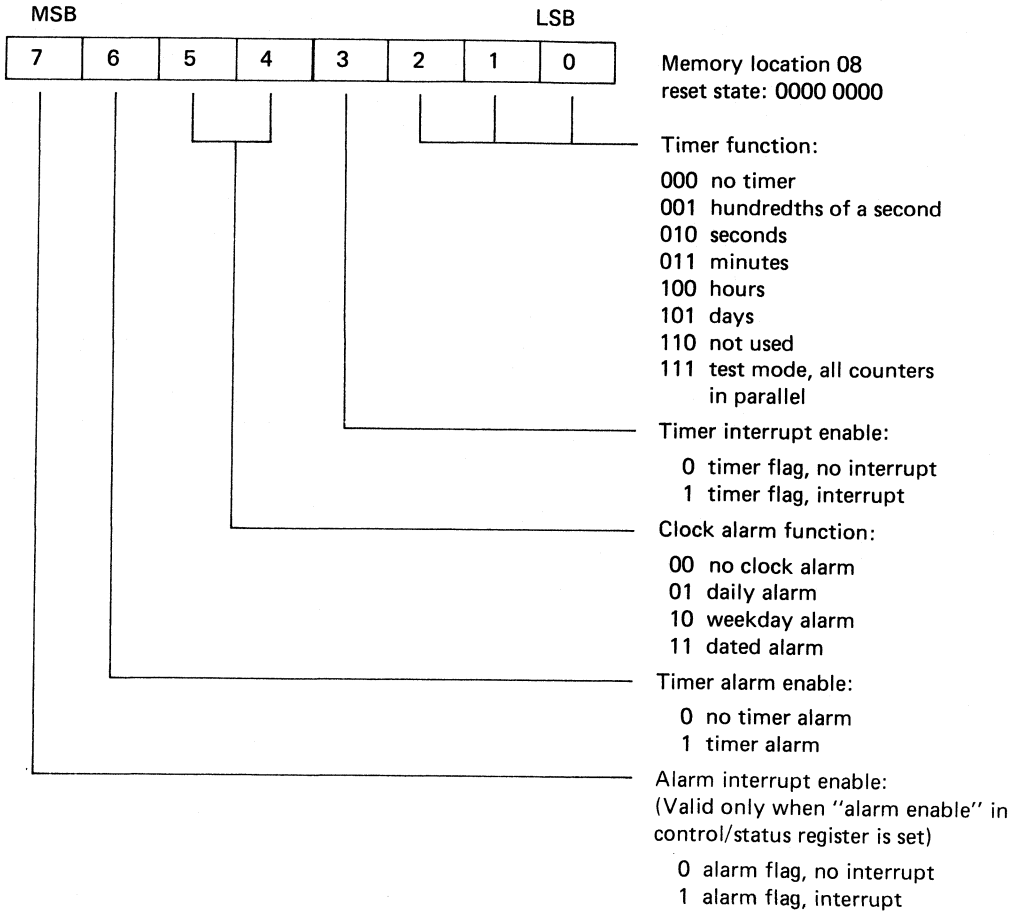
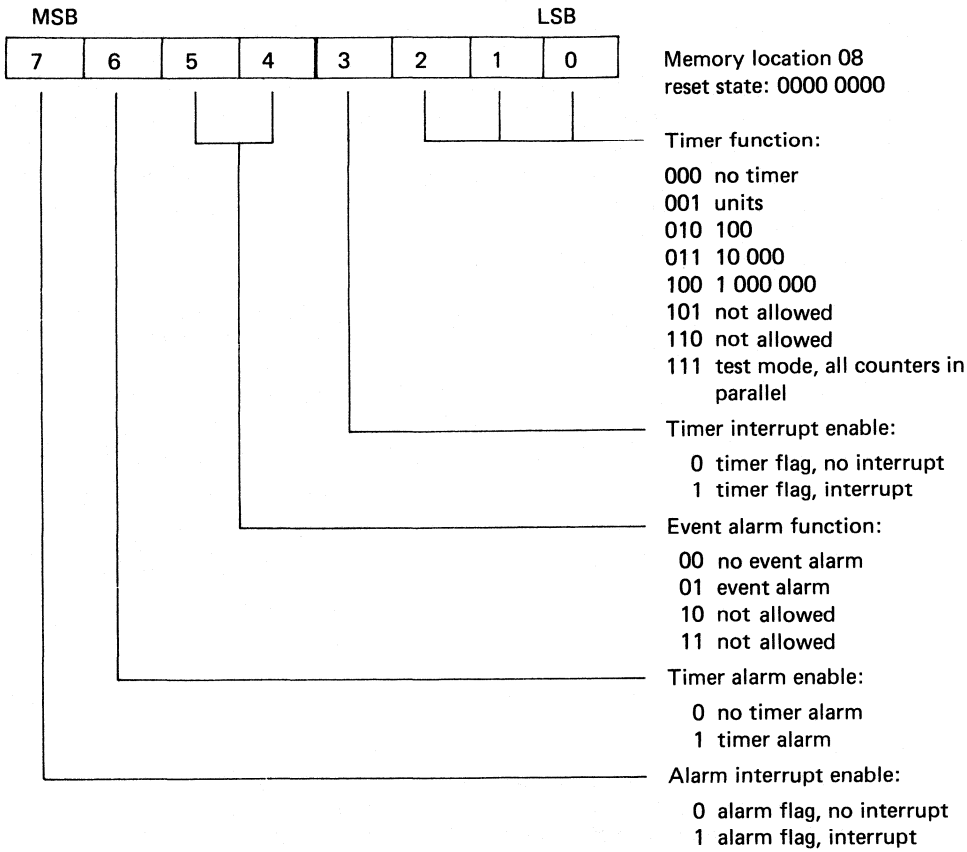


Fig.8a Alarm control register, clock modes.



DEVELOPMENT DATA

Fig.8b Alarm control register, event-counter mode.

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Note: In the 12 h mode bits 6 and 7 of the alarm hours register must be the same as the hours counter.

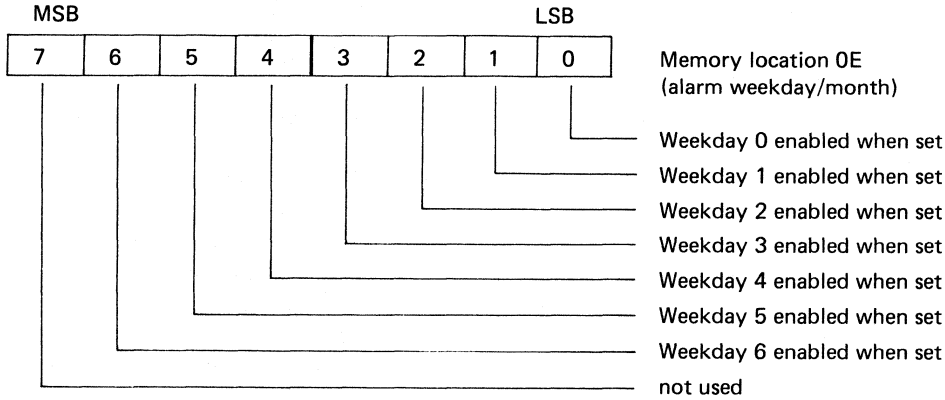


Fig.9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see quartz frequency adjustment). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I²C-bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32.768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00. 1 Hz is output at the interrupt (starts HIGH). This can be disabled by setting the alarm enable bit in the control/status register.

A second level-sensitive reset signal to the I²C-bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

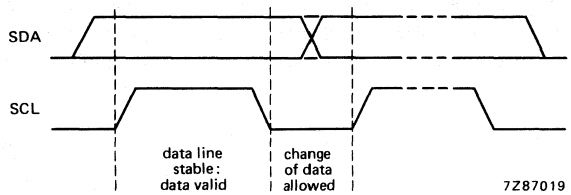


Fig.10 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

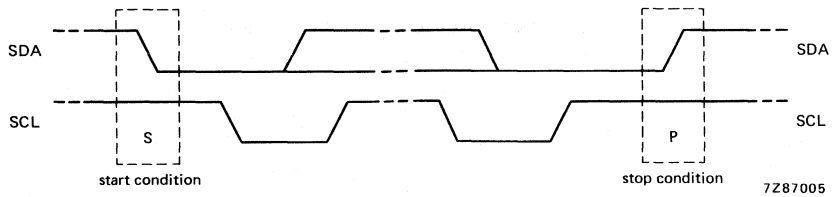


Fig.11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

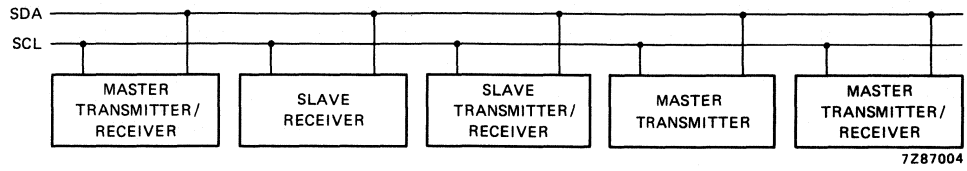


Fig.12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

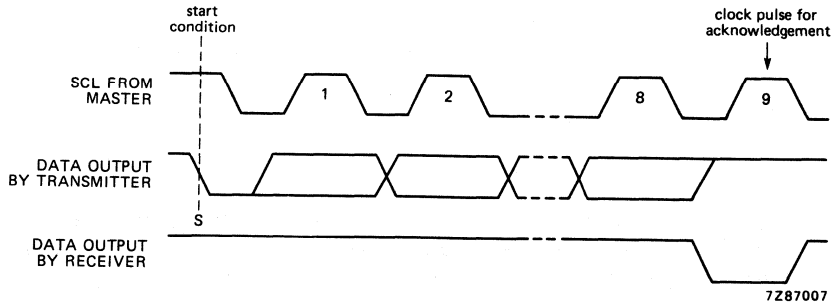


Fig.13 Acknowledgement on the I^2C-bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

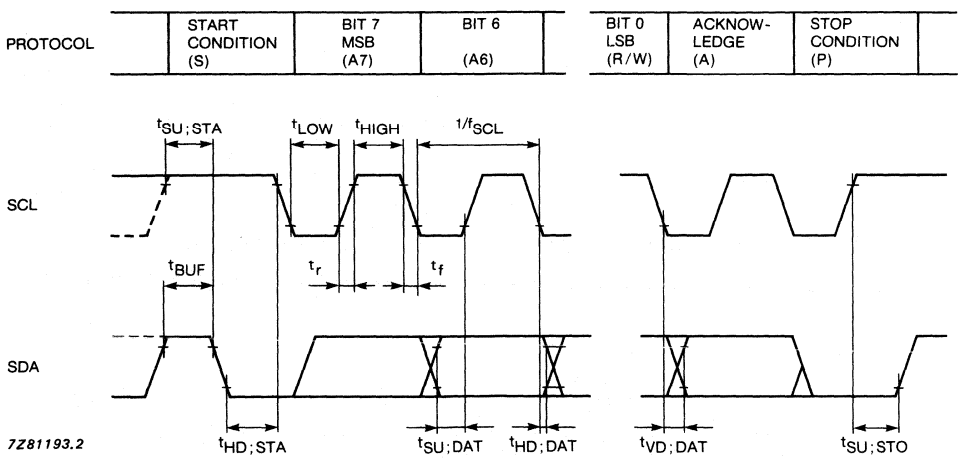


Fig. 14 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig.15.

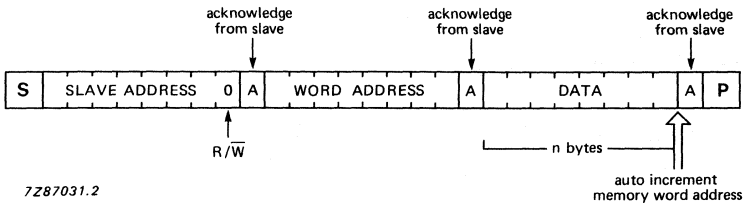


Fig.15a Master transmits to slave receiver (WRITE mode).

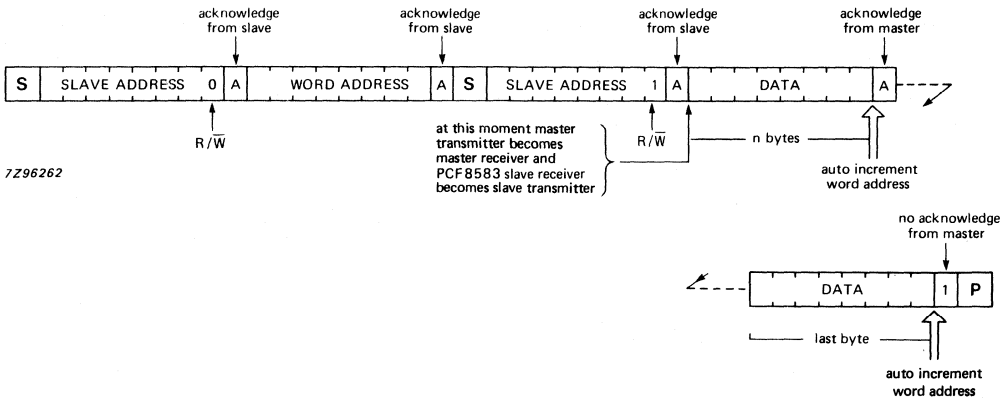


Fig.15b Master reads after setting word address (WRITE word address; READ data).

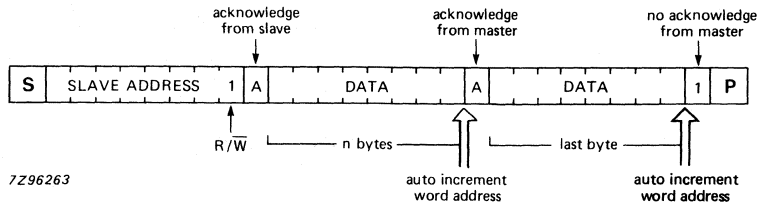


Fig.15c Master reads slave immediately after first byte (READ mode).

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
operating		V_{DD}	2.5	–	6.0	V
clock	T_{amb} = 0 to + 70 °C	V_{DD}	1.0	–	6.0	V
Supply current						
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
clock	V_{DD} = 5 V	I_{DDO}	–	10	50	μA
clock	V_{DD} = 1 V	I_{DDO}	–	2	10	μA
Power-on reset voltage level	note 1	V_{POR}	1.5	1.9	2.3	V
Inputs; Input/output SDA						
Input voltage LOW	note 2	V_{IL}	−0.8	–	$0.3V_{DD}$	V
Input voltage HIGH	note 2	V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.8	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
A0; OSCI						
Input leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_{LI}\|$	–	–	250	nA
SCL; SDA						
Input capacitance	$V_I = V_{SS}$	C_I	–	–	7	pF
Output INT						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
LOW V_{DD} data retention						
Supply voltage for data retention		V_{DDR}	1	–	6	V
Supply current	note 3					
	V_{DDR} = 1 V T_{amb} = −25 to + 70 °C;	I_{DDR}	–	–	5	μA
	V_{DDR} = 1 V	I_{DDR}	–	–	2	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OSC}	–	40	–	pF
Oscillator stability for ΔV_{DD} = 100 mV	T_{amb} = 25 °C; V_{DD} = 1.5 V	f/fOSC	–	2×10^{-7}	–	
Input frequency	note 4	f_i	–	–	1	MHz
Quartz crystal parameters						
Frequency = 32.768 kHz						
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

Notes to the characteristics

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0.5 mA.
3. Event or 50 Hz mode only (no Quartz).
4. Event mode only.

APPLICATION INFORMATION

Quartz frequency adjustment

Method 1: Fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal available after power-on at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average ± 5 x 10^{-6}). Average deviations of ± 5 minutes per year can be achieved.

Method 2: OSCI Trimmer

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

Power-on
Initialization (alarm function)

Routine:

Set clock to time T and set alarm to time T + dT.
At time T + dT (interrupt) repeat routine.

If time dT is approximately 10 ms a frequency of approximately 40 Hz is obtained.

APPLICATION INFORMATION (continued)

The PCF8583 slave address has a fixed combination 1010 as group 1.

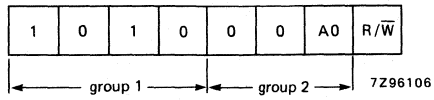
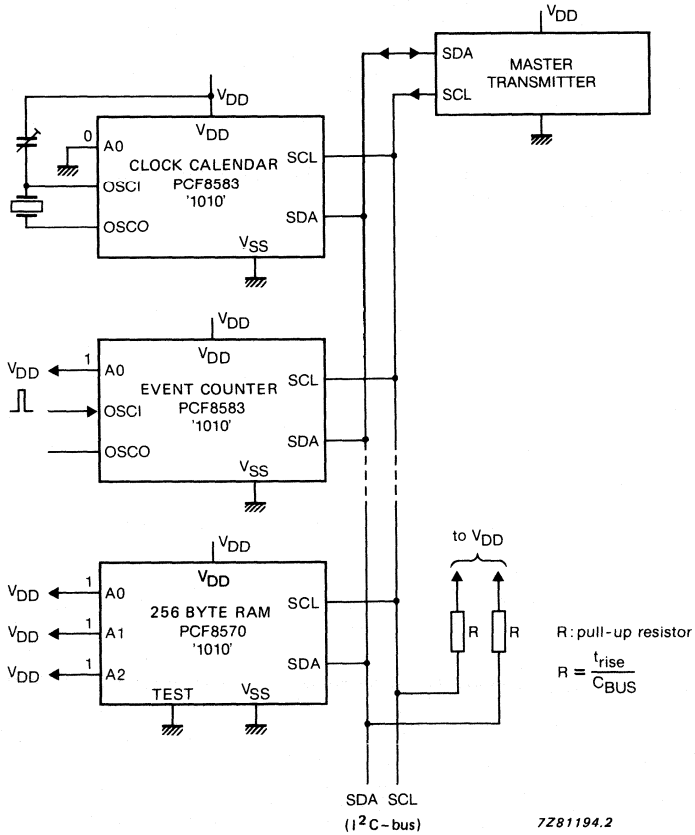


Fig.16 PCF8583 address.



Recommendation:
Connect a 4.7 μF 10 V solid aluminium (SAL) capacitor between V_{DD} and V_{SS}.

Fig.17 PCF8583 application diagram.

DEVELOPMENT DATA

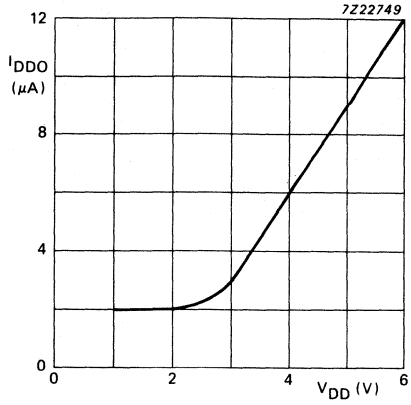


Fig.18 Typical supply current as a function of supply voltage (clock); $T_{amb} = -40$ to $+85$ °C.

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

FEATURES

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

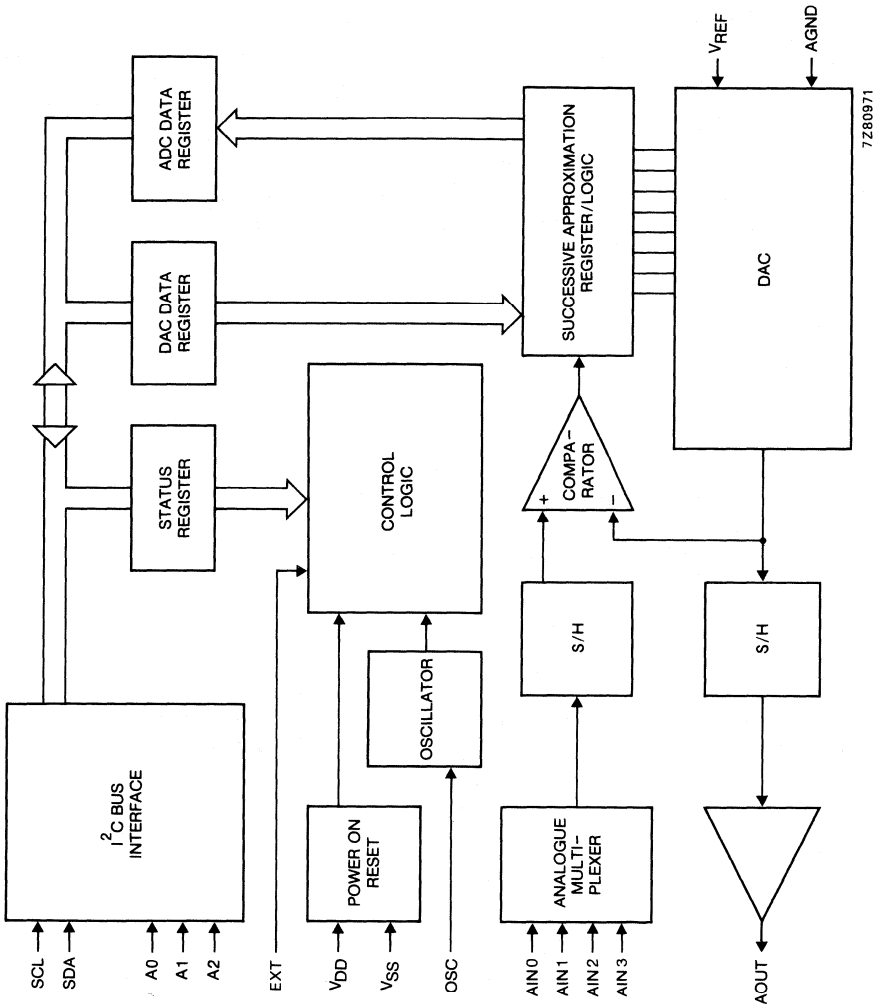


Fig. 1 Block diagram.

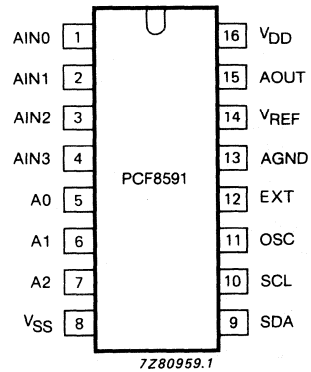


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

DEVELOPMENT DATA

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

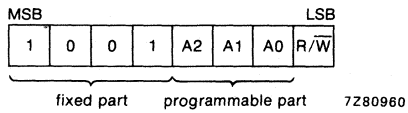


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

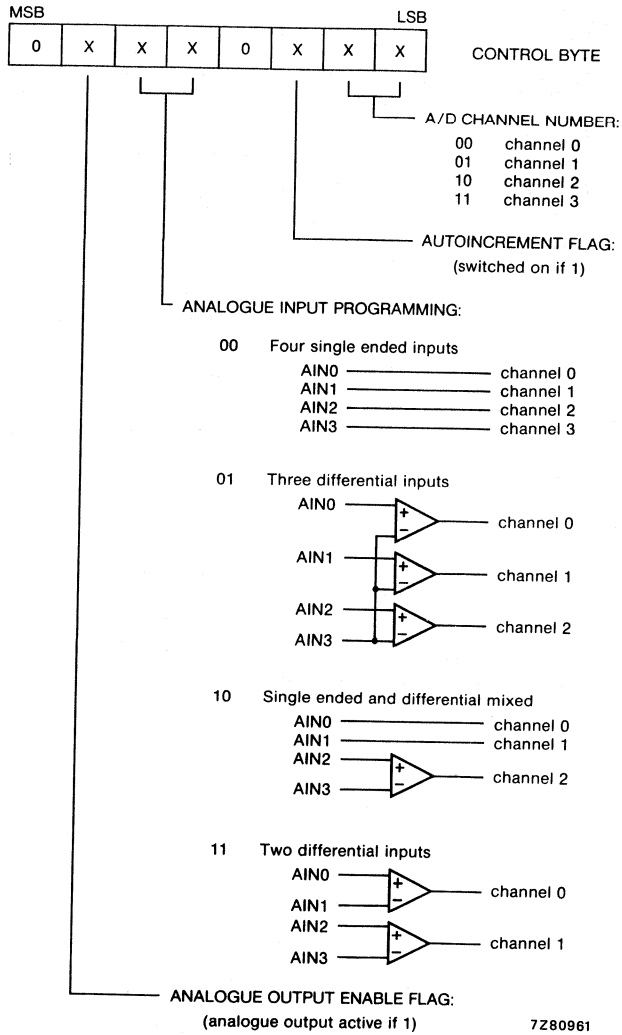


Fig. 4 Control byte.

DEVELOPMENT DATA

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

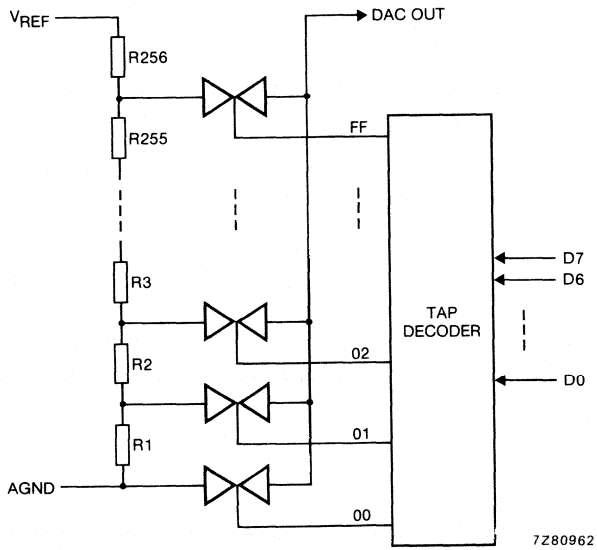


Fig. 5 DAC resistor divider chain.

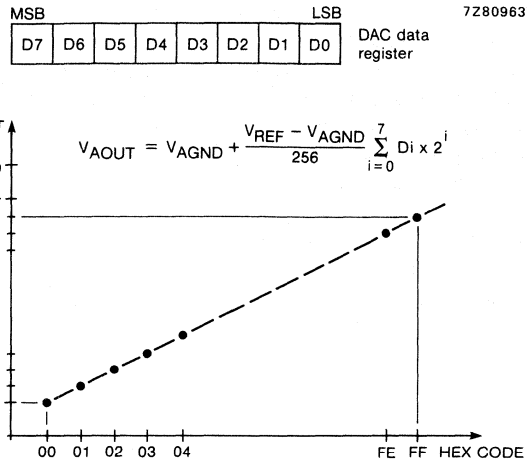


Fig. 6 DAC data and d.c. conversion characteristics.

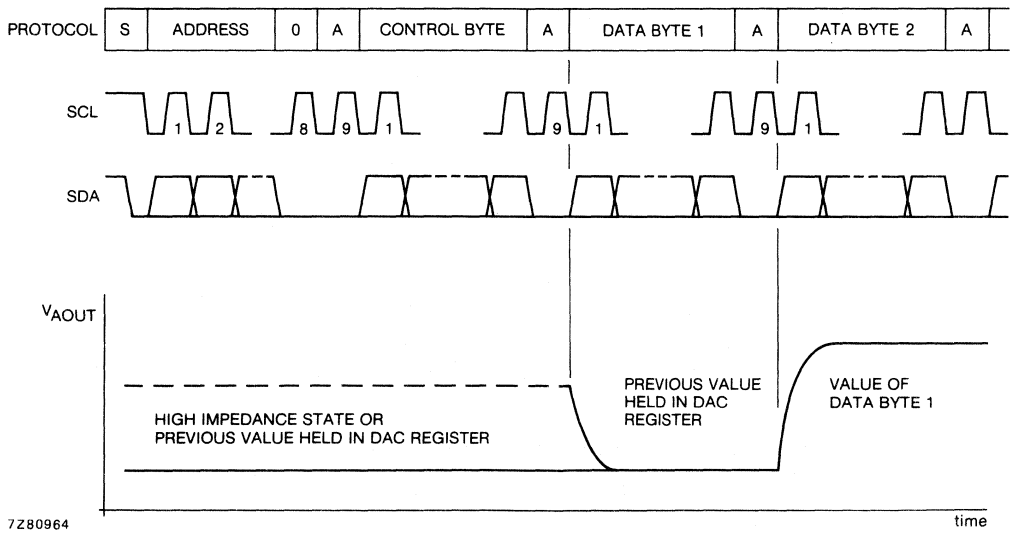


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

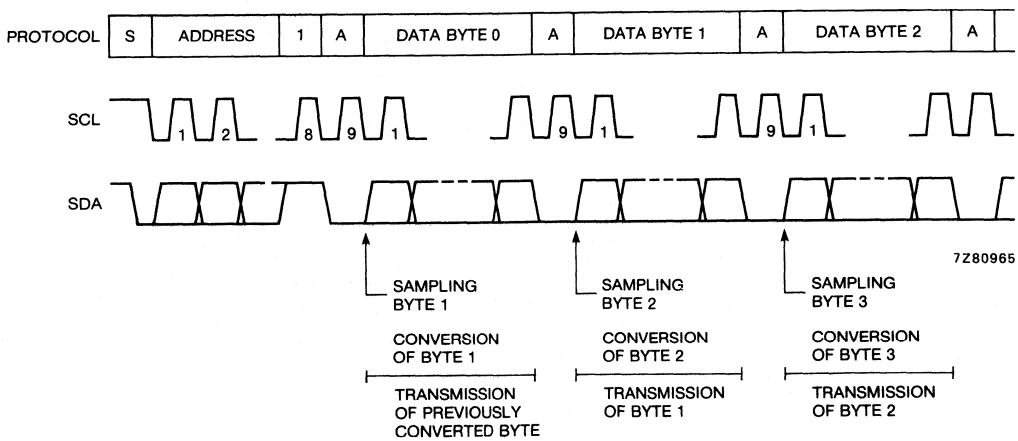


Fig. 8 A/D conversion sequence.

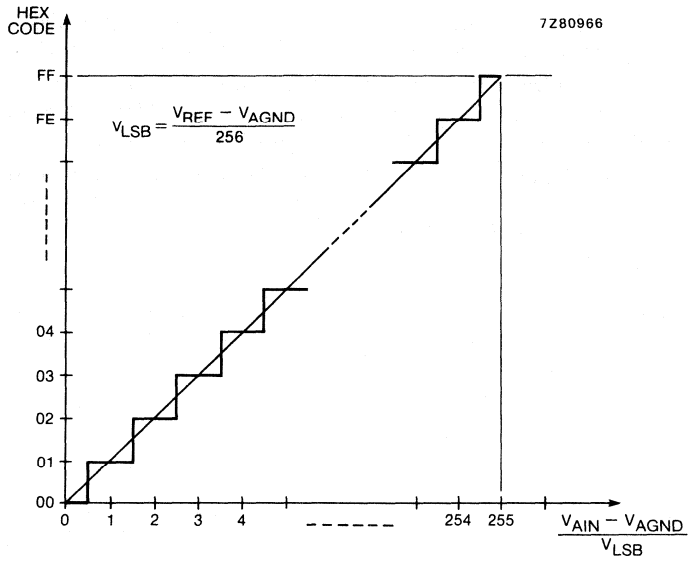


Fig. 9a A/D conversion characteristics of single-ended inputs.

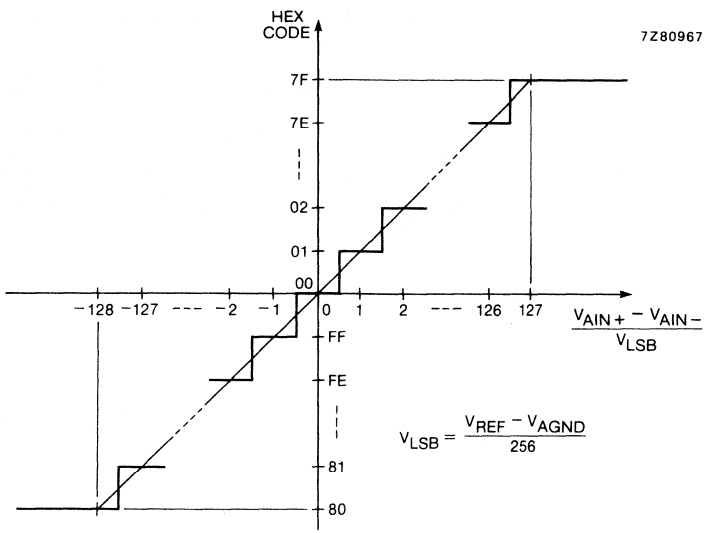


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

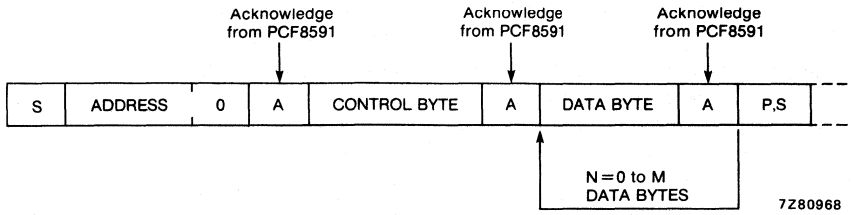


Fig. 10a Bus protocol for write mode, D/A conversion.

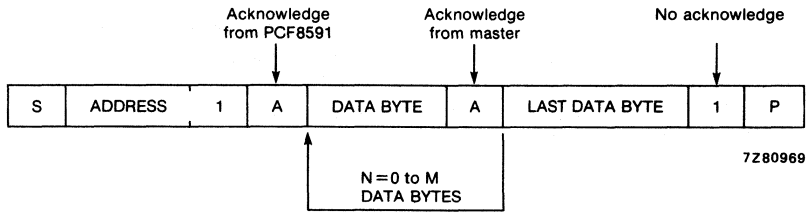


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

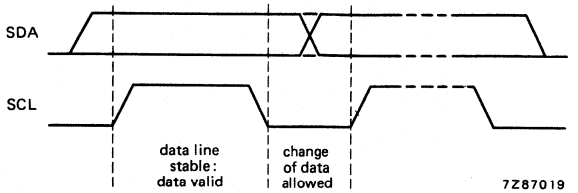


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

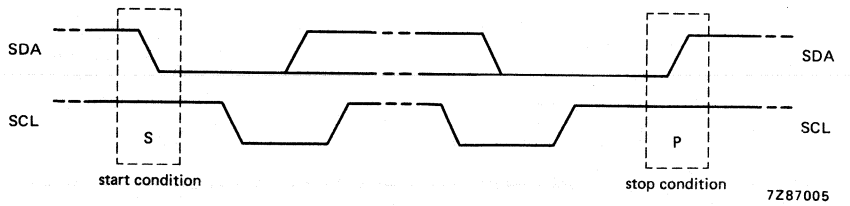


Fig. 12 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

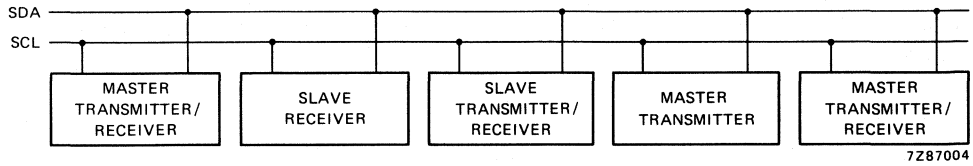


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

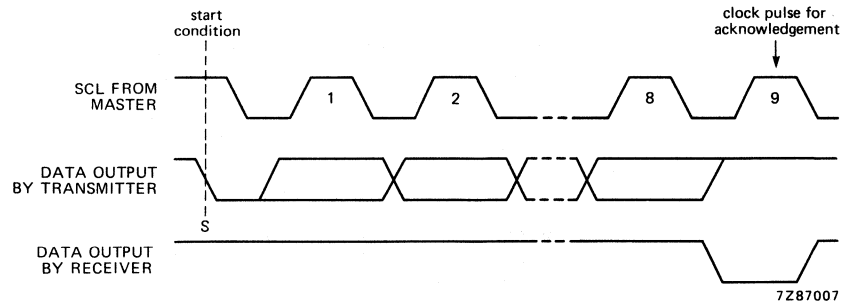


Fig. 14 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

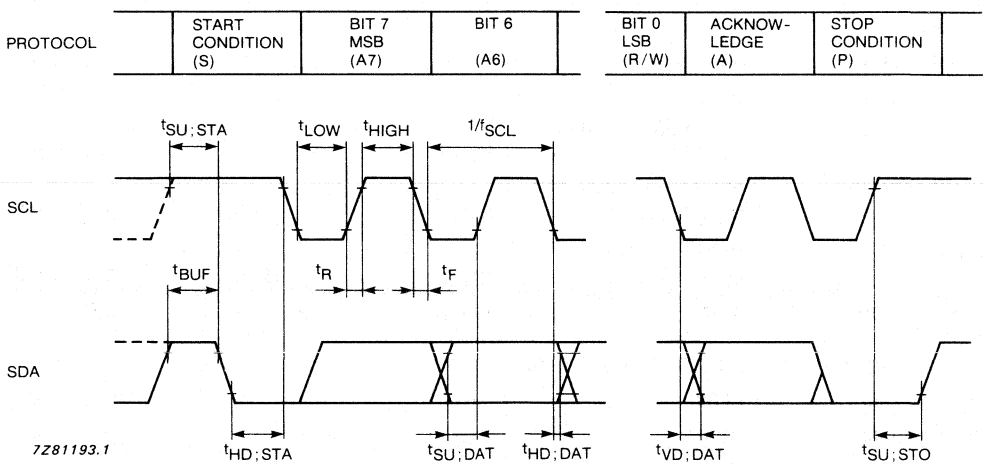


Fig. 15 I^2C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby V_I = V_{SS} or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; V_I = V_{SS} to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs	V_{REF}, AGND					
Voltage range	reference	V_{REF}	V_{AGND}	–	V_{DD}	V
Voltage range	analogue ground	V_{AGND}	V_{SS}	–	V_{REF}	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	0,9xV_{DD}	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

DEVELOPMENT DATA

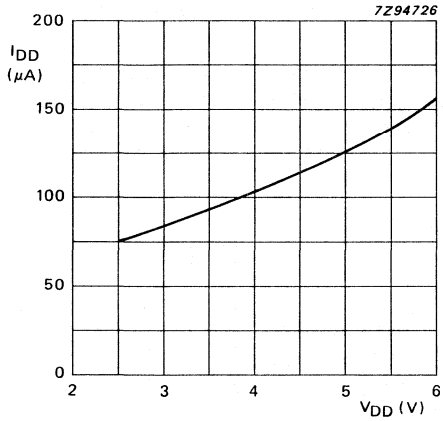
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

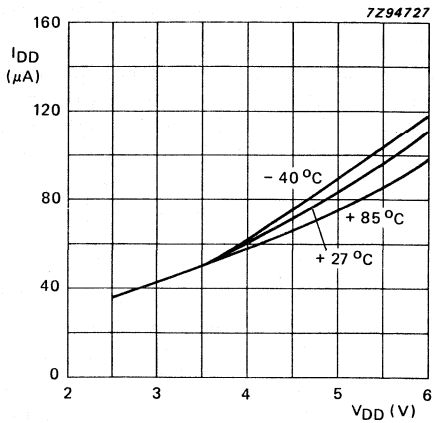
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; $V_{DDN} = 0{,}1 \times V_{PP}$	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.



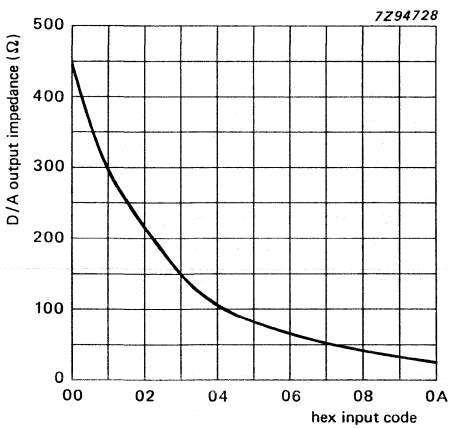
(a) internal oscillator; T_{amb} = + 27 °C.



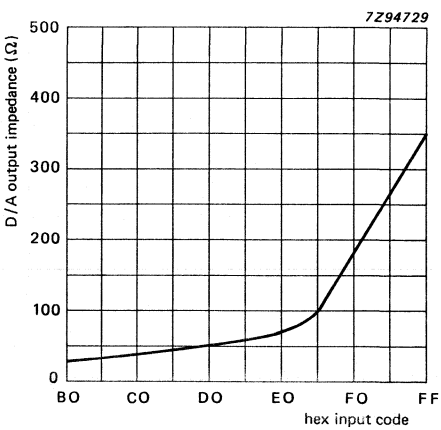
(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).

DEVELOPMENT DATA



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors ($> 10\ \mu F$) are recommended for power supply and reference voltage inputs.

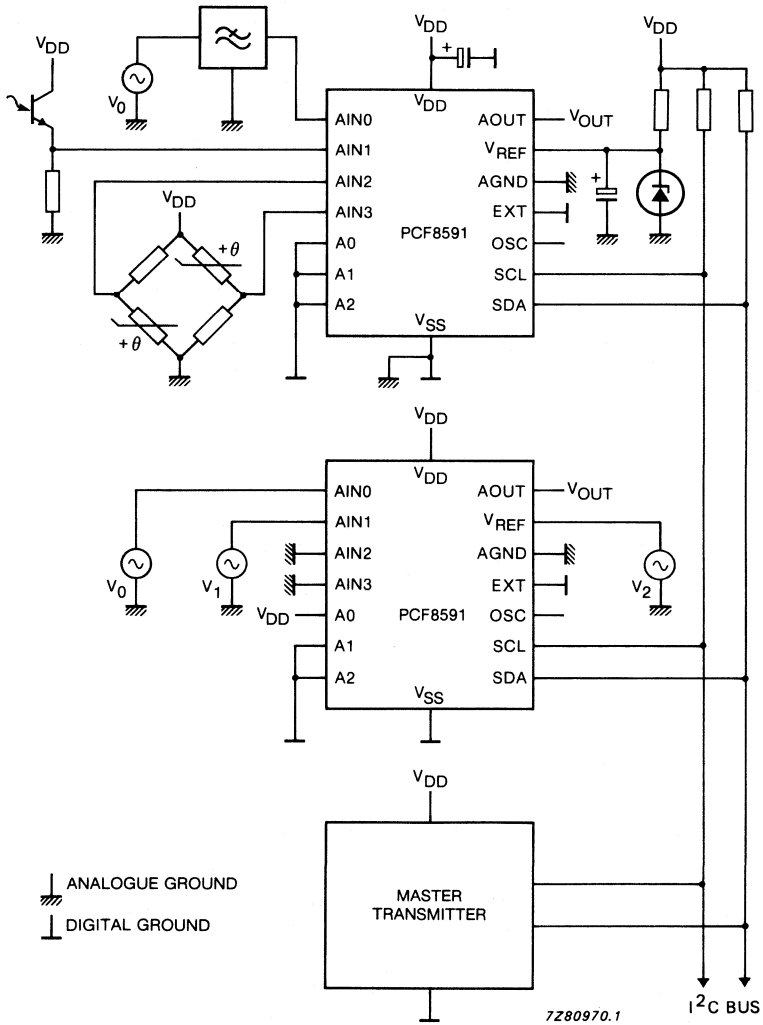


Fig. 18 Application diagram.

4-DIGIT LED-DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{CC}	4,5	5	15	V
Supply current all outputs OFF	V_{CC} = 5 V	I_{CC}	–	9,5	–	mA
Total power dissipation 24-lead DIL (SOT-101B)		P_{tot}	–	–	1000	mW
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINE

SAA1064P: 24-lead DIL; plastic (with internal heat spreader) (SOT-101B).

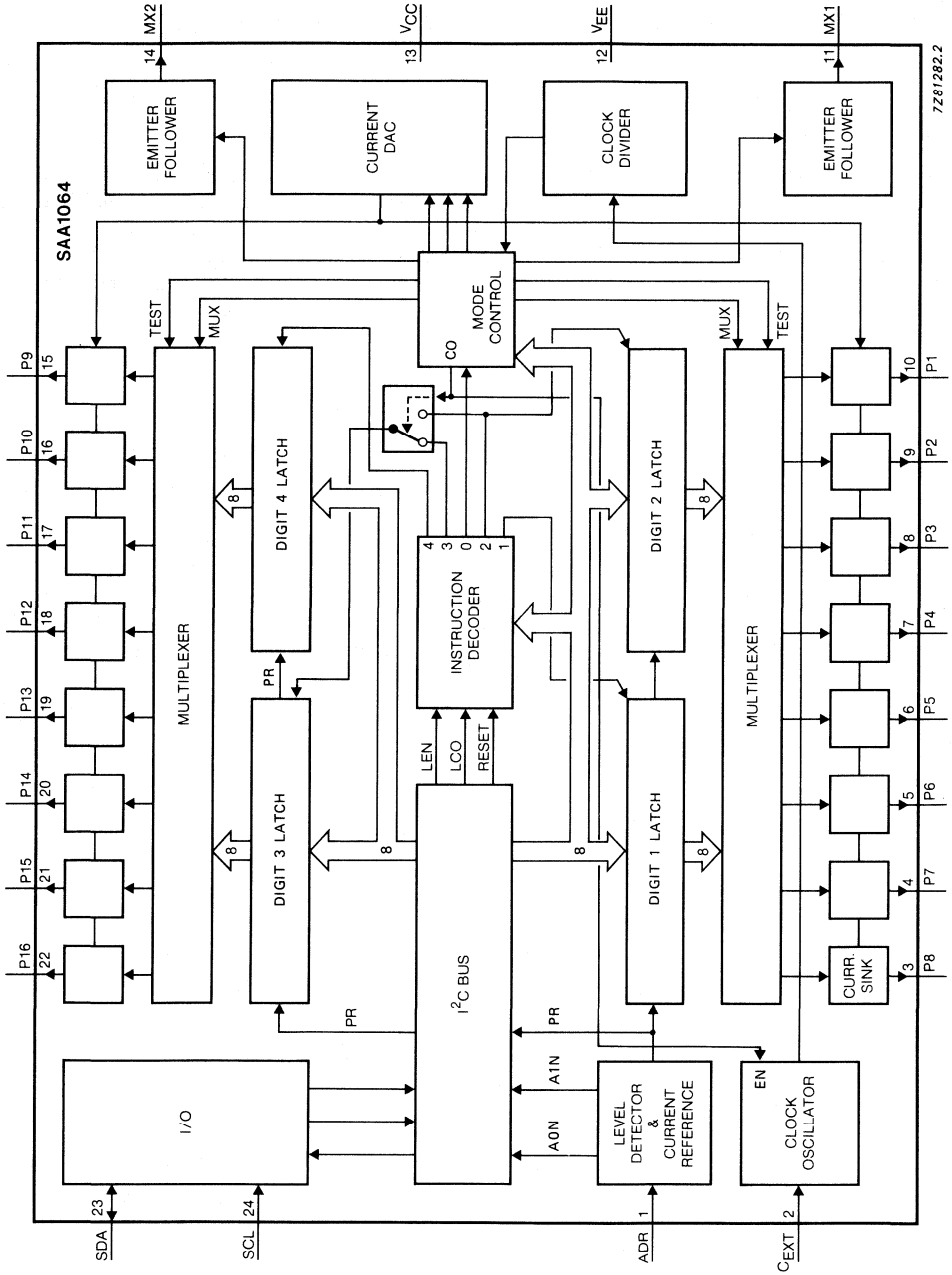


Fig. 1 Block diagram.

PINNING

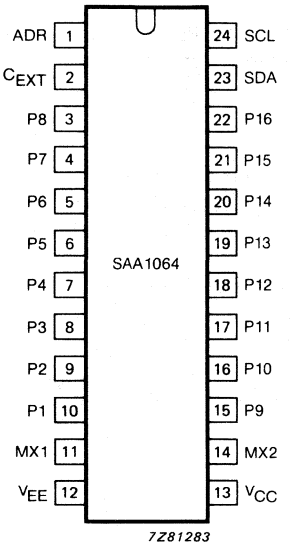


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

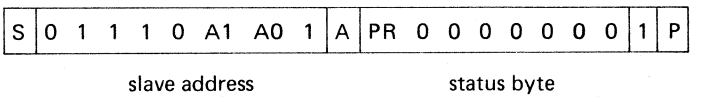


Fig. 3a I²C bus format; READ mode.

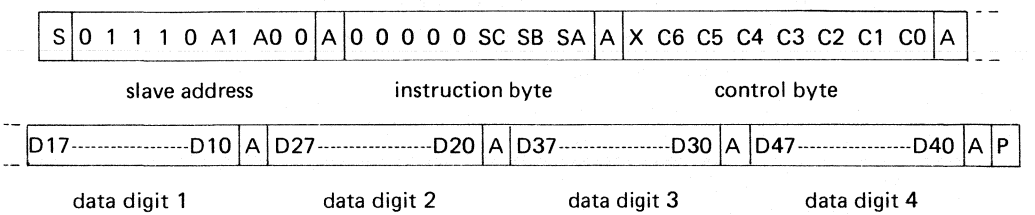


Fig. 3b I²C bus format; WRITE mode.

S = start condition
P = stop condition
A = acknowledge
X = don't care

A1, A0 = programmable address bits
SC SB SA = subaddress bits
C6 to C0 = control bits
PR = POWER RESET flag

Address pin ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, 3/8 V_{CC}, 5/8 V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

Status byte

Only one bit is present in the status byte, the POWER RESET flag. A logic 1 indicates the occurence of a power failure since the last time it was read out. After completion of the READ action this flag will be set to logic 0.

Subaddressing

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master.
The subaddress pointer will wrap around from 7 to 0.
The subaddresses are given as follows:

SC	SB	SA	sub-address	function
0	0	0	00	control register
0	0	1	01	digit 1
0	1	0	02	digit 2
0	1	1	03	digit 3
1	0	0	04	digit 4
1	0	1	05	reserved, not used
1	1	0	06	
1	1	1	07	

Control bits (see Fig. 4)

The control bits C0 to C6 have the following meaning:

C0 = 0	static mode, i.e. continuous display of digits 1 and 2
C0 = 1	dynamic mode, i.e. alternating display of digit 1 + 3 and 2 + 4
C1 = 0/1	digits 1 + 3 are blanked/not blanked
C2 = 0/1	digits 2 + 4 are blanked/not blanked
C3 = 1	all segment outputs are switched-on for segment test*
C4 = 1	adds 3 mA to segment output current
C5 = 1	adds 6 mA to segment output current
C6 = 1	adds 12 mA to segment output current

Data

A segment is switched ON if the corresponding data bit is logic 1. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4.
The MSBs correspond with outputs P8 and P16, the LSBs with P1 and P9. Digit numbers 1 to 4 are equal to their subaddresses (hex) 1 to 4.

* At a current determined by C4, C5 and C6.

SDA, SCL

The SDA and SCL I/O meet the I²C bus specification. For protection against positive voltage pulses on these inputs voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5,5 volt. Data will be latched on the positive-going edge of the acknowledge related clock pulse.

Power-on reset

The power-on reset signal is generated internally and sets all bits to zero, resulting in a completely blanked display. Only the POWER RESET flag is set.

External Control (C_{EXT})

With a capacitor connected to pin 2 the multiplex frequency can be set (see Fig. 5). When static this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

Segment outputs

The segment outputs P1 to P16 are controllable current-sink sources. They are switched on by the corresponding data bits and their current is adjusted by control bits C4, C5 and C6.

Multiplex outputs

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock-oscillator. In static mode MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly provided that the total power dissipation of the circuit is not exceeded. If this occurs external transistors should be connected to pins 11 and 14 as shown in Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 13)		V_{CC}	−0,5	18	V
Supply current (pin 13)		I_{CC}	−50	200	mA
Total power dissipation SOT-101 24-lead DIL		P_{tot}		1000	mW
SDA, SCL voltages		$V_{23,\ 24\text{-}12}$	−0,5	5,9	V
Voltages A0-MX1 and MX2-P16		$V_{1\text{-}11},\ V_{14\text{-}22}$	−0,5	V_{CC} + 0,5	V
Input/output current all pins	outputs OFF	± I	−	10	mA
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−65	+ 125	°C

THERMAL RESISTANCE

From crystal to ambient
24-lead DIL $R_{th\ cr\text{-}a}$ 35 K/W

CHARACTERISTICS

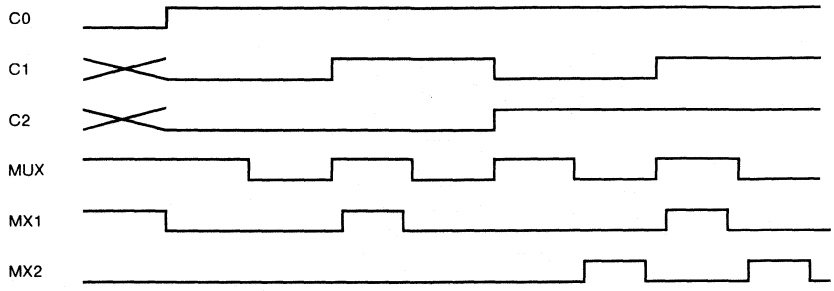
V_{CC} = 5 V; T_{amb} = 25 °C; voltages are referenced to ground (V_{EE} = 0 V); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 13)		V_{CC}	4,5	5,0	15	V
Supply current	all outputs OFF V_{CC} = 5 V	I_{CC}	7,0	9,5	14,0	mA
Power dissipation	all outputs OFF	P_d	–	50	–	mW
SDA; SCL bus (pins 23 and 24)						
Input voltages		$V_{23,24}$	0	–	5,5	V
Logic input voltage LOW		$V_{IL(L)}$	–	–	1,5	V
Logic input voltage HIGH		$V_{IH(L)}$	3,0	–	–	V
Input current LOW	$V_{23,24} = V_{EE}$	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{23,24} = V_{CC}$	I_{IH}	–	–	10	μA
SDA						
Logic output voltage LOW	I_O = 3 mA	$V_{OL(L)}$	–	–	0,4	V
Output sink current		I_O	3	–	–	mA
Address input (pin 1)						
Input voltage programmable address bits:						
A0 = 0; A1 = 0		V_1	V_{EE}	–	$3/16V_{CC}$	V
A0 = 1; A1 = 0		V_1	$5/16V_{CC}$	$3/8V_{CC}$	$7/16V_{CC}$	V
A0 = 0; A1 = 1		V_1	$9/16V_{CC}$	$5/8V_{CC}$	$11/16V_{CC}$	V
A0 = 1; A1 = 1		V_1	$13/16V_{CC}$	–	V_{CC}	V
Input current LOW	$V_1 = V_{EE}$	I_1	–	–	−10	μA
Input current HIGH	$V_1 = V_{CC}$	I_1	–	–	10	
External control (C_{EXT}) pin 2						
Switching level input						
Input voltage LOW		V_{IL}	–	–	$V_{CC}-2,5$	V
Input voltage HIGH		V_{IH}	$V_{CC}-1,5$	–	–	V
nput current	V_2 = 2 V	I_2	−140	−160	−180	μA
	V_2 = 4 V	I_2	140	160	180	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Segment outputs (P8 to P1; pins 3 to 10) (P9 to P16; pins 15 to 22)						
Output voltages	I_O = 15 mA	V_O	–	–	0,5	V
Output current HIGH	$V_O = V_{CC}$ = 15 V	I_O	–	–	± 10	μA
Output current LOW control bits HIGH C4, C5 and C6	V_O = 5 V	I_O	17,85	21	25	mA
Contribution of:						
control bit C4		I_O	2,55	3,0	4,0	mA
control bit C5		I_O	5,1	6,0	7,0	mA
control bit C6		I_O	10,2	12,0	14,0	mA
Relative segment 1 output accuracy with respect to highest value when:						
I_3 to I_{10} and I_{15} to I_{22} = 3 mA		ΔI_O	–	–	5	%
I_3 to I_{10} and I_{15} to I_{22} = 21 mA		ΔI_O	–	–	7	%
Multiplex 1 and 2 (pins 11 and 14)						
Output voltage (when ON)	I_O = 50 mA	V_O	V_{CC} 1,5	–	–	V
Output current HIGH (when ON)	V_O = 2 V	$I_{11}; I_{14}$	50	–	*	mA
Output current LOW (when OFF)	V_O = 2 V	$-I_{11}; -I_{14}$	50	70	100	mA
Output period	$C_{2\text{-}12}$ = 2,7 nF	T_{MPX}	5	–	10	ms
	$C_{2\text{-}12}$ = 820 pF	T_{MPX}	–	1,25	–	ms
	$C_{2\text{-}12}$ = 390 pF	T_{MPX}	–	666	–	μs
Output duty factor			48,4	–	–	%

* Value to be fixed.



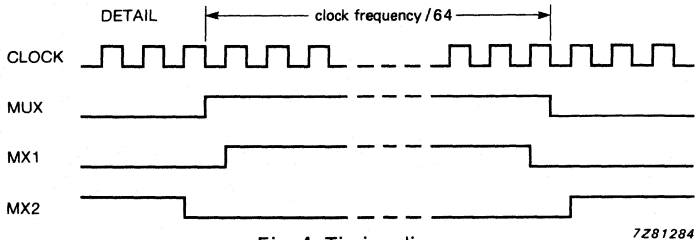


Fig. 4 Timing diagram.

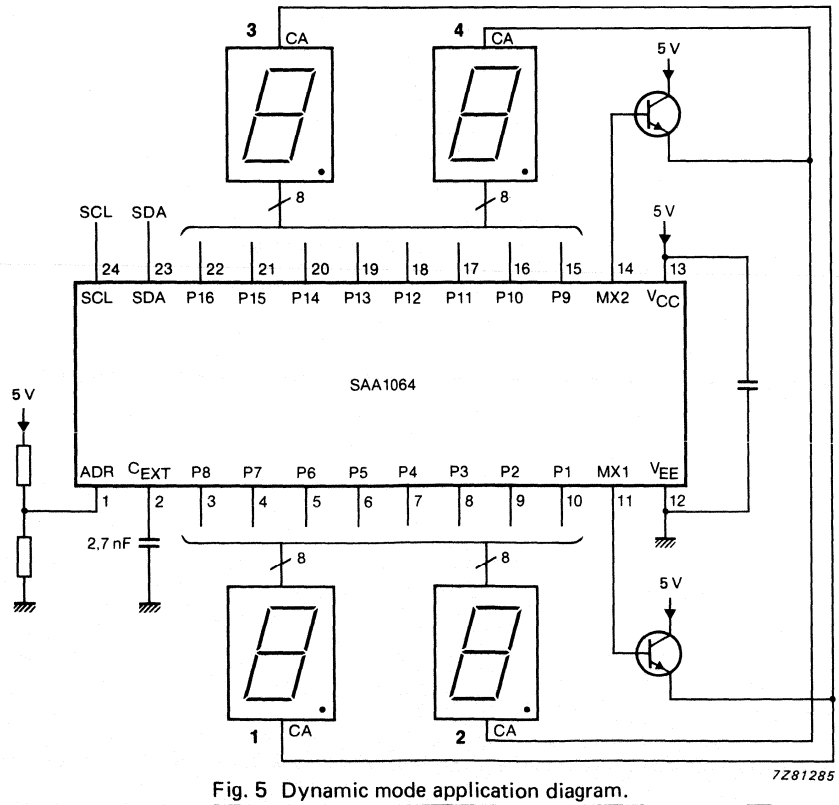


Fig. 5 Dynamic mode application diagram.

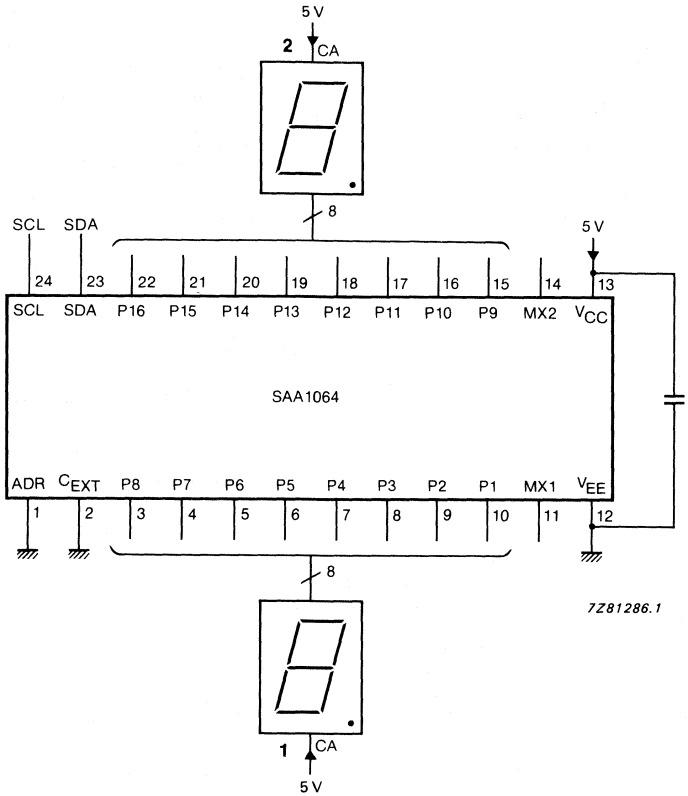


Fig. 6 Static mode application diagram.

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

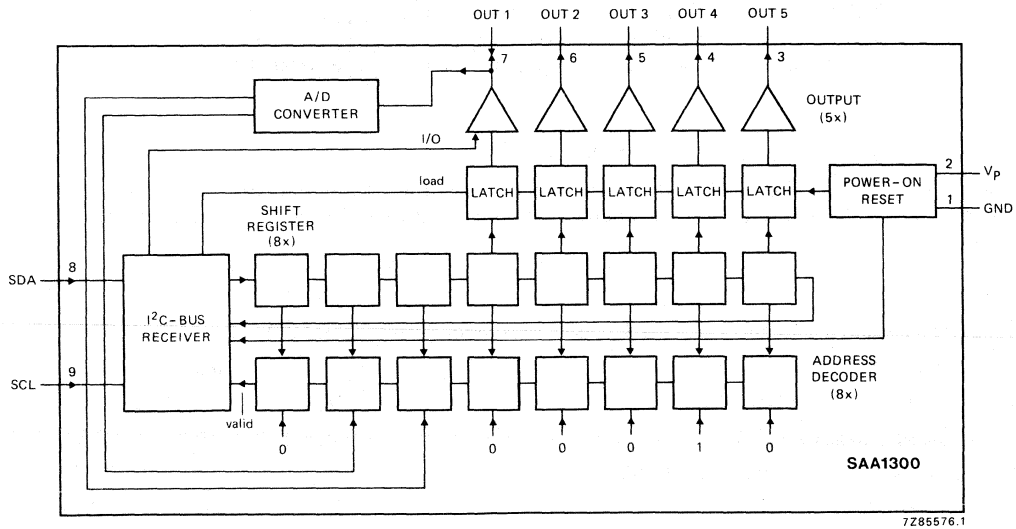


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max. 13,2	V
Input voltage range at SDA, SCL	V_I	−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I	−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O	−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max. 20	mA
Input current at OUT 1	I_I	max. 20	mA
Total power dissipation	P_{tot}	max. 825	mW
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power-on reset level output stage in "OFF' condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	μA
Input current LOW	I_{IH}	–	–	0,4	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+ 85	–	+ 150	mA
Maximum output current; source: "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi} = –100 μA	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V

* Outputs must not be driven simultaneously at maximum source current.

INFRARED REMOTE CONTROL TRANSCODER (RC-5)

GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available: one for RC-5 coded signals only; the other is selectable to accept (1) RC-5 coded signals only, or (2) RC-5 (extended) coded signals only. The input used is that at which an active code is first detected. Coded signals not in RC-5/RC-5(ext) format are rejected. Data input and output is by serial transfer, the output interface being compatible for I^2C bus operation.

Features

- Converts RC-5 or RC-5(ext) biphase coded signals into binary equivalents
- Two data inputs, one fixed (RC-5), one selectable (RC-5/RC-5(ext))
- Rejects all codes not in RC-5/RC-5(ext) format
- I^2C output interface capability
- Power-off facility
- Master/slave addressable for multi-transmitter/receiver applications in RC-5(ext) mode
- Power-on-reset for defined start-up

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,5 to	5,5 V
Supply current (quiescent) at V_{DD} = 5,5 V; T_{amb} = 25 °C	I_{DD}	max.	200 μA
Operating ambient temperature range	T_{amb}	−25 to	+85 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

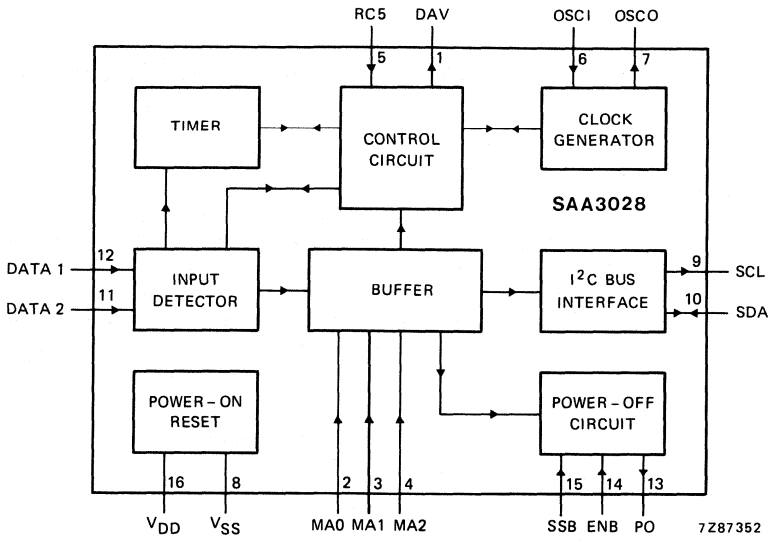


Fig. 1 Block diagram.

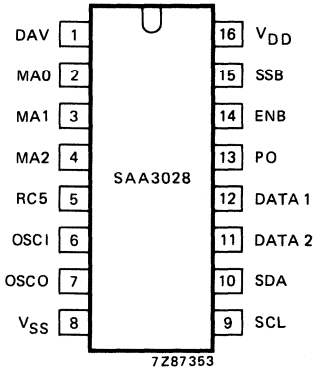


Fig. 2 Pinning diagram.

PINNING

1	DAV	data valid output with open drain N-channel transistor
2	MA0	master address inputs
3	MA1	master address inputs
4	MA2	master address inputs
5	RC5	data 2 input select
6	OSCI	oscillator input
7	OSCO	oscillator output
8	V_{SS}	negative supply (ground)
9	SCL	serial clock line (I^2C bus)
10	SDA	serial data line (I^2C bus)
11	DATA 2	data 2 input
12	DATA 1	data 1 input
13	PO	power-off signal output with open drain N-channel transistor
14	ENB	enable input
15	SSB	set standby input
16	V_{DD}	positive supply (+5 V)

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Input function

The two data inputs are accepted into the buffer as follows:

- DATA 1. Only biphase coded signals which conform to the RC-5 format are accepted at this input.
- DATA 2. This input performs according to the logic state of the select input RC5. When RC5 = HIGH, DATA 2 input will accept only RC-5 coded signals. When RC5 = LOW, DATA 2 input will accept only RC-5(ext) coded signals.

The input detector selects the input, DATA 1 or DATA 2, in which a HIGH to LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected.

Formats of RC-5 and RC-5(ext) biphase coded signals are shown in Figs 3 and 4 respectively; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Fig. 5.

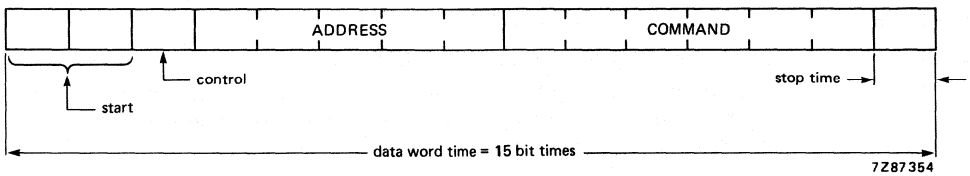


Fig. 3 RC-5 code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

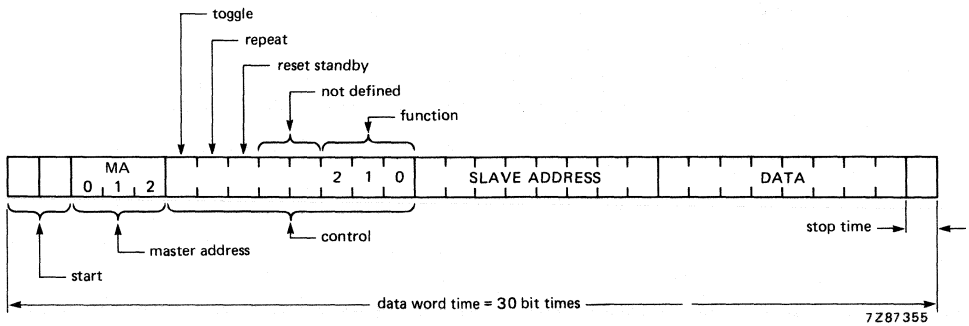


Fig. 4 RC-5(extended) code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

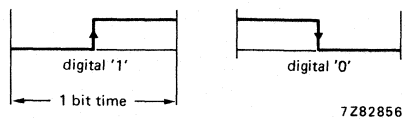


Fig. 5 Biphase code definition: RC-5 bit-time = $2^7 \times T_{OSC}$ = 1,778 ms (typical); RC-5(ext) bit-time = $2^6 \times T_{OSC}$ = 0,89 ms (typical), where T_{OSC} = the oscillator period time.

FUNCTIONAL DESCRIPTION (continued)

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I^2C interface. The information now held in the buffer is as follows:

RC-5 buffer contents		RC-5(ext) buffer contents	
• data valid indicator	1 bit	• data valid indicator	1 bit
• format indicator	1 bit	• format indicator	1 bit
• input indicator	1 bit	• input indicator	1 bit
• control	1 bit	• master address	3 bits
• address data	5 bits	• control	8 bits
• command data	6 bits	• slave address	8 bits
		• data	8 bits

The information assembled in the buffer is subjected to the following controls before being made available at the I^2C interface:

ENB = HIGH — Enables the set standby input SSB.

SSB = LOW — Causes power-off output PO to go HIGH.

PO = HIGH — This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW — This occurs according to the type of code being processed, as follows:

RC-5. When the binary equivalent value is transferred to the buffer.

RC-5(ext). When the reset standby bit is active and the master address bits are equal in value to the MA0, MA1, MA2 inputs.

At power-on, PO is reset to LOW.

DAV = HIGH — This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, then the new binary values are discarded.

Output function

The data is assembled in the buffer in the format shown in Fig. 6 for RC-5 binary equivalent values, or in the format shown in Fig. 7 for RC-5(ext) binary equivalent values. The data is output serially, starting from the left of the formats shown in Figs 6 and 7.

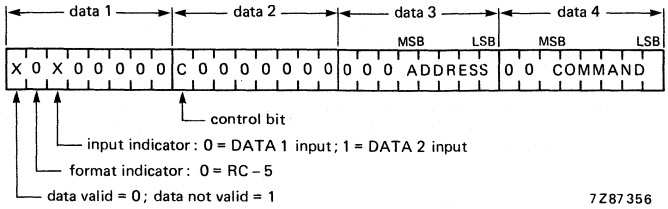


Fig. 6 RC-5 binary equivalent value format.

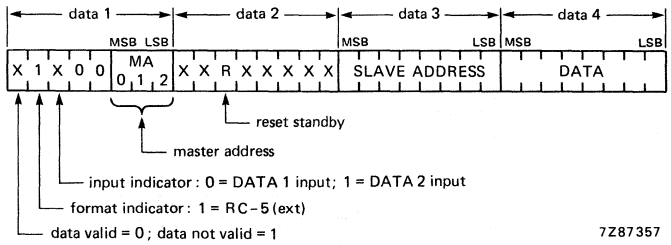


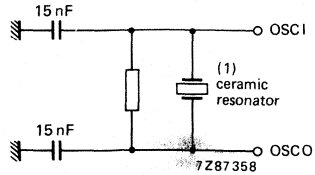
Fig. 7 RC-5(ext) binary equivalent value format.

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I^2C interface allows transmission on a bidirectional, two-wire I^2C bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110. Serial output of the slave address onto the I^2C bus starts from the left-hand bit.

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Fig. 8. The typical frequency of oscillation is 455 kHz.



(1) Catalogue number of ceramic resonator: 2422 540 98008.

Fig. 8 Oscillator circuit.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

I²C bus transmission

Formats for I²C transmission in low and high speed modes are shown respectively in Figs 9 and 10.

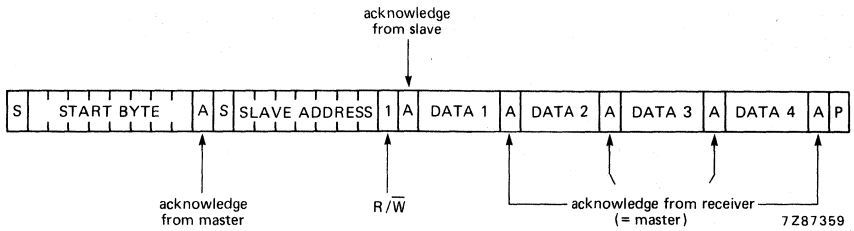


Fig. 9 Format for transmission in I²C low speed mode.

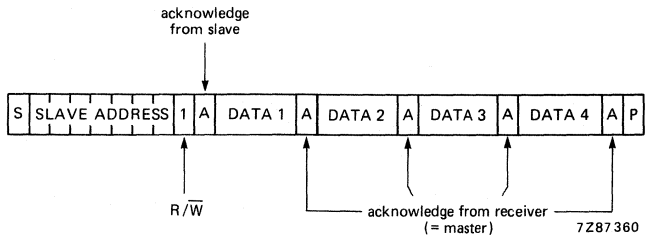


Fig. 10 Format for transmission in I²C high speed mode.

Note to Figures 9 and 10

When R/$\overline{W}$ bit = 0; the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.

When the receiver generates a NACK; the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).

When all data has been transmitted, the data line remains HIGH and the slave waits for P.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to	+15	V
Input voltage range	V_I	−0,5 to	(V_{DD}+0,5)	V*
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O	−0,5 to	(V_{DD}+0,5)	V*
Output current	$\pm I_O$	max.	10	mA
Power dissipation output OSCO	P_O	max.	50	mW
Power dissipation per output (all other outputs)	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}	−25 to	+85	°C
Storage temperature range	T_{stg}	−55 to	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,5	–	5,5	V
Supply current; quiescent at T_{amb} = 25 °C	5,5	I_{DD}	–	–	200	μA
Inputs						
MA0, MA1, MA2, DATA 1, DATA 2, RC5, SCL, ENB, SSB, OSCI						
Input voltage HIGH	4,5 to 5,5	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,5 to 5,5	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 5,5 V; T_{amb} = 25 °C	5,5	I_I	–	–	1	μA
Input leakage current at V_I = 0 V; T_{amb} = 25 °C;	5,5	$-I_I$	–	–	1	μA
Outputs						
DAV, PO						
Output voltage LOW at I_{OL} = 1,6 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
OSCO						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	4,5 to 5,5	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,3 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at T_{amb} = 25 °C; V_O = 5,5 V	5,5	I_{OR}	–	–	1	μA
V_O = 0 V	5,5	I_{OR}	–	–	1	μA
SDO						
Output voltage LOW at I_{OL} = 2 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
Oscillator						
Max. oscillator frequency (Fig. 8)	4,75	f_{OSCI}	500	–	–	kHz

VPS DATALINE PROCESSOR

GENERAL DESCRIPTION

The SAA4700 is a bipolar integrated circuit designed for use in dataline receivers and incorporates a dataline slicer and decoder. The slicer extracts the dataline signal from the video signal and regenerates the dataline clock. It also provides signals for the decoder. The decoder decodes the binary data that is transmitted in line 16 of every first field of a composite video signal (Video Programming Signal and Video-recording Programming by Teletext, VPS and VPT systems). The decoded information (words 5 and 11 to 14) is accessed via the built-in I^2C-bus interface. The information can then be used to program a video cassette recorder to start and stop the recording of a television program at the correct time, regardless of a delay or extension in the transmission time of the required program.

Features

- Adaptive sync slicer with buffered composite sync output
- Adaptive data slicer
- Dataline clock regenerator
- Field selection and line 16 decoding
- Startcode and biphase check
- Storage of dataline information
- I^2C-bus transmitter

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pins 15 and 16)		V_P	4.5	5	5.5	V
Supply current (pins 15 and 16)	V_P = 5 V	I_P	–	20	25	mA
Composite video amplitude (sync-to-white)		$CVBS_I$	0.5	1.0	1.4	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

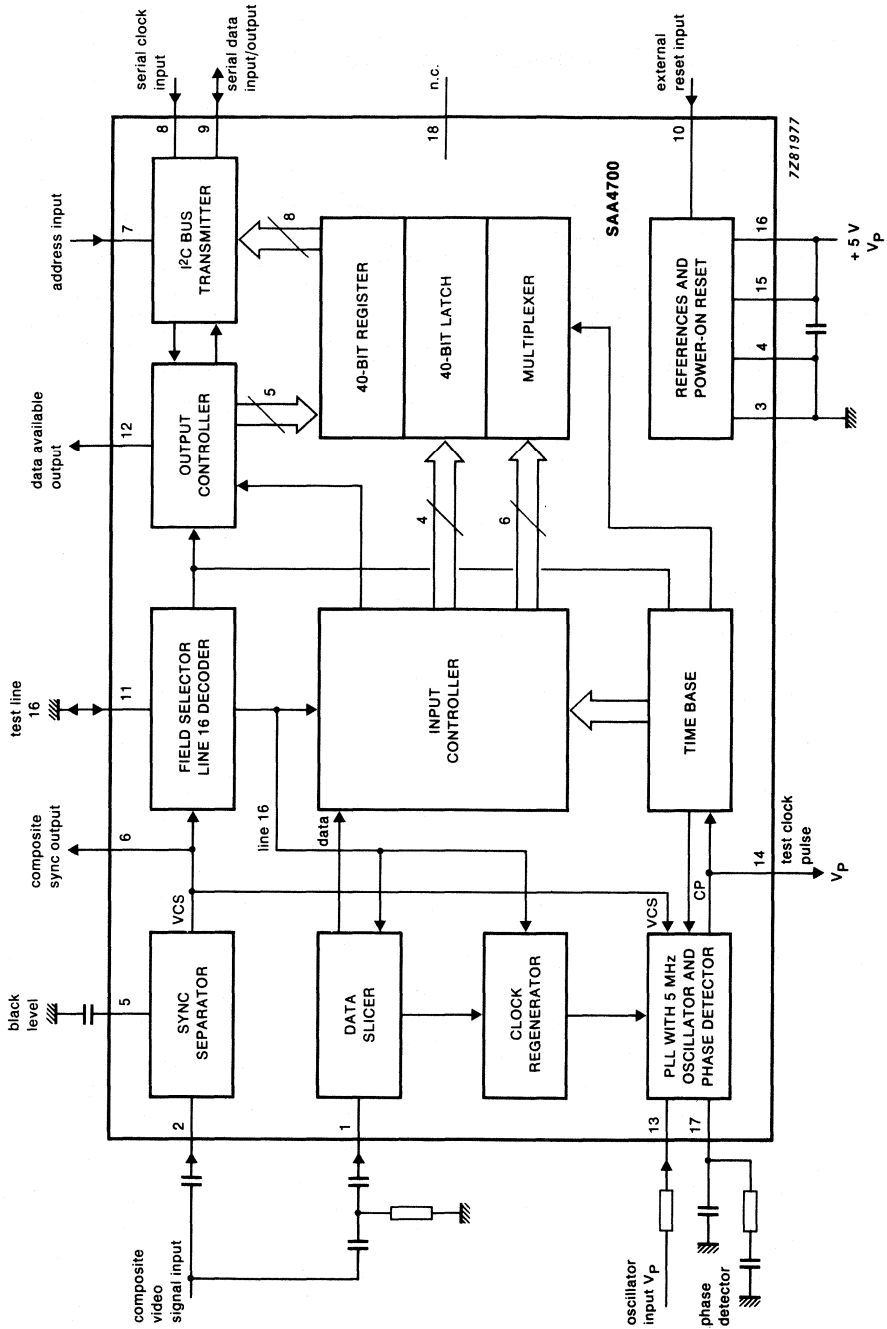


Fig. 1 Block diagram.

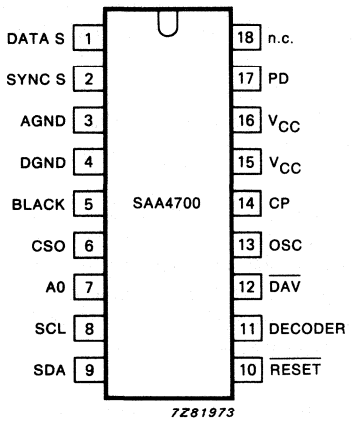


Fig. 2 Pinning diagram.

PINNING

1	Data slicer input	composite video
2	Sync separator input	burst sync (CVBS)
3	Analogue ground	
4	Digital ground	
5	Black level	
6	Composite sync output	
7	Address input	
8	Serial clock input	I^2C-bus
9	Serial data input/output	I^2C-bus
10	External reset input	
11	Test line 16	
12	Data available output	
13	Oscillator input	
14	Test clock pulse	
15	Digital supply voltage	
16	Analogue supply voltage	
17	Phase detector	
18	Not connected	

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Dataline 16

The information contained on dataline 16 consists of fifteen 8-bit words. The total information content is shown in Fig. 4. A timing diagram of dataline 16 is shown in Fig. 5 and a survey of the Video Tape Recorder (VTR) control labels is shown in Fig. 6.

From the fifteen 8-bit words, the SAA4700 extracts words 5 and 11 to 14. The contents of these words can be requested via the built-in I^2C-bus interface. The circuit is fully transparent, thus each bit is transferred without modification with only the sequence of words being changed. Words 11 to 14 are transmitted first followed by word 5.

By evaluating the sliced sync signal the SAA4700 can identify the beginning of dataline 16 in the first field. The dataline decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection see Fig. 7) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in a register bank. If no biphase error has occured, the contents of the register bank are transferred to a second register bank by the data valid control signal. If the system has been addressed, this transfer will be delayed until the next start or stop condition of the I^2C-bus has been received.

The last bit of correct information on the dataline remains available until it is read via the I^2C-bus. Once the stored information has been read it is considered to be no longer valid and the internal new data flag is reset. Subsequently, if the circuit is addressed, the only VPS data that will be sent back is "FFF . . . F". The same conditions apply after power-up when no data can be read out. New data is available after reception of another error-free dataline 16.

External $\overline{\text{RESET}}$ (pin 10)

The SAA4700 provides an internal power-on reset. When using this facility pin 10 should be connected to V_P or, if External $\overline{\text{RESET}}$ is to be used pin 10 should be connected to V_P via a 10 kΩ pull-up resistor.
When External $\overline{\text{RESET}}$ is used, pin 10 is active LOW and forces the following:

- I^2C-bus not to acknowledge
- Data available output ($\overline{\text{DAV}}$ active LOW) at pin 12 to go HIGH
- I^2C-bus transfer register to "FFFF"

CVBS input (pins 1 and 2)

The composite video signal (CVBS) is applied to the sync separator (pin 2) via a decoupling capacitor and to the data slicer (pin 1) via an RC high-pass filter. To enable proper storage of the sync value in the decoupling capacitor, the sync generator output resistance should not exceed 1 kΩ.

Black level (pin 5)

The capacitor connected to pin 5 stores the black level value for the adaptive sync slicer.

Composite sync out (pin 6)

This pin provides a composite sync signal output for customer application.

$\overline{\text{DAV}}$ output (pin 12)

The data available output at pin 12 is set LOW after an error free dataline 16 is received. The $\overline{\text{DAV}}$ output returns to HIGH after the beginning of the next first field. If no valid data is available $\overline{\text{DAV}}$ remains HIGH. A short duration pulse (1 μs) is inserted at the beginning of dataline 16 it will ensure that a HIGH-to-LOW transmission occurs which can then be used for triggering (see Fig. 8).

5 MHz oscillator and phase detector (pins 13 and 17)

The resistor connected between pin 13 and V_P determines the current into the current controlled oscillator. The RC network connected to pin 17 acts as a low pass filter for the phase detector.

Power supply (pins 3, 4, 15 and 16)

To prevent crosscoupling the IC provides separate power supply connectors;

- pin 3 = analogue ground
- pin 4 = digital ground
- pin 15 = digital supply voltage
- pin 16 = analogue supply voltage

I^2C-bus address input (pin 7)

The I^2C-bus address input (A0) provides the two addresses 20H and 22H.

I^2C-bus

The internally latched data from words 5 and 11 to 14 can be clocked out via the I^2C-bus interface by a bus master. The lines are the serial clock input (SCL) at pin 8 and the serial data input/output (SDA) at pin 9. The SAA4700 can operate only as a slave transmitter on the bus. Data format is shown in Fig. 3.

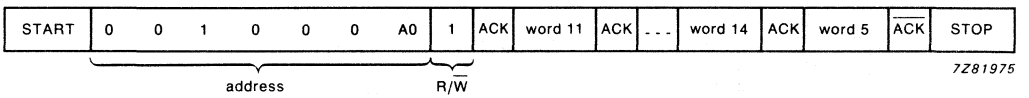


Fig. 3 I^2C-bus data format.

- The MSB of each word is transmitted first
- There is no restriction on the number of words to be transmitted, but if more than five words are requested from word 6 onwards, the content will be "FF . . . . FF".
- Normally every dataline transmission has to be ended with a STOP condition (as shown in Fig. 3).

Word number	Content
1	Run in
2	Start code
3	Program source identification (binary coded)
4	Program source identification (ASCII sequential)
5	Sound and VTR control information
6	Program/Test picture identification
7	Internal information exchange
8	Address assignment of signal distribution
9	
10	Messages/Commands
11	VTR Control Information
12	
13	
14	
15	Reverse

Fig. 4 Total information of data line 16.

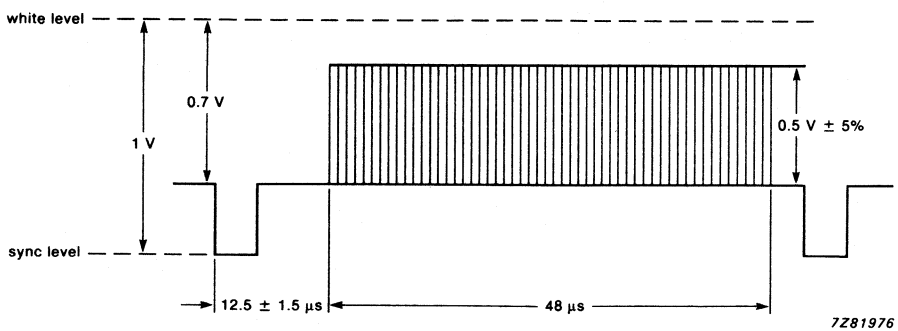


Fig. 5 Timing diagram of dataline 16; modulation depth 71.4%.

	VTR Control information																							
Word-no.	11								12								13							14
Bit-no.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22–25	26–31
Label binary	Address range		Day					Month				Hour					Minute						Nation	Program Source
			Special System Code																					
System Status Code	1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	NC... NC	PC. . . . PC
Pause Code	1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	NC. . NC	PC. . . . PC
Interrupt Code	1	X	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	NC. . NC	PC. . . . PC

Word 5, bit-no. 1 2 3 4 5 6 7 8:

	Bit 1	Bit 2	Status
Label binary	0	0	2-Channel
	0	1	Mono
	1	0	Stereo
System Status Code	1	1	2-Channel
	Bit 3	**Bit 4**	
Pause Code	1	0	free
Interrupt Code	0	1	free

Where:

X = 0 or 1 (bit)

NC is the Nation Code

PC is the Program Source Code

Fig. 6 VTR control information of dataline 16.

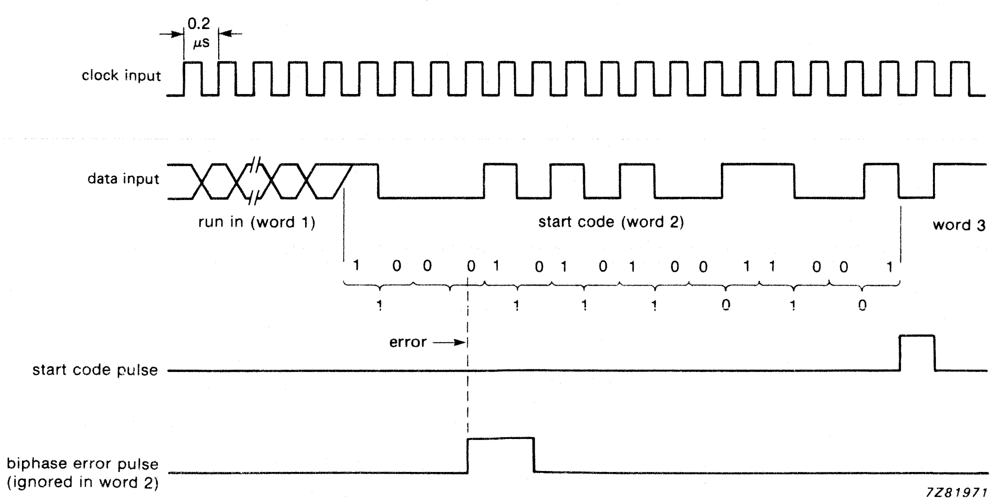


Fig. 7 Timing diagram of start code detection.

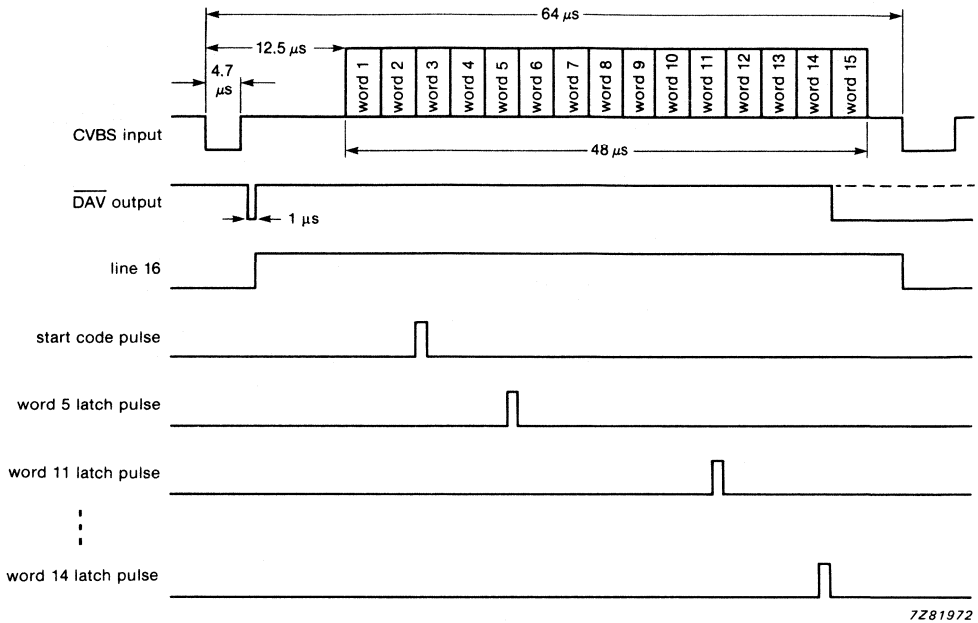


Fig. 8 Timing diagram of the data available output and word latch pulses.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pins 15 and 16)	V_P	4.5	5.5	V
Storage temperature range	T_{stg}	−20	+ 125	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a} \leqslant 78$ K/W

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; external components as shown in Fig. 9, unless otherwise specified. CVBS signal according to VPS, VPT standard. All voltages are referenced to ground (pins 3 and 4) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pins 15 and 16)		V_P	4.5	5.0	5.5	V
Supply current (pins 15 and 16)		I_P	–	20	25	mA
Video input and sync separator (pins 1, 2)						
Data amplitude		V_1	0.25	0.5	0.7	V
Sync amplitude	negative going	V_2	0.1	–	0.6	V
CVBS input voltage sync-to-white	note 1	$CVBS_I$	0.5	1.0	1.4	V
Source impedance		Z_s	–	–	1.0	kΩ
Composite sync output (pin 6)						
Output voltage LOW		V_{OL}	–	–	0.4	V
Output voltage HIGH		V_{OH}	2.4	–	–	V
Output current LOW		I_{OL}	–	–	0.2	mA
Output current HIGH		I_{OH}	–	–	0.5	mA
Sync separator delay time		t_d	–	0.3	–	μs
External reset input (pin 10)						
Input voltage LOW	active reset	V_{IL}	–	–	0.4	V
Input voltage HIGH	non-active reset	V_{IH}	2.4	–	–	V
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	nA
$\overline{\text{DAV}}$ **output** (pin 12)	note 2					
Output voltage LOW		V_{OL}	–	–	0.4	V
Output voltage HIGH		V_{OH}	2.4	–	–	V
Output current LOW		I_{OL}	–	–	0.5	mA
Output current HIGH		I_{OH}	–	–	10	nA
Address input A0 (pin 7)						
Input voltage LOW (bus address 22H)		V_{IL}	–	–	0.4	V
Input voltage HIGH (bus address 20H)		V_{IH}	2.4	–	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
I²C-bus (pins 8 and 9)						
Input current	0.9 V_{CC}	I_I	–	–	10	μA
Input capacitance		C_I	–	–	10	pF
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Clock frequency		f_{CL}	–	–	100	kHz
Pulse duration LOW		t_{LOW}	4.7	–	–	μs
Pulse duration HIGH		t_{HIGH}	4.0	–	–	μs
SDA output	I_{OL} = 3 mA	V_{OL}	–	–	0.4	V

Notes to the characteristics

1. With standard sync and data amplitude of 68 to 75% black-white.
2. If the $\overline{DAV}$ output (open collector) is used, a pull-up resistor to V_{CC} is necessary.

DEVELOPMENT DATA

APPLICATION INFORMATION

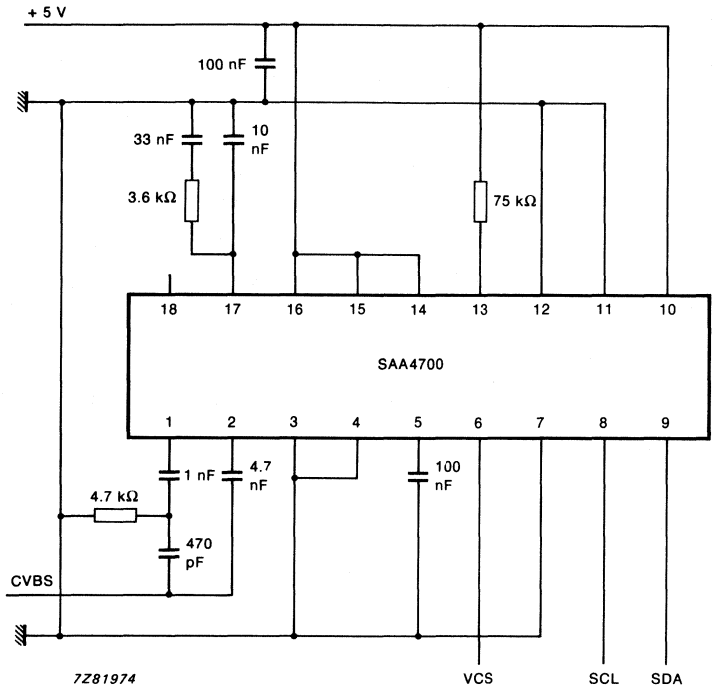


Fig. 9 Application circuit.

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUITS
(ECCT)

GENERAL DESCRIPTION

The SAA5243 series are MOS N-channel integrated circuits which perform all the digital logic functions of a 625-line World System Teletext decoder. The SAA5243 series operate in conjunction with the teletext video processor SAA5231, standard static RAMs and are controlled via the 2-wire I²C-bus. The devices can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 2 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language section of up to seven different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C-bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- Odd/even field output for de-interlaced displays

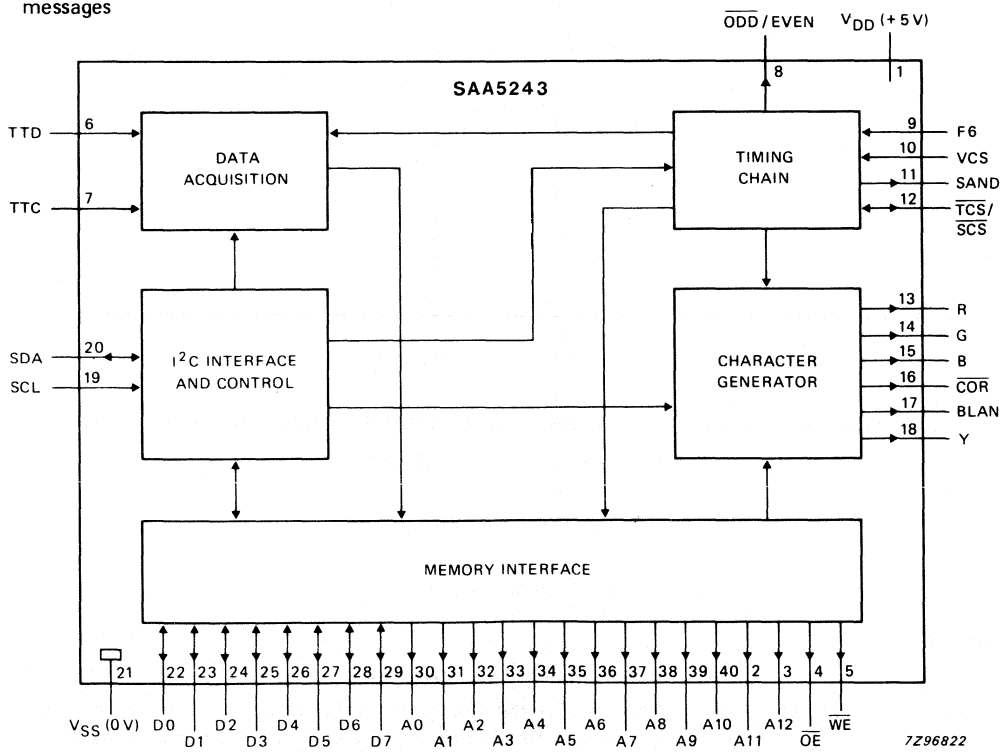


Fig.1 Block diagram.

PACKAGE OUTLINE 40-lead DIL; plastic (SOT-129).

ORDERING INFORMATION

type number	version
SAA5243P/E/M2	West European languages
SAA5243P/H	East European languages
SAA5243P/K	Arabic and English languages
SAA5243P/L	Arabic and Hebrew languages

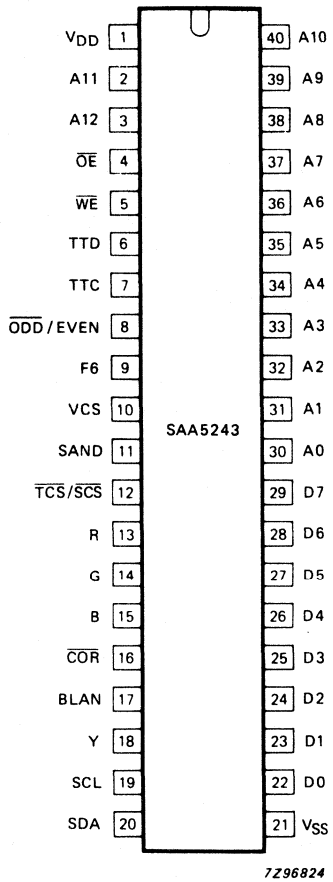


Fig.2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.

5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct DC level following the external AC coupling.
7	TTC	**Teletext Clock**: 6.9375 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
8	$\overline{ODD}$/EVEN	**$\overline{Odd}$/Even**: for interlaced mode, the output changes once per field at 2 μs before the end of line 311 (624). The output is high for even fields and low for odd fields.
9	F6	**Character display clock**: 6 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{TCS}/\overline{SCS}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig.6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue**: these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{COR}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C-bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C-bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	DO-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 1	V_{DD}	−0.3	7.5	V
Input voltage range					
VCS, SDA, SCL, D0-D7		V_I	−0.3	7.5	V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$		V_I	−0.3	10.0	V
Output voltage range					
SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, $\overline{ODD}/EVEN$, R, G, B, BLAN, $\overline{COR}$, Y		V_O	−0.3	7.5	V
$\overline{TCS}/\overline{SCS}$		V_O	−0.3	10.0	V
Storage temperature range		T_{stg}	−20	+125	°C
Operating ambient temperature range		T_{amb}	−20	+70	°C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.0	–	7.0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
DC input voltage range	V_I	−0.3	–	+ 10.0	V
AC input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1.0	–	7.0	V
AC input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1.5	–	7.0	V
Input peaks relative to 50% duty cycle	$\pm V_P$	0.2	–	3.5	V
TTC clock frequency	f_{TTC}	–	6.9375	–	MHz
F6 clock frequency	f_{F6}	–	6.0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
at I_{OH} = 0.1 mA	V_{OH}	2.4	–	6.0	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time between 3.0 V and 1.0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5.5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0.2 mA	V_{OL}	0	–	0.25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1.1	–	3.1	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 0.9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3.3 V and 3.8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3.8 V and 0.4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1.0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6.0	V
Output fall time with a load resistor of 1.2 kΩ to 6 V and measured between 5.5 V and 1.5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1.2 kΩ to 6 V and measured on the falling edges at 3.5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C-bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig.3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2.0 V; data stable 0 $\leqslant$ 0.8 V (see Fig.4).
5. The TTC and F6 inputs have internal clamping diodes and are AC coupled (see Fig.3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C-bus timing see Fig.8.
8. For details of RAM timing see Fig.9.
9. For details of synchronization timing see Fig.5.
10. For details of display output timing see Fig.7.
11. The I^2C-bus timings are referred to V_{IH} = 3 V and V_{IL} = 1.5 V. For waveforms see Fig.8.
12. The memory interface timings are referred to V_{IL} = 1.5 V. For waveforms see Fig.9.

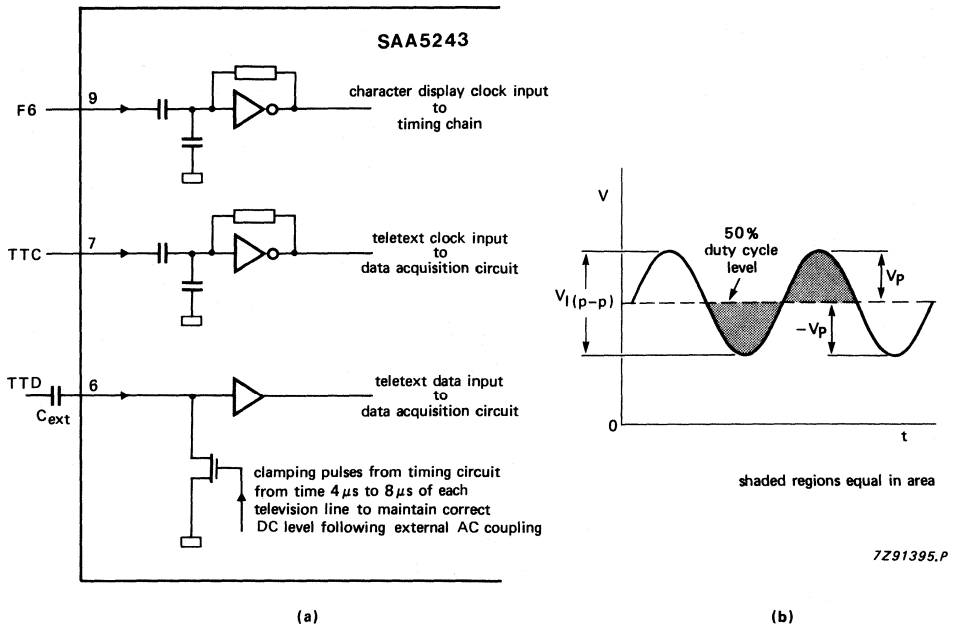
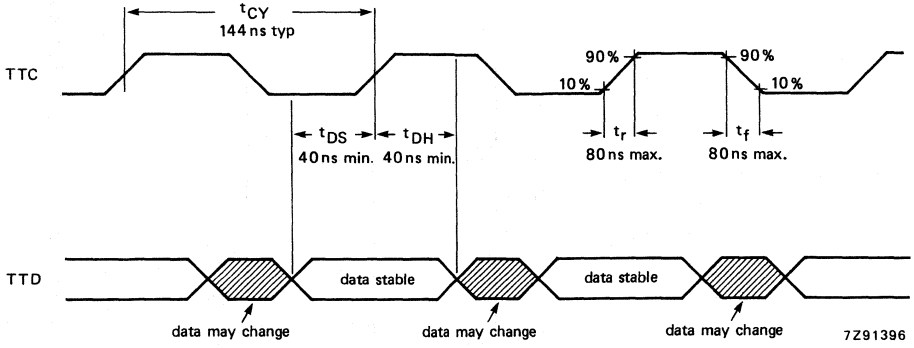


Fig.3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2.0 V; 0 is $\leqslant$ 0.8 V.

Fig.4 Teletext data input timing.

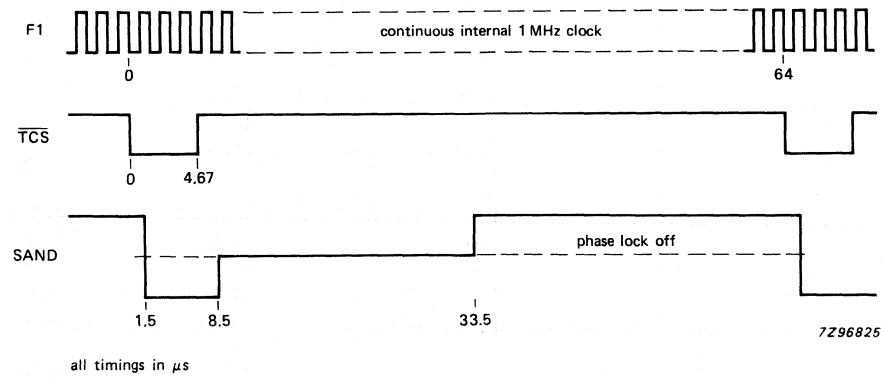
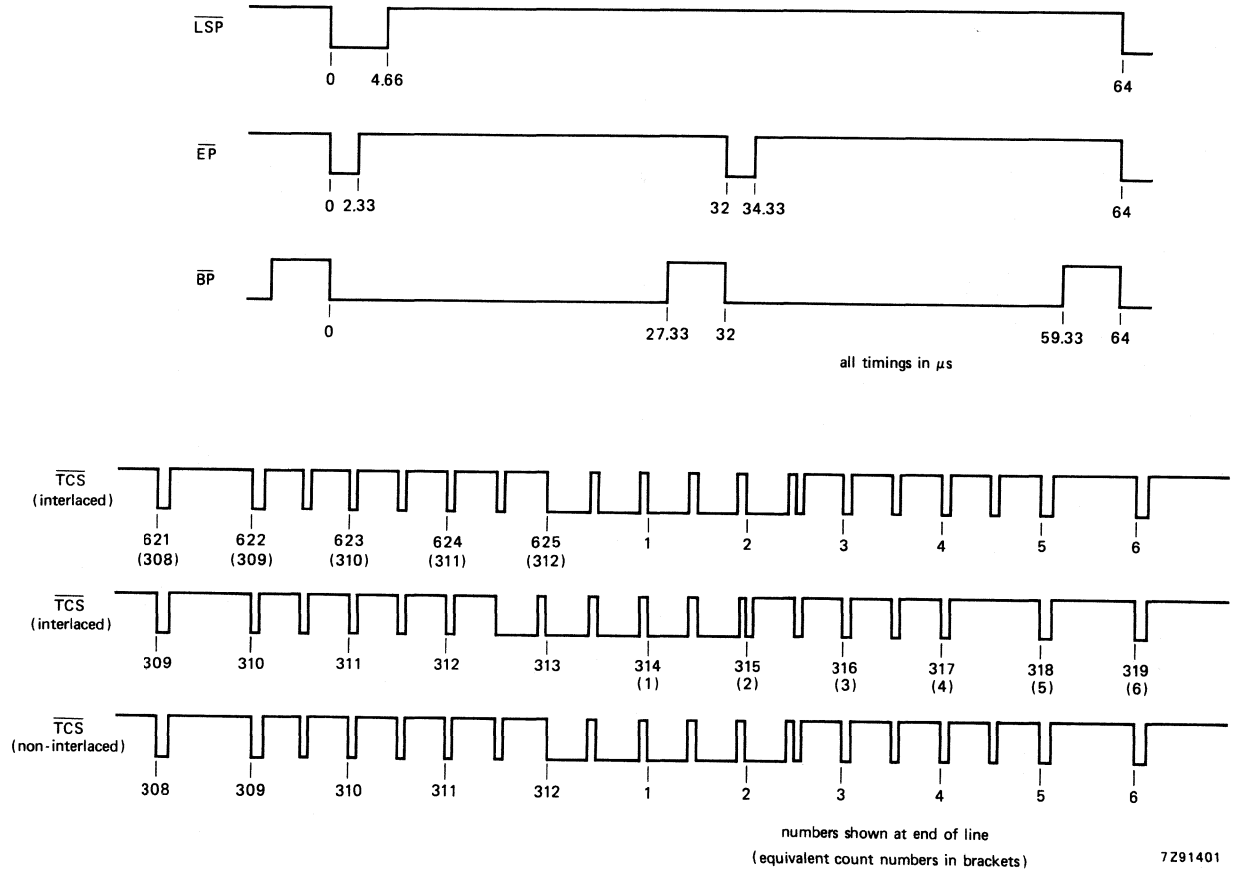


Fig.5 Synchronization timing.



Line sync pulses ($\overline{LSP}$), equalizing pulses ($\overline{EP}$) and broad pulses ($\overline{BP}$) are combined to provide the text composite sync waveform ($\overline{TCS}$) as shown. All timings measured from falling edge of $\overline{LSP}$ with a tolerance of ± 100 ns.

Fig.6 Composite sync waveforms.

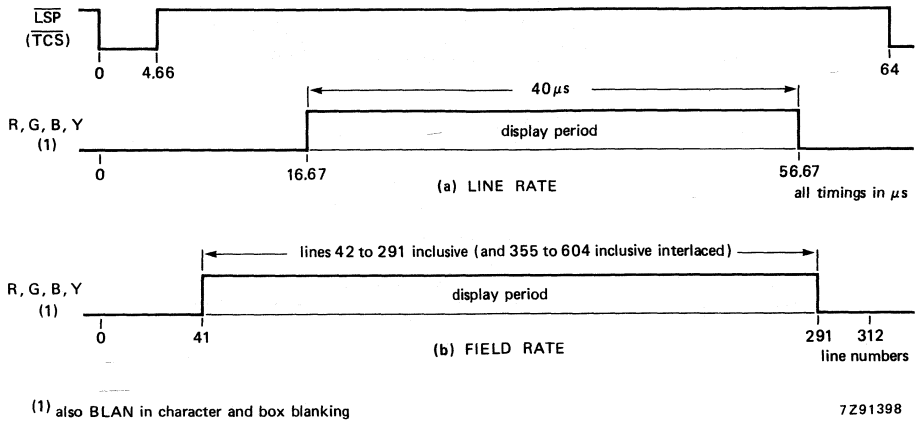


Fig.7 Display output timing (a) line rate (b) field rate.

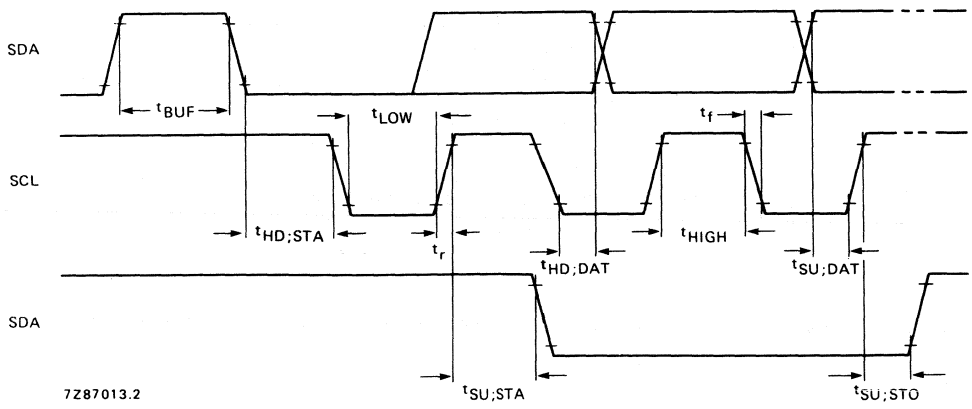


Fig.8 I²C-bus timing.

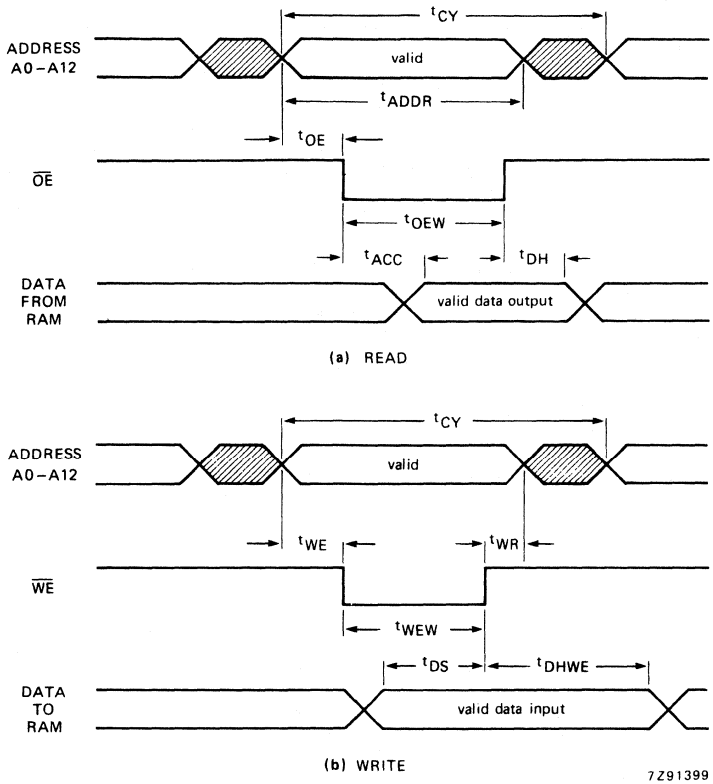
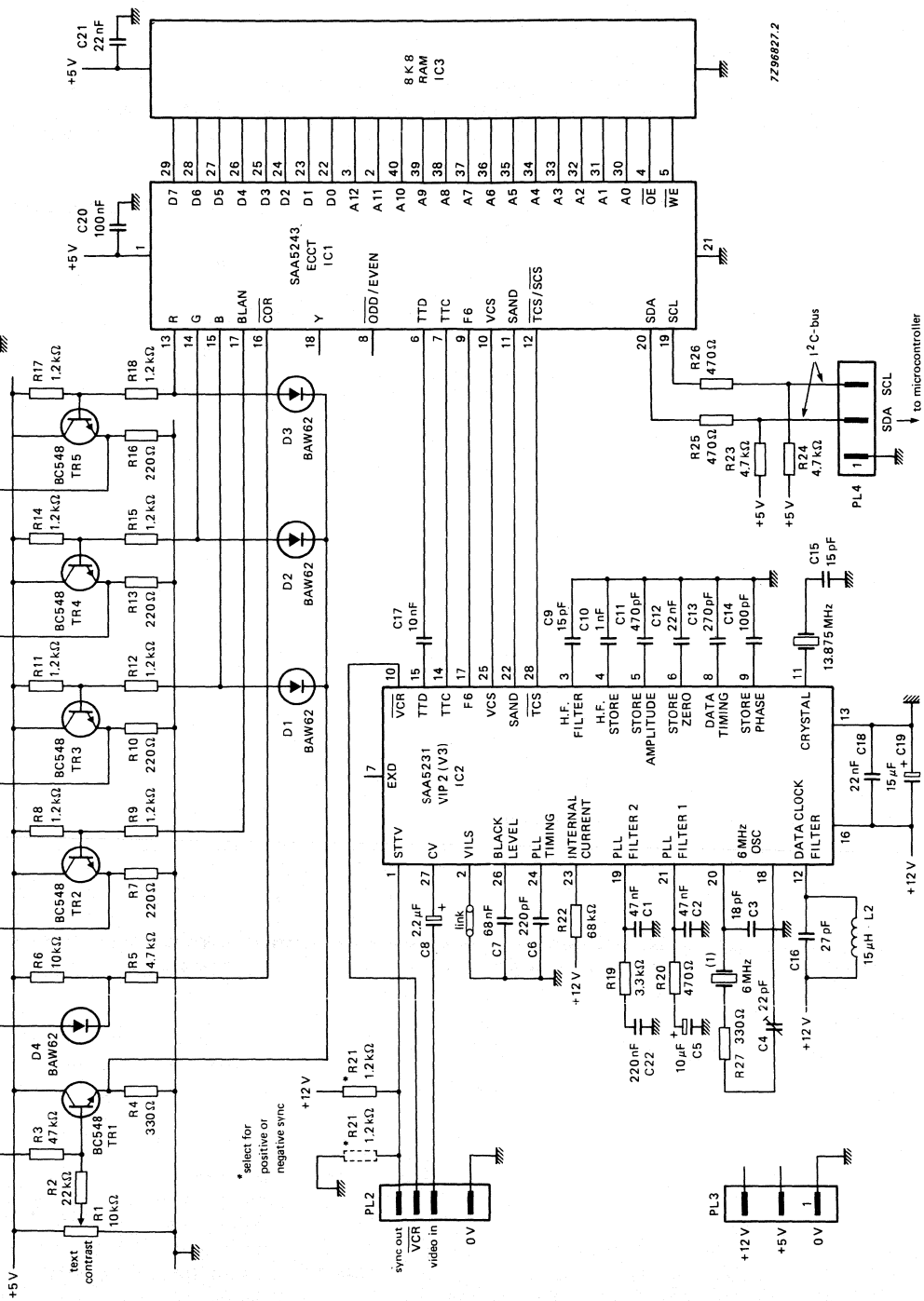


Fig.9 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION



(1) Ceramic resonator e.g. Kyocera KBR 6.0 M.

Fig. 10 ECCT based multi-page decoder circuit diagram.

APPLICATION INFORMATION (continued)

ECCT page memory organization

The organization of a page memory is shown in Fig.11. The ECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF ECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

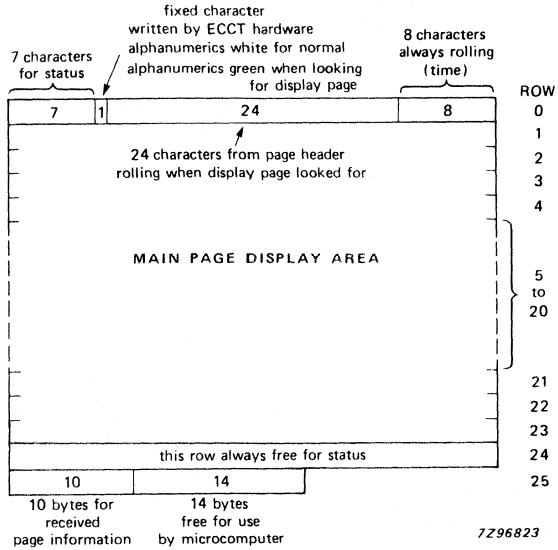


Fig.11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
PBLF	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by ECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

ECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 ECCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
—	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
—	—	—	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
—	—	—	—	—	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
—	—	—	—	CLEAR MEM.	A2	A1	A0	R8	Active chapter
—	—	—	R4	R3	R2	R1	R0	R9	Active row
—	—	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

— bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

APPLICATION INFORMATION (continued)

Table 2 (continued)

Where:

R1 Mode	
T0, T1	interlace/non-interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode	
BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C-bus.

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for DO CARE bits.
When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

APPLICATION INFORMATION (continued)

CHARACTER SETS

Several versions of the ECCT are available, offering a variety of character sets. The full character sets are shown in Tables 4a to 4d.

The world system teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14. These bits are automatically decoded by the ECCT, the resulting character sets are shown in Tables 6a to 6d. For certain languages, control software processing of the extension packet data may be required for optimum useage of the range of available characters. See Fig. 12 for alphanumeric and graphic options.

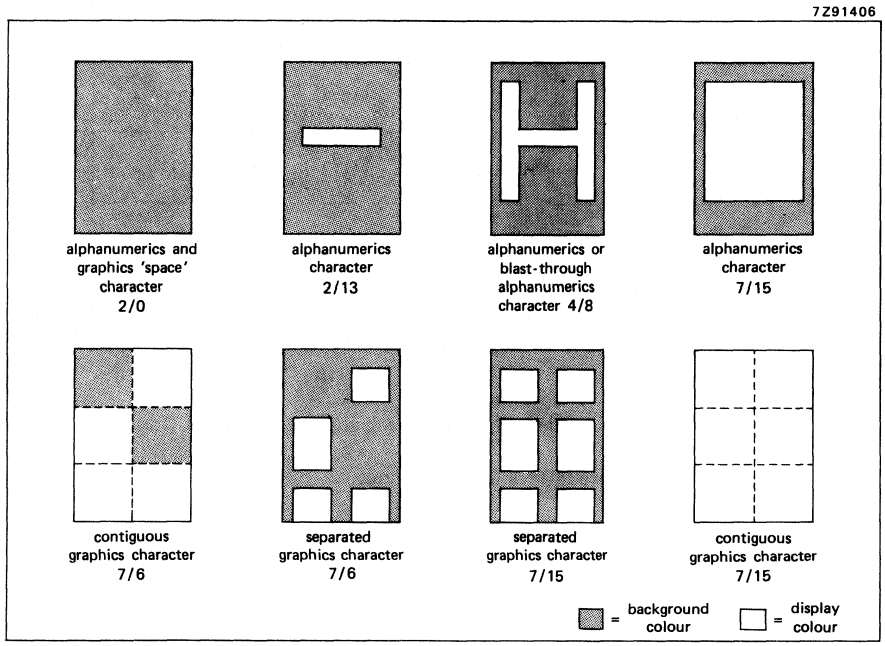


Fig.12 Alphanumeric and graphic options.

Table 4a Character data input decoding, West European languages (SAA5243P/E/M2)

BITS b_4 b_3 b_2 b_1 ↓	row \ column →	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
		b_8 0 b_7 0 b_6 0 b_5 0	0 0 0 1	0 or 1 0 1 0	0 0 1 0	0 or 1 0 1 0	0 0 1 0	0 1 0 0	0 1 0 1	0 1 1 0		0 1 1 1		1 0 0 0	1 0 0 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
0 0 0 0	0	alpha-numerics black	graphics black			0		§	P	°		p		@	É	é	à	i	Á
0 0 0 1	1	alpha-numerics red	graphics red	!		1		A	Q	a		q		—	é	ù	è	¿	À
0 0 1 0	2	alpha-numerics green	graphics green	"		2		B	R	b		r		¼	ä	à	â	ü	È
0 0 1 1	3	alpha-numerics yellow	graphics yellow	#		3		C	S	c		s		£	#	£	é	ç	Í
0 1 0 0	4	alpha-numerics blue	graphics blue	$		4		D	T	d		t		$	¤	$	ï	$	Ï
0 1 0 1	5	alpha-numerics magenta	graphics magenta	%		5		E	U	e		u		←	↑	ä	Ä	¤	Ó
0 1 1 0	6	alpha-numerics cyan	graphics cyan	&		6		F	V	f		v		→	↓	ö	Ö	¤	Ô
0 1 1 1	7	alpha-** numerics white	graphics white	'		7		G	W	g		w		?	↑	·	Ç	Ñ	Ú
1 0 0 0	8	flash	conceal display	(		8		H	X	h		x		‖	ö	ò	ô	ñ	æ
1 0 0 1	9	** steady	** contiguous graphics	)		9		I	Y	i		y		¾	ä	è	û	è	Æ
1 0 1 0	10	** end box	separated graphics	*		:		J	Z	j		z		÷	ü	ì	ç	à	ð
1 0 1 1	11	start box	* ESC	+		;		K	Ä	k		ä		←	Ä	°	ë	á	Đ
1 1 0 0	12	** normal height	** black background	,		<		L	Ö	l		ö		½	Ö	ç	ê	é	ø
1 1 0 1	13	double height	new background	−		=		M	Ü	m		ü		→	Å	→	ù	í	Ø
1 1 1 0	14	* SO	hold graphics	.		>		N	^	n		ß		↑	Ü	↑	î	ó	þ
1 1 1 1	15	* SI	** release graphics	/		?		O	_	o		■		#	_	#	#	ú	Þ

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* These control characters are reserved for compatibility with other data codes

** These control characters are presumed before each row begins

APPLICATION INFORMATION (continued)

Table 4b Character data input decoding, East European languages (SAA5243P/H)

BIT b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0	1	1	1	1	1	1
b_7	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	1
b_6	0	0	1	1	1	1	0	0	1	1	0	0	1	0	1	1
b_5	0	1	0	0	0	0	0	1	0	1	0	1	0	0	1	1
b_4 b_3 b_2 b_1 ↓ row / column →	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black			0		P	p		p		§	É	č	ą	Č	ű
0 0 0 1	1	alpha-numerics red	graphics red	!		1		A	Q	a		q		°	é	é	ę	č	d
0 0 1 0	2	alpha-numerics green	graphics green	"		2		B	R	b		r		ä	ä	á	ż	ć	Ď
0 0 1 1	3	alpha-numerics yellow	graphics yellow	#		3		C	S	c		s		Ő	Ű	Ę	Ą	Ź	Ł
0 1 0 0	4	alpha-numerics blue	graphics blue	¤		4		D	T	d		t		$	¤	ů	ń	½	Ľ
0 1 0 1	5	alpha-numerics magenta	graphics magenta	%		5		E	U	e		u		(€)	(▤)	Á	Ó	ö	Ł
0 1 1 0	6	alpha-numerics cyan	graphics cyan	&		6		F	V	f		v		(Đ)	(o)	É	Ó	ő	Ľ
0 1 1 1	7	alpha-** numerics white	graphics white	'		7		G	W	g		w		(?)	(Ł)	í	Ü	Ü	Ň
1 0 0 0	8	flash	conceal display	(		8		H	X	h		x		ö	ö	ě	ś	ž	ň
1 0 0 1	9	** steady	** contiguous graphics	)		9		I	Y	i		y		ü	å	ú	ł	đ	Ň
1 0 1 0	10	** end box	separated graphics	*		:		J	Z	j		z		ß	ü	š	ż	š	ŕ
1 0 1 1	11	start box	* ESC	+		;		K	Ä	k		ä		Ä	Ä	ť	Ž	Ć	Ŕ
1 1 0 0	12	** normal height	** black background	,		<		L	Ş	l		ş		Ö	Ö	ž	Ś	Ž	Ř
1 1 0 1	13	double height	new background	−		=		M	Ă	m		ă		Ü	A	ý	Ł	Đ	Ť
1 1 1 0	14	* SO	hold graphics	.		>		N	Ţ	n		ţ		^	Ü	í	ć	Š	Ý
1 1 1 1	15	* SI	** release graphics	/		?		O	ı	o				_		ř	ó	ë	Ë

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* These control characters are reserved for compatibility with other data codes

** These control characters are presumed before each row begins

Table 4c Character data input decoding, Arabic and English languages (SAA5243P/K)

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0 or 1	0	0 or 1	1	1	1	1	1
b_7	0	0	0	1	1	1	0	1	1	1	1	1	0	0	1	1	1
b_6	0	0	1	0	1	1	0	0	1	1	1	1	0	1	0	1	1
b_5	0	1	0	0	1	1	0	1	0	0	1	1	0	0	0	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black															
0 0 0 1	1	alpha-numerics red	graphics red															
0 0 1 0	2	alpha-numerics green	graphics green															
0 0 1 1	3	alpha-numerics yellow	graphics yellow															
0 1 0 0	4	alpha-numerics blue	graphics blue															
0 1 0 1	5	alpha-numerics magenta	graphics magenta															
0 1 1 0	6	alpha-numerics cyan	graphics cyan															
0 1 1 1	7	alpha-numerics** white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	steady**	contiguous graphics**															
1 0 1 0	10	end box**	separated graphics															
1 0 1 1	11	start box	TWIST															
1 1 0 0	12	normal height**	black background**															
1 1 0 1	13	double height	new background															
1 1 1 0	14	SO*	hold graphics															
1 1 1 1	15	SI*	release graphics**															

7Z22660.3

* These control characters are reserved for compatibility with other data codes

** These control characters are presumed before each row begins

APPLICATION INFORMATION (continued)

Table 4d Character data input decoding, Arabic and Hebrew languages (SAA5243P/L)

BIT b_8				0	0	0 or 1	0	0 or 1	0	0	0	0	0 or 1	0	0 or 1	1	1	1	1	1	1
	b_7			0	0	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
	b_6			0	1	0	0	1	1	0	0	1	1	1	1	0	1	0	0	1	1
	b_5			0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
b_4	b_3	b_2	b_1	column / row 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha-numerics black	graphics black															
0	0	0	1	1	alpha-numerics red	graphics red															
0	0	1	0	2	alpha-numerics green	graphics green															
0	0	1	1	3	alpha-numerics yellow	graphics yellow															
0	1	0	0	4	alpha-numerics blue	graphics blue															
0	1	0	1	5	alpha-numerics magenta	graphics magenta															
0	1	1	0	6	alpha-numerics cyan	graphics cyan															
0	1	1	1	7	alpha-numerics white **	graphics white															
1	0	0	0	8	flash	conceal display															
1	0	0	1	9	steady **	contiguous graphics **															
1	0	1	0	10	end box **	separated graphics															
1	0	1	1	11	start box	TWIST															
1	1	0	0	12	normal height **	black background **															
1	1	0	1	13	double height	new background															
1	1	1	0	14	SO *	hold graphics															
1	1	1	1	15	SI *	release graphics **															

7Z22679.2

* These control characters are reserved for compatibility with other data codes

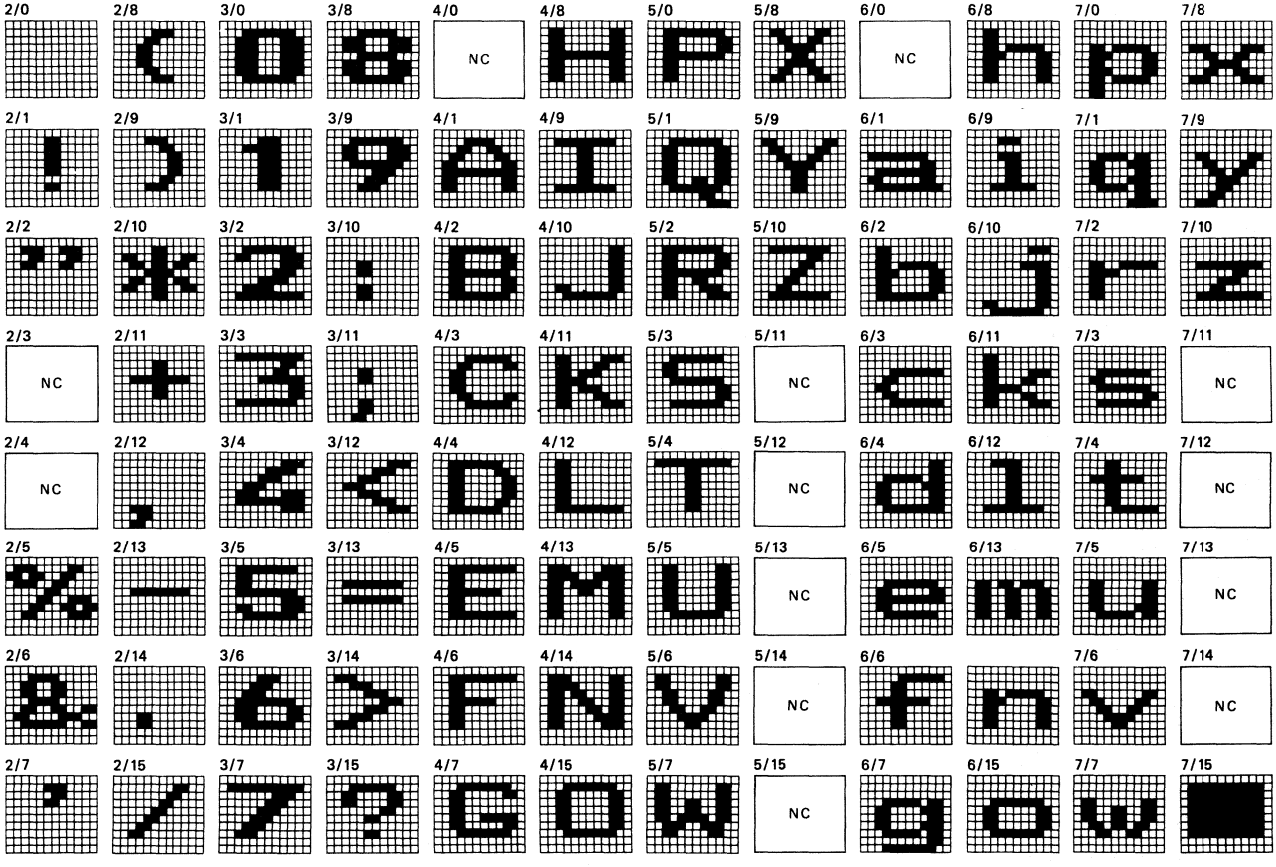
** These control characters are presumed before each row begins

Notes to Table 4

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. National option characters are shown in Table 6.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters (for /E and /H character tables only) to combine with character 8/5.
7. With bit 8 = 0 national option character will be decoded according to the setting of control bits C12 to C14 (see Table 6).

APPLICATION INFORMATION (continued)

Table 5 SAA5243 basic character matrix



Where: NC national option character position.

Table 6a SAA5243P/E/M2 national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

7Z22659.2

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

APPLICATION INFORMATION (continued)

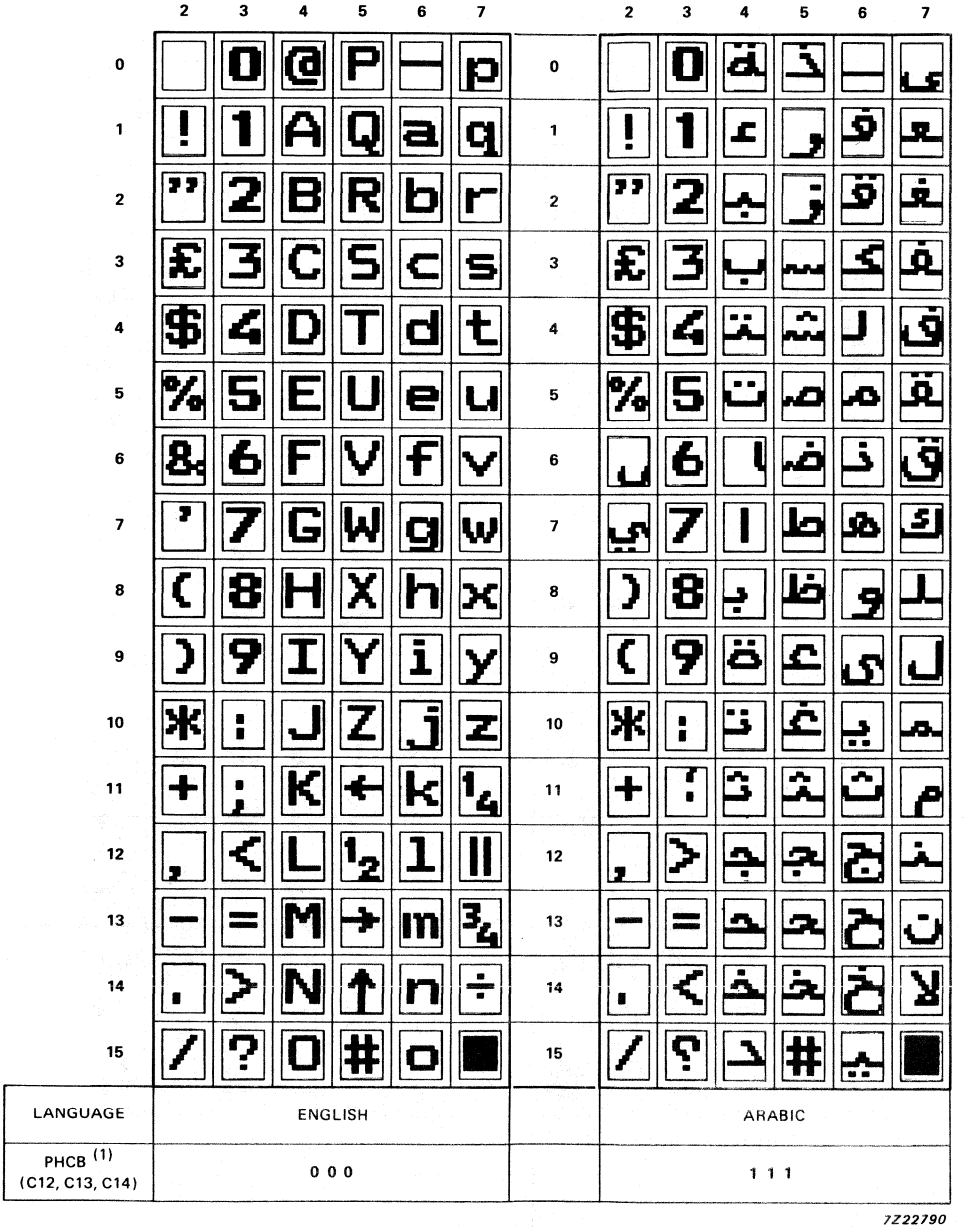
Table 6b SAA5243P/H national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
POLISH	0	0	0	#	ń	ą	Ż	ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAK	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

7Z22658.1

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

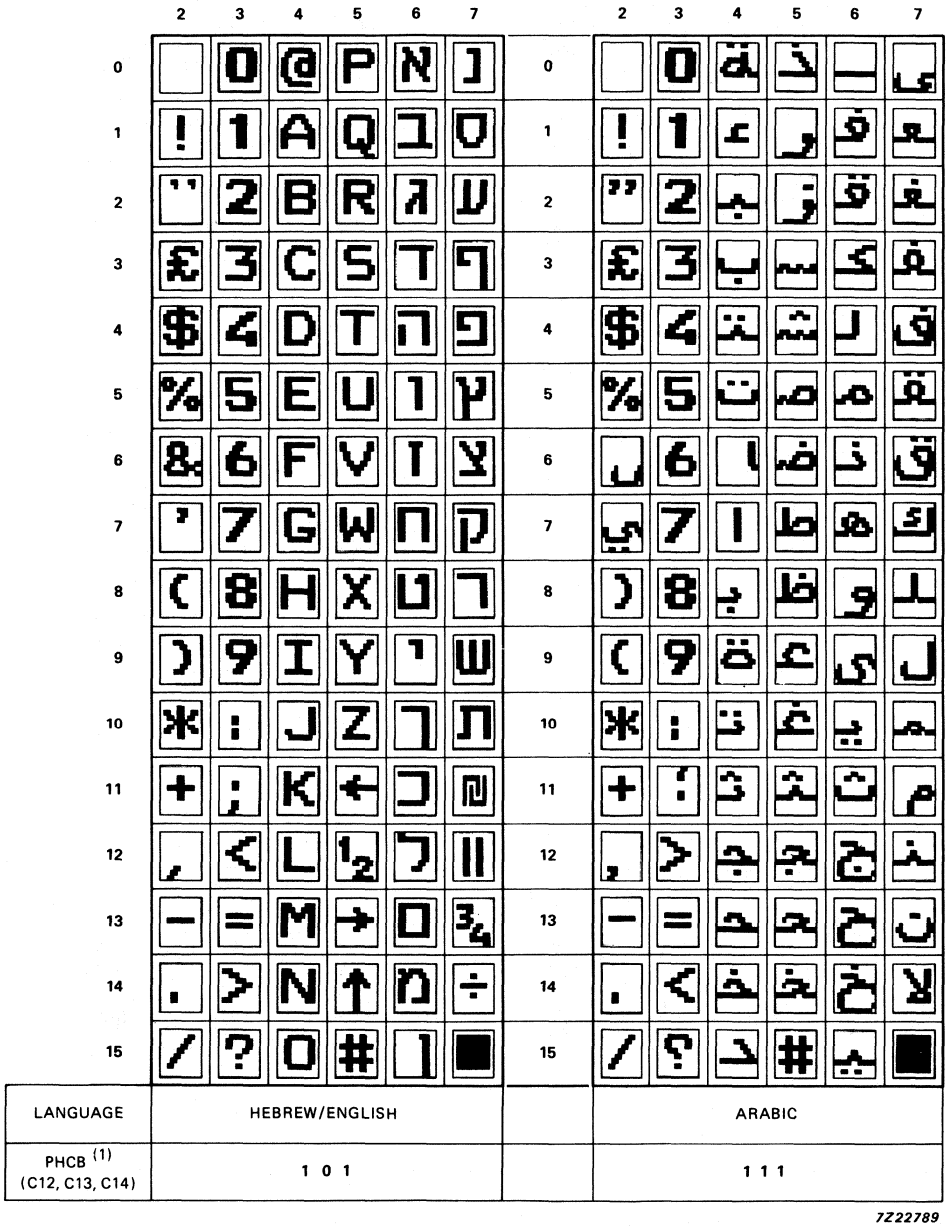
Table 6c SAA5243P/K national option character set



(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

APPLICATION INFORMATION (continued)

Table 6d SAA5243P/L national option character set



LANGUAGE	HEBREW/ENGLISH	ARABIC
PHCB (1) (C12, C13, C14)	1 0 1	1 1 1

7Z22789

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUIT

(USECCT)

GENERAL DESCRIPTION

The SAA5245 is a MOS N-channel integrated circuit which performs all the digital logic functions of a 525-line World System Teletext decoder. It operates in conjunction with the teletext video processor SAA5231, standard static RAMs and is controlled via the 2-wire I²C-bus The device can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 8 character matrix
- Field flyback (lines 5 to 19), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language selection of up to seven different languages
- 25th display row for software generated status messages
- Automatic processing of gearing function
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C-bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- Odd/even field output for de-interlaced displays

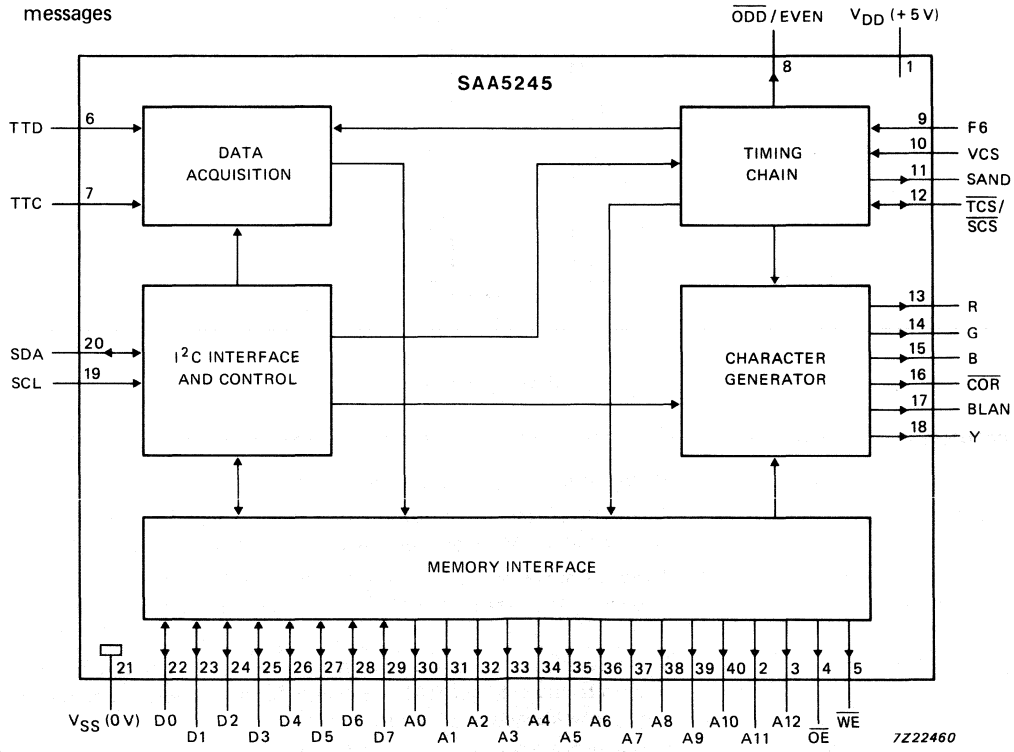


Fig. 1 Block diagram.

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

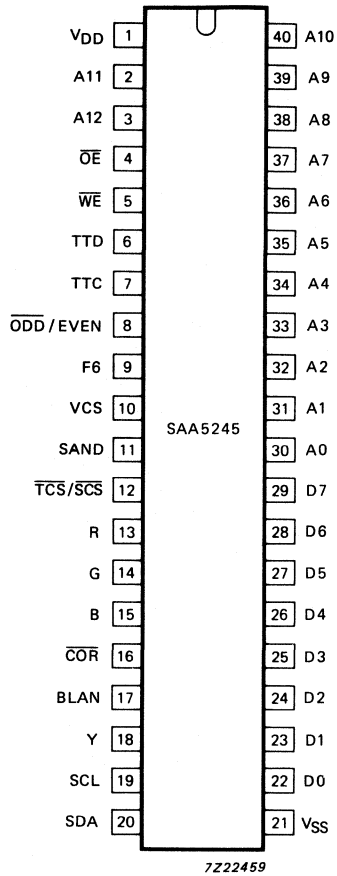


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.
5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct DC level following the external AC coupling.

7	TTC	**Teletext Clock**: 5.727 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
8	$\overline{\text{ODD}}$/EVEN	**$\overline{\text{Odd}}$/Even:** for interlaced mode, the output changes once per field at 2 μs before the end of line 1 (263). The output is high for even fields and low for odd fields.
9	F6	**Character display clock**: 6.042 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync:** input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{\text{TCS}}/\overline{\text{SCS}}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig. 6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue:** these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{\text{COR}}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C-bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C-bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	D0-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 1)	V_{DD}	−0.3	+ 7.5	V
Input voltage range				
VCS, SDA, SCL, D0 - D7	V_I	−0.3	+ 7.5	V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$	V_I	−0.3	+ 10.0	V
Output voltage range				
SAND, A0 - A12, $\overline{OE}$, $\overline{WE}$, D0 - D7, SDA, $\overline{ODD}$/EVEN R, G, B, BLAN, $\overline{COR}$, Y	V_O	−0.3	+ 7.5	V
$\overline{TCS}/\overline{SCS}$	V_O	−0.3	+ 10.0	V
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	+ 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.0	–	7.0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
DC input voltage range	V_I	−0.3	–	+ 10.0	V
AC input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1.0	–	7.0	V
AC input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1.5	–	7.0	V
Input peaks relative to 50% duty cycle	± V_P	0.2	–	3.5	V
TTC clock frequency	f_{TTC}	–	5.727	–	MHz
F6 clock frequency	f_{F6}	–	6.042	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
at I_{OH} = 0.1 mA	V_{OH}	2.4	–	6.0	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time between 3.0 V and 1.0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5.5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0.2 mA	V_{OL}	0	–	0.25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1.1	–	3.1	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 0.9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3.3 V and 3.8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3.8 V and 0.4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1.0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6.0	V
Output fall time with a load resistor of 1.2 kΩ to 6 V and measured between 5.5 V and 1.5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1.2 kΩ to 6 V and measured on the falling edges at 3.5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C-bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	495	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	495	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns
QUALITY (note 13)					
Failure rate					
Failure rate at T_{amb} = 55 °C (1×10^{-6} failures per hour)		–	–	1000	FITS

DEVELOPMENT DATA

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig. 3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2.0 V; data stable 0 $\leqslant$ 0.8 V (see Fig. 4).
5. The TTC and F6 inputs have internal clamping diodes and are AC coupled (see Fig. 3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C-bus timing see Fig. 8.
8. For details of RAM timing see Fig. 9.
9. For details of synchronization timing see Fig. 5.
10. For details of display output timing see Fig. 7.
11. The I^2C-bus timings are referred to V_{IH} = 3 V and V_{IL} = 1.5 V. For waveforms see Fig. 8.
12. The memory interface timings are referred to V_{IL} = 1.5 V. For waveforms see Fig. 9.
13. This device shall meet the requirements of the Elcoma General Quality and Specification for ICs: URV - 4 - 2 - 59/601 (LSI).

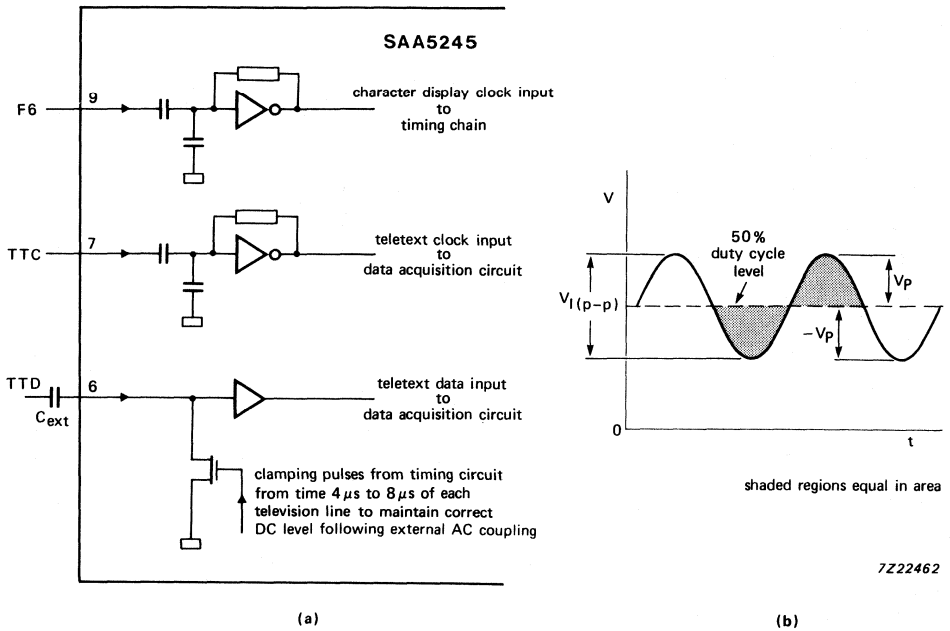
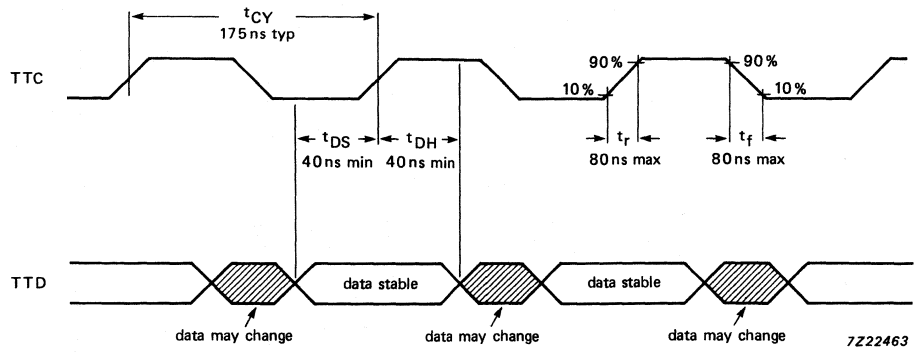


Fig. 3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2.0 V; 0 is $\leqslant$ 0.8 V.

Fig. 4 Teletext data input timing.

DEVELOPMENT DATA

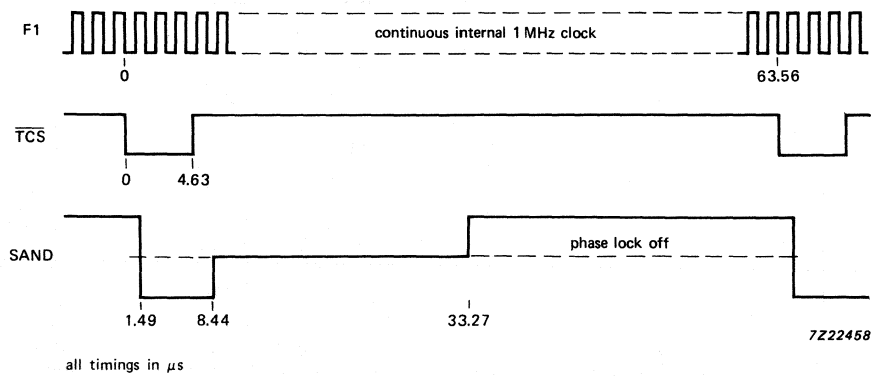


Fig. 5 Synchronization timing.

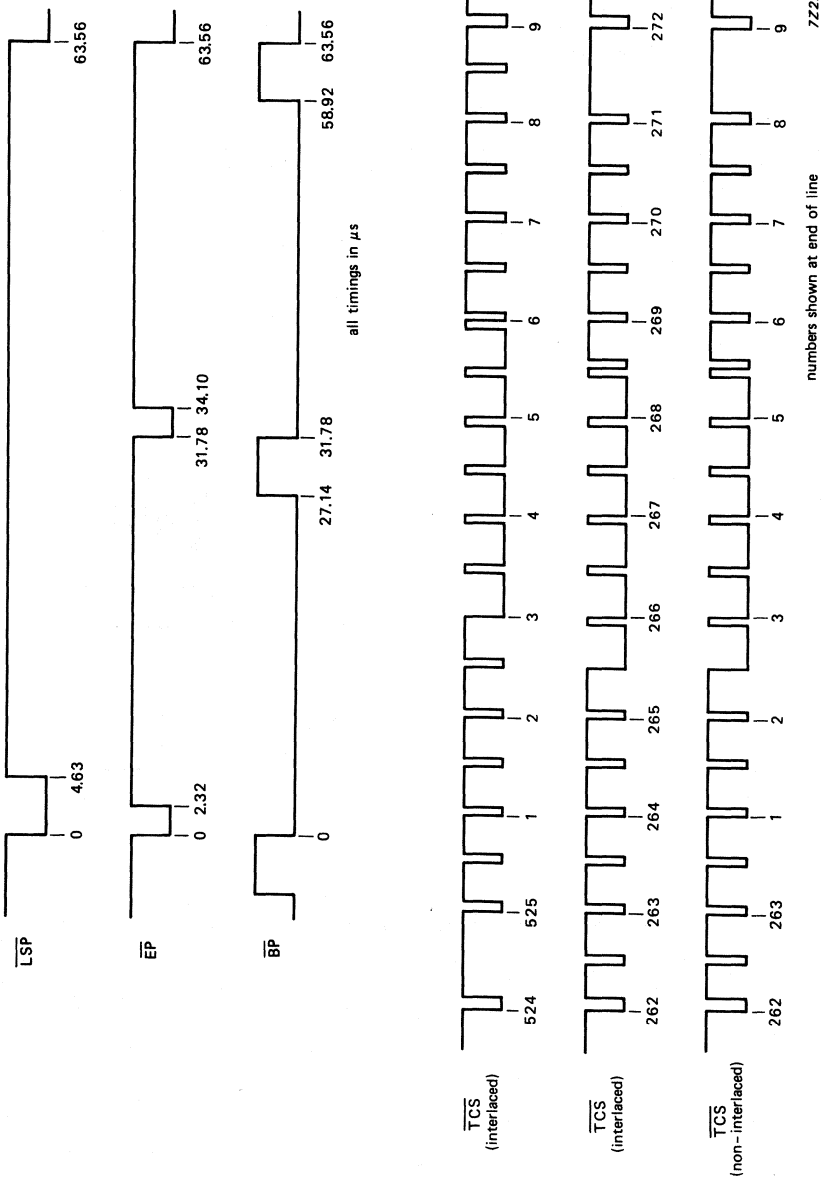


Fig. 6 Composite sync waveforms (525-line version).

Line sync pulses ($\overline{\text{LSP}}$), equalizing pulses ($\overline{\text{EP}}$) and broad pulses ($\overline{\text{BP}}$) are combined to provide the text composite sync waveform ($\overline{\text{TCS}}$) as shown. All timings measured from falling edge of $\overline{\text{LSP}}$ with a tolerance of ± 100 ns.

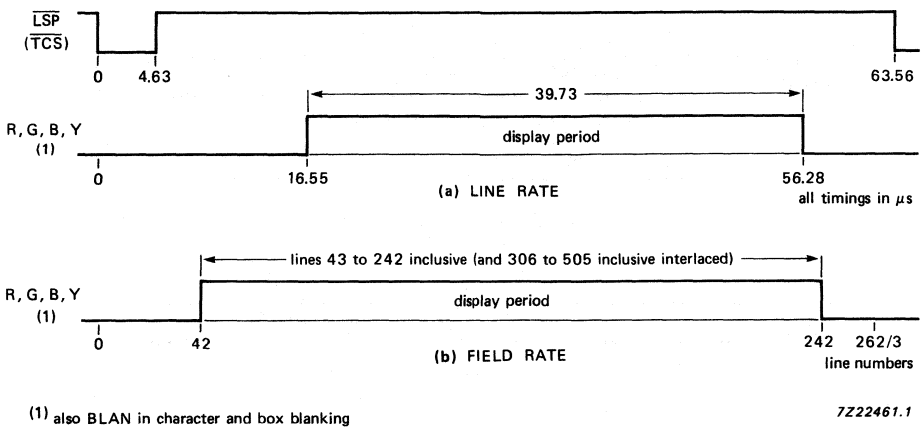


Fig. 7 Display output timing (a) line rate (b) field rate.

DEVELOPMENT DATA

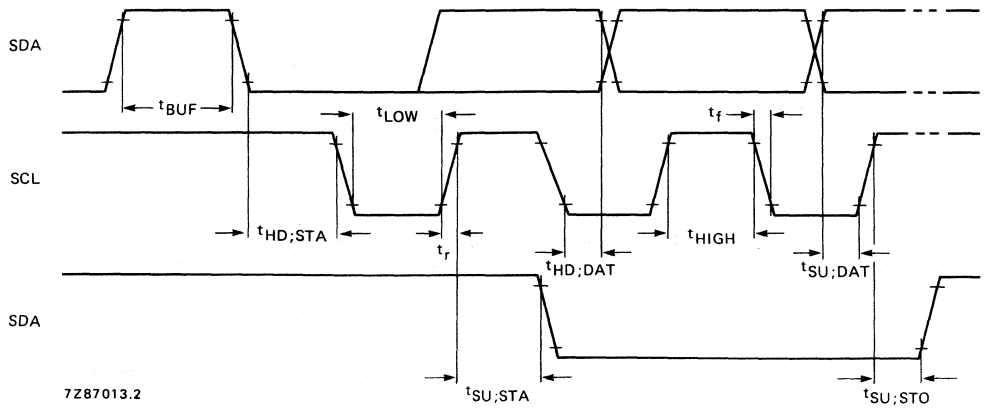


Fig. 8 I²C-bus timing.

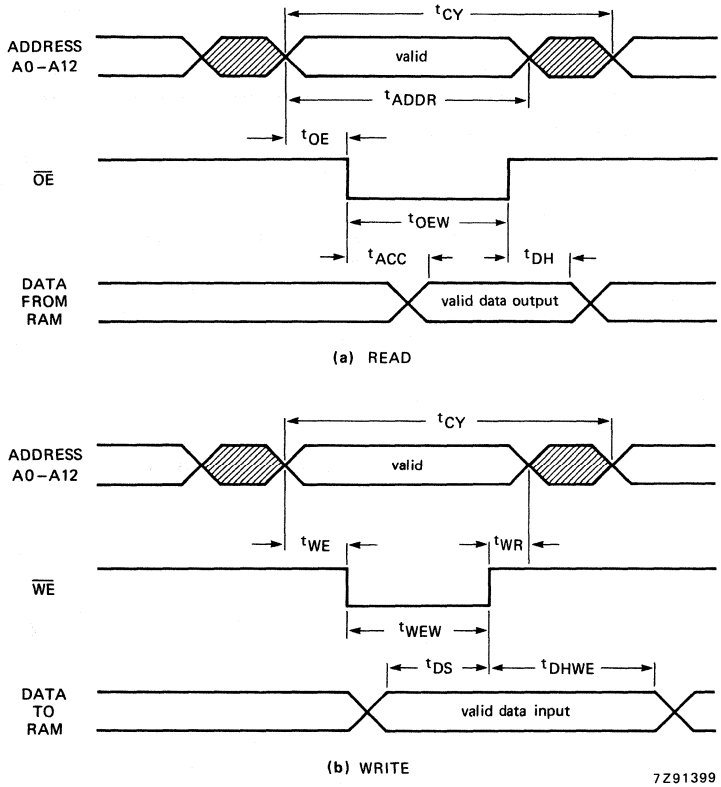


Fig. 9 Memory interface timing (a) read (b) write.

DEVELOPMENT DATA

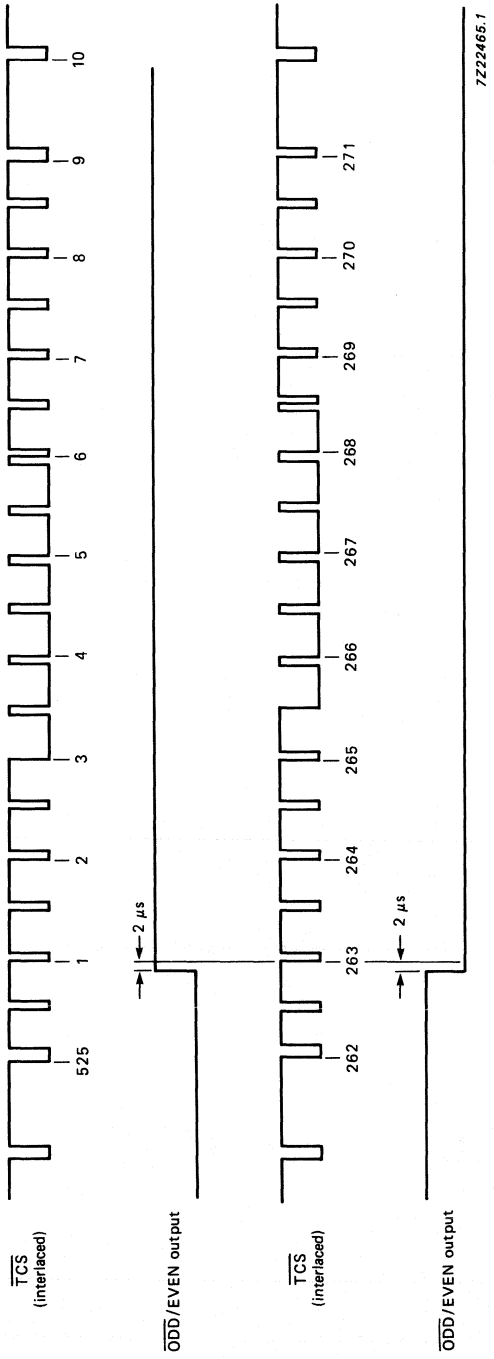


Fig. 10 ODD/EVEN timing diagram.

APPLICATION INFORMATION

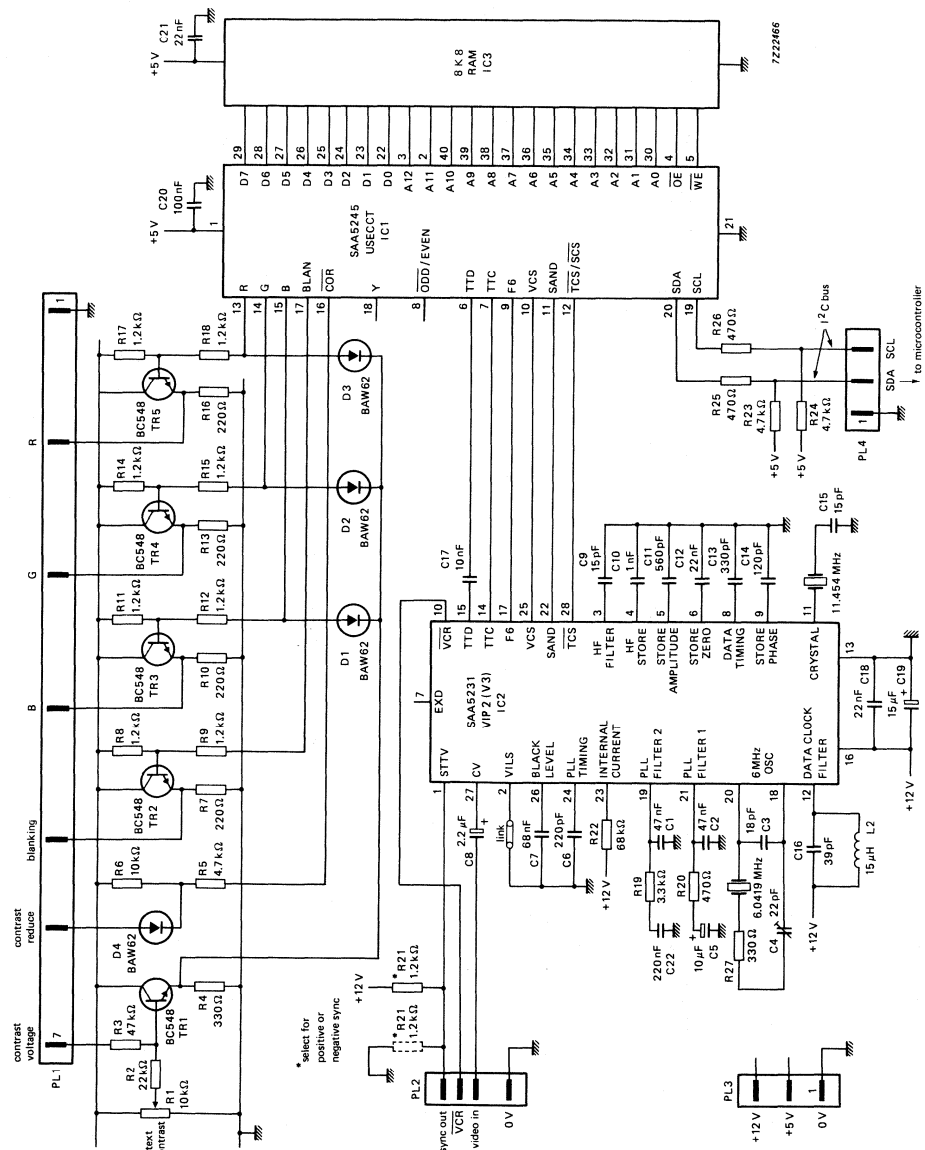


Fig. 11 USECCT based multi-page decoder circuit diagram.

DEVELOPMENT DATA

USECCT page memory organization

The organization of a page memory is shown in Fig. 12. The USECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF USECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

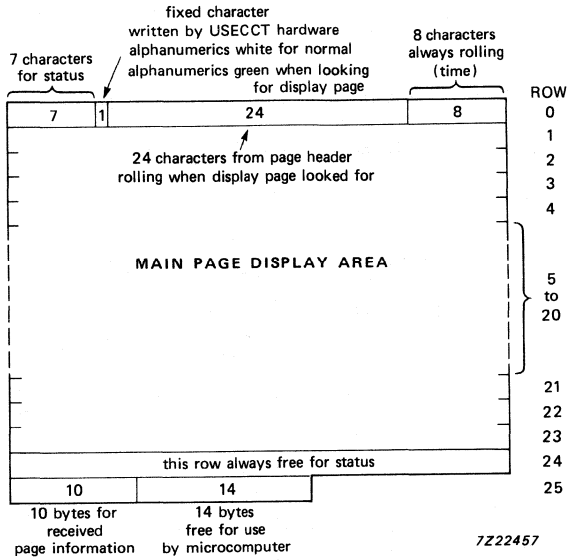


Fig. 12 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	0	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
PBLF	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

APPLICATION INFORMATION (continued)

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by USECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

USECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 USECCT register map

		D7	D6	D5	D4	D3	D2	D1	D0
Operating mode	R1	TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0
Page request address	R2	–	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	R3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	R4	–	–	–	–	–	A2	A1	A0
Display control (normal)	R5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash/subtitle)	R6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	R7	STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	R8	–	–	–	–	CLEAR MEM.	A2	A1	A0
Active row	R9	–	–	–	R4	R3	R2	R1	R0
Active column	R10	–	–	C5	C4	C3	C2	C1	C0
Active data	R11	D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)

–bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

Where:

R1 Mode	
T0, T1	interlace/non-interlace 262/263 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode	
BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C-bus

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	X	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for D0 CARE bits.
When the D0 CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the D0 CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

CHARACTER SETS

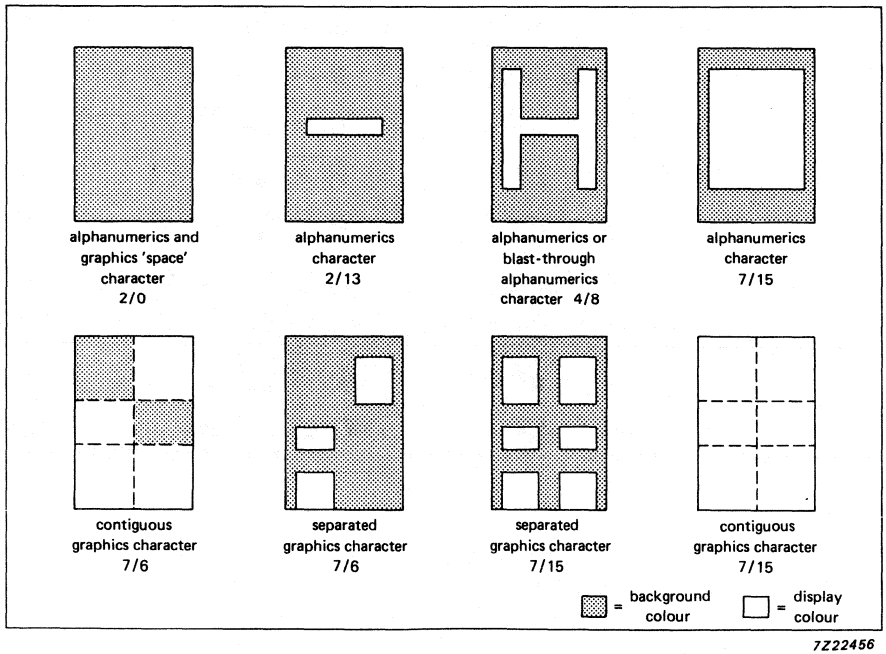
The US teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14 as shown in Table 4.
USECCT automatically decodes transmission bits C12 to C14. Other combinations of C12 to C14 are defaulted to English in SAA5245P/A. With 8-bit decoding the character matrices are shown in Table 5.

Table 4 Selection of national character sets (SAA5245P/A)

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH	SPANISH
C12	0	0	0	0	1	1
C13	0	0	1	1	0	0
C14	0	1	0	1	0	1

Where:

PHCB page header control bits.



Character bytes are listed as transmitted from b_1 to b_7.

Fig. 13 Character format.

APPLICATION INFORMATION (continued)

Table 5 Character data input decoding (SAA5245A).

BITS b_8	0	0	0 or 1	0 or 1	0	0	0	0	1	1	1	1	1	1
b_7	0	0	0	0	1	1	1	1	0	0	1	1	1	1
b_6	0	0	1	1	0	0	1	1	0	0	1	1	1	1
b_5	0	1	0	1	0	1	0	1	0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓ row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha–numerics black	graphics black															
0 0 0 1	1	alpha–numerics red	graphics red															
0 0 1 0	2	alpha–numerics green	graphics green															
0 0 1 1	3	alpha–numerics yellow	graphics yellow															
0 1 0 0	4	alpha–numerics blue	graphics blue															
0 1 0 1	5	alpha–numerics magenta	graphics magenta															
0 1 1 0	6	alpha–numerics cyan	graphics cyan															
0 1 1 1	7	alpha–numerics white **	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	steady **	contiguous graphics **															
1 0 1 0	10	end box **	separated graphics															
1 0 1 1	11	start box	ESC *															
1 1 0 0	12	normal height **	black back–ground **															
1 1 0 1	13	double height	new back–ground															
1 1 1 0	14	SO *	hold graphics															
1 1 1 1	15	SI *	release graphics **															

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Notes to Table 5

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters to combine with character 8/5.
6. With bit 8 = 0 national option characters will be decoded according to the setting of control bits C12 to C14 (see Table 4).

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins.

TELETEXT IC FOR ANALOGUE AND DIGITAL TV

GENERAL DESCRIPTION

The SAA9041 is a CMOS integrated circuit designed for reception, decoding and display of 625 and 525 line World System Teletext (WST).

It is used in conjunction with a teletext video processor (SAA5231 or SAA5236) for data regeneration, and a single-chip 64 K x 4-bit or 256 K x 4-bit dynamic RAM page memory.

The SAA9041 acquires teletext packets defined at levels 1, 2 and 3 in the WSTspecification and produces a level 1 display.

The device is μC controlled via the standard I^2C-bus and is compatible with the Philips digital TV chip-set.

Features

General

- Interfaces with the Philips digital TV chip-set
- Interfaces with analogue TV
- Directly interfaces up to 1 Mbit dynamic RAM
- Fully independent acquisition and display timing
- 3 display modes
  - normal
  - 32 kHz (progressive scan)
  - 100 Hz/120 Hz (field doubling)
- I^2C controlled
- Single 5 V power supply

Acquisition

- Simultaneous update of up to 8 pages
- Up to 100 page background memory capability
- Software selectable 625/525 line operation
- Full Level One Features (FLOF) operation
- VBI and full channel operation
- Extension packets 26/27/28/29 and 30 fully decoded

Display

- Stable display by slaving from scan-related timing signals
- Automatic selection of up to seven different languages
- Storage of 192 characters (12 x 10 dot matrix)
- Software controlled RGB level removes the need for hardware adjustment
- Up to 27 display rows; 0 to 24 and up to 2 status rows

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

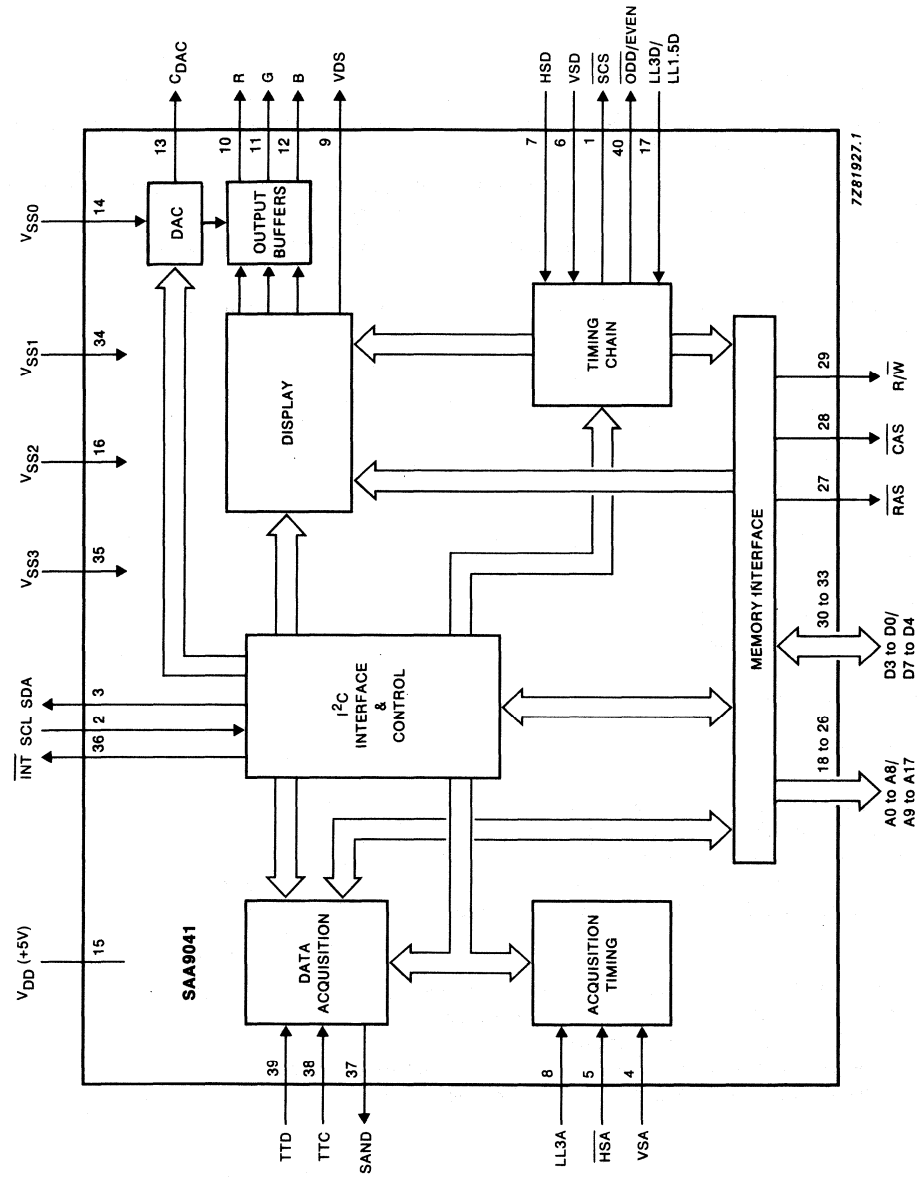


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

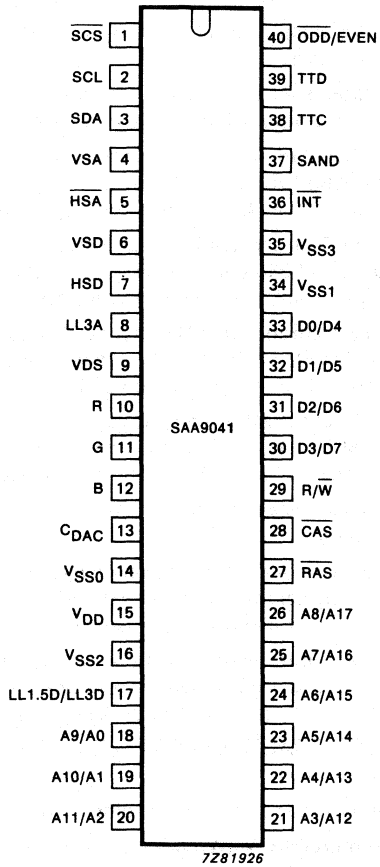


Fig. 2 Pinning diagram

Pin functions

pin no.	mnemonic	description
1	$\overline{SCS}$	**Scan Composite Sync:** active LOW output containing line and field information related to the timing of the display section. It is used to slave an external display device such as the SAA5350 (EUROM).
2	SCL	**Serial Clock:** input signal which is the I^2C-bus clock from the microcontroller.
3	SDA	**Serial Data:** is the I^2C-bus data line connected to the microcontroller. It is an input/output function with an open-drain output.
4	VSA	**Vertical Synchronization Acquisition:** vertical synchronization signal from the SAA9050 (VS), derived from the incoming video. This input enables field timing to be established in the acquisition section.
5	$\overline{HSA}$	**Horizontal Synchronization Acquisition:** horizontal synchronization signal from the SAA9050 (HSY), derived from the incoming video. This active LOW input enables line timing to be established in the acquisition section.
6	VSD	**Vertical Synchronization Display:** vertical synchronization signal from the SAA9050 (VS), which indicates the vertical position of the TV picture. This input follows field synchronization of the display section.
7	HSD	**Horizontal Synchronization Display:** horizontal synchronization signal from the SAA9050 (HS). This input enables the display section to be synchronized to line timing of the TV picure.
8	LL3A	**Line-Locked system clock:** 13.5 MHz system clock input for the acquisition section.
9	VDS	**Video/Data Switch:** push-pull active HIGH 3-state output which controls the switching between text (HIGH) and normal TV (LOW) picture for both normal text and superimposed displays.
10	R	**Red, Green, Blue:** analogue 3-state outputs which contain video character and background information for text display. The output level is adjustable over 16 steps and is controlled by V_{SS0}, V_{DD} and an internal register.
11	G	
12	B	
13	C_{DAC}	**DAC output:** DAC output level external decoupling capacitor not less than 1 μF.
14	V_{SS0}	**Ground:** ground connection for video outputs.
15	V_{DD}	**Power Supply:** + 5 V (typ.).
16	V_{SS2}	**Ground:** ground connection.
17	LL3D/ LL1.5D	**Line-Locked system clock:** 13.5 MHz or 27 MHz system clock input for the display, memory interface and control sections.
18 to 26	A0 to A8/ A9 to A17	**Address:** multiplexed address outputs for the external nibble-wide dynamic RAM (DRAM). With a 256-Kbit (16 K x 4) DRAM the address A8 pin is not used.
27	$\overline{RAS}$	**Row Address Strobe:** active LOW output for the external DRAM.
28	$\overline{CAS}$	**Column Address Strobe:** active LOW output for the external DRAM.
29	R/$\overline{W}$	**Read/Write:** input/output enable signal for the external DRAM.

pin no.	mnemonic	description
30 to 33	D3 to D0/ D4 to D7	**Data:** data inputs/outputs to and from the external nibble-wide DRAM.
34	V_{SS1}	**Ground:** ground connection.
35	V_{SS3}	**Ground:** ground connection.
36	$\overline{INT}$	**Interrupt:** open-drain active LOW output which provides an interrupt signal for a microprocessor indicating the arrival of a page in any one of the acquisition channels.
37	SAND	**Sandcastle:** 3-level output for the SAA5231 or SAA5236 representing the $\overline{PL}/\overline{CBB}$ signal.
38	TTC	**Teletext Clock:** input from the SAA5231 or SAA5236 supplied via an external coupling capacitor.
39	TTD	**Teletext Data:** input from the SAA5231 or SAA5236 supplied via an external coupling capacitor with pin 39 clamped to V_{SS} for 4 to 8 μs of each line to maintain the correct DC level.
40	$\overline{ODD}$/EVEN	**Odd/Even:** output for de-interlacing circuits. The signal is LOW for odd fields and HIGH for even fields when text but no picture is displayed. It is forced LOW when a TV picture is present.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.5	+ 6.5	V
DC input voltage	V_I	−0.5	V_{DD} + 0.5	V
DC input current	I_I	−20	+ 20	mA
DC output voltage	V_O	−0.5	V_{DD} + 0.5	V
DC output current	I_O	−20	+ 20	mA
DC V_{DD} current	I_{DD}	*	*	mA
Storage temperature range	T_{stg}	−55	+ 125	°C
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Electrostatic handling**	V_{es}	−1000	+ 1000	V

Notes to the ratings

1. All voltages are with respect to V_{SS}.
2. V_{SSO} is considered as an output.

* Value to be fixed.

** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a rise time of 15 ns.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	note 1	V_{DD}	4.5	5.0	5.5	V
Supply current		I_{DD}	–	*	–	mA
Inputs	note 2					
TTD	note 3					
Input voltage						
(peak-to-peak value)		$V_{I(p-p)}$	2.0	–	5.0	V
External coupling capacitor		C_{ext}	–	–	50	nF
Input rise and fall times	note 4	t_r, t_f	10	–	80	ns
Input data set-up time	note 5	$t_{SU;DAT}$	40	–	–	ns
Input data hold time	note 5	$t_{HD;DAT}$	40	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	7	–	pF
Clamp start time	note 6	t_{CLon}	3.5	4.0	4.5	μs
Clamp finish time	note 6	t_{CLoff}	7.5	8.0	8.5	μs
Clamp output current	note 7	I_{clamp}	1.0	–	–	mA
TTC	note 8					
Input voltage						
(peak-to-peak value)		$V_{I(p-p)}$	2.0	–	5.0	V
External coupling capacitor		C_{ext}	–	10	–	nF
Peak input current		I_{IM}	−10	–	+ 10	mA
Input peaks relative to 50% duty factor		$\pm V_{IM}$	0.2	–	3.5	V
Input rise and fall times	note 4	t_r, t_f	10	–	80	ns
Input capacitance		C_I	–	7	–	pF
Input impedance	$V_I = V_{SS}$	$\lvert Z_I \rvert$	–	*	–	Ω
Input impedance	$V_I = V_{DD}$	$\lvert Z_I \rvert$	–	*	–	Ω
Clock frequency						
625 line		f_{TTC}	–	6.9375	–	MHz
525 line		f_{TTC}	–	5.7272	–	MHz

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (continued)	note 2					
$\overline{HSA}$	note 9					
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	note 4	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	7	pF
VSA						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	note 4	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	7	pF
LL3A (TTL mode)						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
LL3A cycle time	note 10	t_{CA}	69	74	80	ns
LL3A HIGH time		t_{CAH}	30	–	–	ns
LL3A LOW time		t_{CAL}	30	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−100	–	+ 100	μA
Input capacitance		C_I	–	–	10	pF
LL3A (AC mode)	13.5 MHz					
Mean voltage level	note 24	V_{ACM}	−12	–	+ 12	V
AC voltage (peak-to-peak value)		$V_{AC(p-p)}$	1.0	–	3.0	V
Voltage HIGH w.r.t. mean		V_{ACH}	0.3	–	2.0	V
Voltage LOW w.r.t. mean		V_{ACL}	−2.0	–	−0.3	V
HIGH time w.r.t. mean		t_{ACH}	30	–	–	ns
LOW time w.r.t. mean		t_{ACL}	30	–	–	ns
Series capacitor		C_S	47	100	220	pF
Input impedance	note 24	Z_{ACI}	10	–	–	kΩ
SCL						
Input voltage LOW		V_{IL}	0	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD}	V
Input rise time	note 4	t_r	–	–	1	μs
Input fall time	note 11	t_f	–	–	300	ns
Input leakage current	note 12; V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance		C_I	–	–	7	pF
SCL clock frequency		f_{SCL}	0	–	100	kHz
HSD						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	note 4	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	7	pF
VSD						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	note 4	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	7	pF
LL3D (TTL mode)						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
LL3D cycle time	note 10					
13.5 MHz		t_{CA}	69	74	80	ns
27.0 MHz		t_{CA}	35	37	40	ns
LL3D HIGH time						
13.5 MHz		t_{CAH}	30	–	–	ns
27.0 MHz		t_{CAH}	15	–	–	ns
LL3D LOW time						
13.5 MHz		t_{CAL}	30	–	–	ns
27.0 MHz		t_{CAL}	15	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−100	–	+ 100	μA
Input capacitance		C_I	–	–	10	pF
LL3D (AC mode)						
Mean voltage level	note 24	V_{ACM}	−12	–	+12	V
AC voltage						
(peak-to-peak value)		$V_{AC(p-p)}$	1.0	–	3.0	V
Voltage High w.r.t. mean		V_{ACH}	0.3	–	2.0	V
Voltage LOW w.r.t. mean		V_{ACL}	−2.0	–	−0.3	V
HIGH time w.r.t. mean		t_{ACH}	30	–	–	ns
LOW time w.r.t. mean		t_{ACL}	30	–	–	ns
Series capacitor		C_S	47	100	220	pF
Input impedance	note 24	Z_{ACI}	10	–	–	kΩ
Inputs/Outputs (I/O)	note 13					
SDA (open drain I/O)						
Input voltage LOW		V_{IL}	0	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD}	V

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
SDA (open drain I/O) (continued)						
Input rise time	note 4	t_r	–	–	1	μs
Input fall time	note 11	t_f	–	–	300	ns
Input leakage current	note 12; V_I = 0 to V_{DD}; (with output off)	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	0	–	0.4	V
Output fall time	note 11	t_f	–	–	300	ns
Load capacitance		C_L	–	–	400	pF
D3 to D0						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input leakage current	note 12; V_I = 0 to V_{DD}; (with output off)	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	2.4	–	V_{DD}	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V		t_r, t_f				ns
Load capacitance	note 21	C_L	–	–	100	pF
Outputs	note 13					
SAND	note 22					
Output voltage LOW	I_{OL} = 0.2 mA	V_{OL}	0	–	0.3	V
Output voltage INTERMEDIATE	± I_{OI} = 30 μA	V_{OI}	1.3	–	2.7	V
Output voltage HIGH	I_{OH} = 0 to −10 μA	V_{OH}	4.2	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 1.1 V		t_r, t_f	–	–	400	ns
Output rise time V_{OL} to V_{OH} between 2.9 V and 4.0 V		t_r, t_f	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 4.0 V and 0.4 V		t_r, t_f	–	–	50	ns
Load capacitance		C_L	–	–	30	pF

parameter	conditions	symbol	min.	typ.	max	unit
$\overline{INT}$ (open-drain output)						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Pull-up voltage		V_{PU}	–	–	V_{DD}	V
Output leakage current	output off; V_{PU} = 0 to V_{DD}		−10	–	+ 10	μA
Output fall time	note 15	t_f	–	–	50	ns
Load capacitance		C_L	–	–	100	pF
A0 to A8						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V		t_r, t_f				ns
Load capacitance	note 23	C_L	–	–	100	pF
$\overline{RAS}$, $\overline{CAS}$, R/$\overline{W}$						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V		t_r, t_f				ns
Load capacitance	note 23	C_L	–	–	100	pF
$\overline{SCS}$, $\overline{ODD}$/EVEN						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times	note 16	t_r, t_f	–	–	200	ns
Load capacitance		C_L	–	–	200	pF
R, G, B (3-state)						
V_{SS0} voltage level		V_{SS0}	V_{SS}−0.5	–	V_{SS} + 0.5	V
Output voltage LOW	note 17; I_{OL} = 2.0 mA	V_{OL}	V_{SS0}	–	V_{SS0}+0.2	V
Output voltage HIGH	note 18; I_{OH} = −2 mA	V_{OH}	–	*	–	V
Output rise and fall times between 0.6 V and 1.8 V	notes 4 and 17	t_r, t_f				ns
Skew delay between output rise and fall times	notes 17 and 19	t_d				ns
Load capacitance		C_L	–	–	30	pF
Output capacitance	OFF state	C_{off}				pF
Output leakage current	OFF state; V_I = 0 to V_{DD}	I_{off}	−10	–	+ 10	μA
VDS (3-state)						
Output voltage LOW	I_{OL} = 1.0 mA	V_{OL}	0	–	0.2	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	1.1	–	2.8	V
Output rise and fall times		t_r, t_f				ns
Load capacitance		C_L	–	–	30	pF

* Adjustable over 0.5 to 1.5 V.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
TIMING						
I²C-bus	note 20					
SCL clock frequency		f_{SCL}	0	–	100	kHz
Input clock period						
HIGH time		t_{HIGH}	4	–	–	μs
LOW time		t_{LOW}	4	–	–	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop set-up time from clock HIGH		$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop		t_{BUF}	4	–	–	μs
Start hold time		$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock LOW-to-HIGH transition		$t_{SU;STA}$	4	–	–	μs
Memory interface	note 14					
Cycle time		t_{CY}	–	481	–	ns
Transition time		t_T	–	–	10	ns
$\overline{RAS}$ pulse width		$t_{W;RAS}$	120	–	–	ns
$\overline{RAS}$ pre-charge time		$t_{PC;RAS}$	90	–	–	ns
$\overline{CAS}$ hold time		$t_{HD;CAS}$	120	–	–	ns
Page mode cycle time		$t_{CY;PM}$	120	–	–	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time		t_d	25	–	–	ns
$\overline{CAS}$ pulse width		$t_{W;CAS}$	60	–	–	ns
$\overline{CAS}$ pre-charge time		$t_{PC;CAS}$	50	–	–	ns
Row address set-up time		$t_{SU;ROW}$	0	–	–	ns
Row address hold time		$t_{HD;ROW}$	15	–	–	ns
Column address set-up time		$t_{SU;COL}$	0	–	–	ns
Column address hold time		$t_{HD;COL}$	20	–	–	ns
Read command set-up time		$t_{SU;RD}$	0	–	–	ns
Read command hold time referenced to $\overline{CAS}$		$t_{HD;RDC}$	0	–	–	ns
Read command hold time referenced to $\overline{RAS}$		$t_{HD;RDR}$	10	–	–	ns
Access time from $\overline{CAS}$		$t_{ACC;CAS}$	–	–	60	ns

parameter	conditions	symbol	min.	typ.	max.	unit
Output buffer turn-off delay referenced to $\overline{CAS}$		t_{off}	–	–	30	ns
Write command pulse width		$t_{W;WR}$	50	–	–	ns
Write command hold time		$t_{HD;WR}$	40	–	–	ns
Data-in set-up time		$t_{SU;DATI}$	0	–	–	ns
Data-in hold time		$t_{HD;DATI}$	40	–	–	ns
Access time from $\overline{RAS}$		$t_{ACC;RAS}$	–	–	120	ns
$\overline{RAS}$ hold time after $\overline{CAS}$		$t_{HD;RC}$	60	–	–	ns
$\overline{CAS}$ to $\overline{RAS}$ pre-charge time		$t_{PC;CR}$	10	–	–	ns
Column address hold time referenced to $\overline{RAS}$		$t_{HD;COLR}$	80	–	–	ns
Data-in hold time referenced to $\overline{RAS}$		$t_{HD;DATIR}$	0	–	–	ns
RAS pre-charge to $\overline{CAS}$ hold time		$t_{PC;RCH}$	0	–	–	ns

DEVELOPMENT DATA

Notes to the characteristics

1. The rise time of V_{DD} from 0 to 4.5 V must be >150 ns to ensure that the internal power-on-reset triggers. For this circuit to reset the chip, V_{DD} must be initially <1.0 V or fall to <1.0 V for at least 100 ns. Spikes on V_{DD} are tolerable provided that V_{DD} is not reduced to <2.5 V.
2. All inputs are protected against static charge under normal handling.
3. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor.
4. Rise and fall times are measured between 10% and 90% levels.
5. Teletext input data set-up and hold times are measured with respect to 50% duty factor level of the rising edge of the teletext clock input (TTC). Data stable $1 \geqslant 2.0$ V, data stable $0 \leqslant 0.8$ V.
6. Clamp times measured from the line sync reference point.
7. Clamp transistor on, V_{TTD} to $V_{SS} = 0.1$ V.
8. The TTC input has an internal clamping diode.
9. HSA is falling edge triggered.
10. Minimum and maximum cycles times are $\pm$ 7.1% of the typical value.
11. Fall time is measured between 3.0 V and 1.5 V.
12. Applies even when $V_{DD} = 0$ V.
13. All input/outputs and outputs are protected against static charge under normal handling.
14. For details of memory interface timings to and from external DRAM see Fig. 5 and Fig. 6.

Notes to the characteristics (continued)

15. Output fall time measured between 4.0 V and 1.0 V levels with a 3.3 kΩ load to 5.0 V.
16. Output rise and fall times measured between 0.8 V and 2.0 V levels.
17. Measured with $V_{SS0} = V_{SS}$ and output voltage (C_{DAC}) = 1.5 V.
18. Measured with $V_{SS0} = V_{SS}$ and output voltage (C_{DAC}) = 0.5 V to 1.5 V.
19. Skew delay time measured at 0.7 V levels.
20. For details of I²C-bus timings see Fig. 3; timings are referred to V_{IH} = 3.0 V and V_{IL} = 1.5 V.
21. Load capacitance measured with two DRAM data inputs; 50 pF maximum.
22. A current of 1 μA flows out of the SAA5231 or SAA5236 while its output is in the range of 1 V to 3.5 V.
23. Load capacitance measured with eight DRAM data inputs; 80 pF maximum.
24. Measured through a 200 pF capacitor with a 13.5 MHz sinewave.

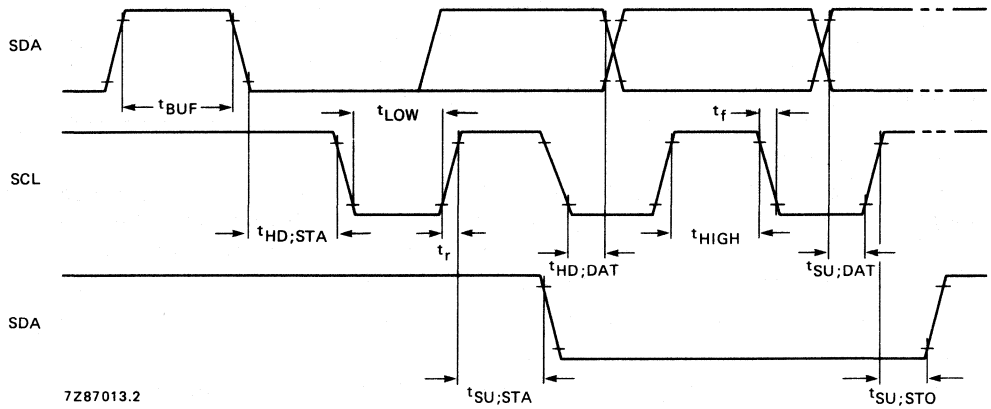


Fig. 3 I²C-bus timing.

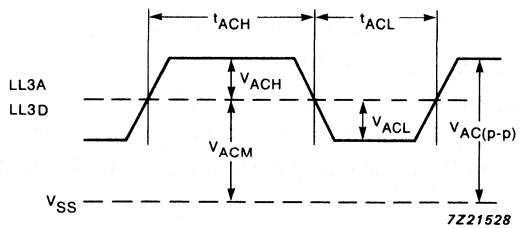


Fig. 4 Line-Locked system clock LL3A and LL3D timing diagram.

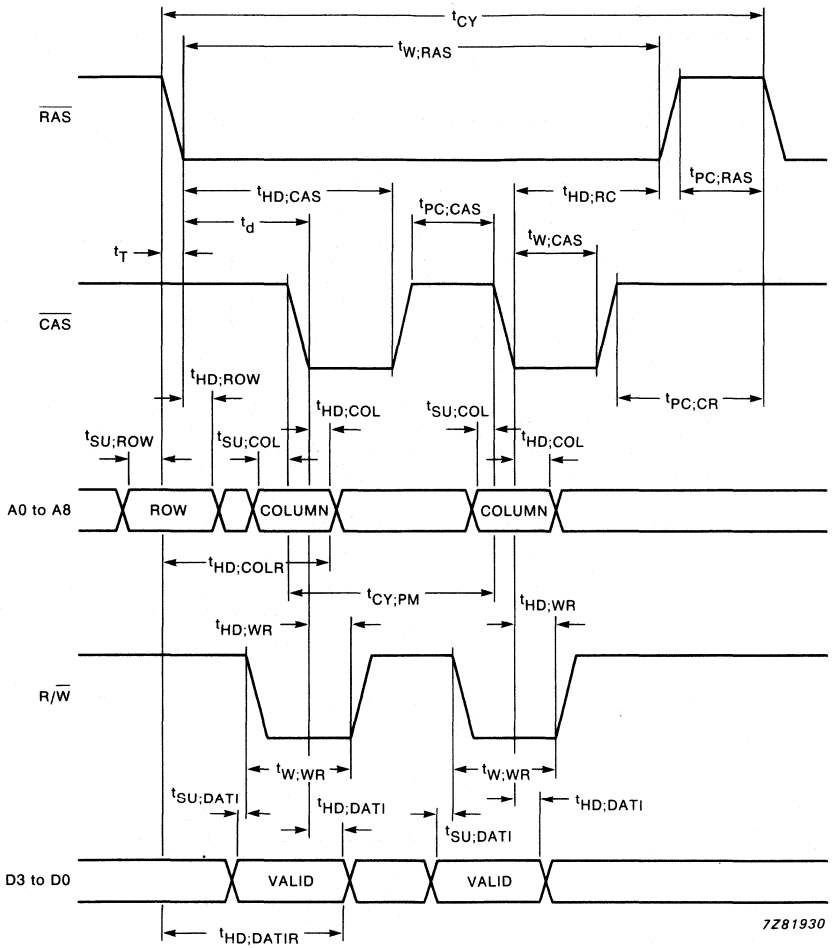


Fig. 5 Memory interface timing for write cycle to external DRAM.

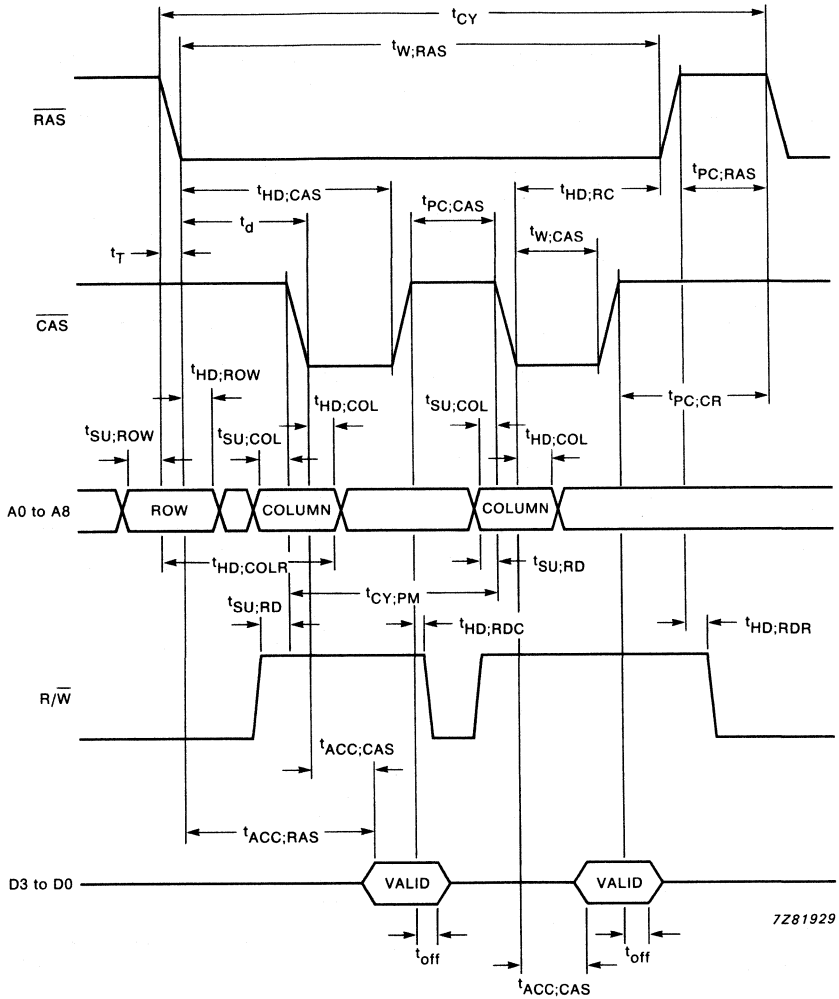
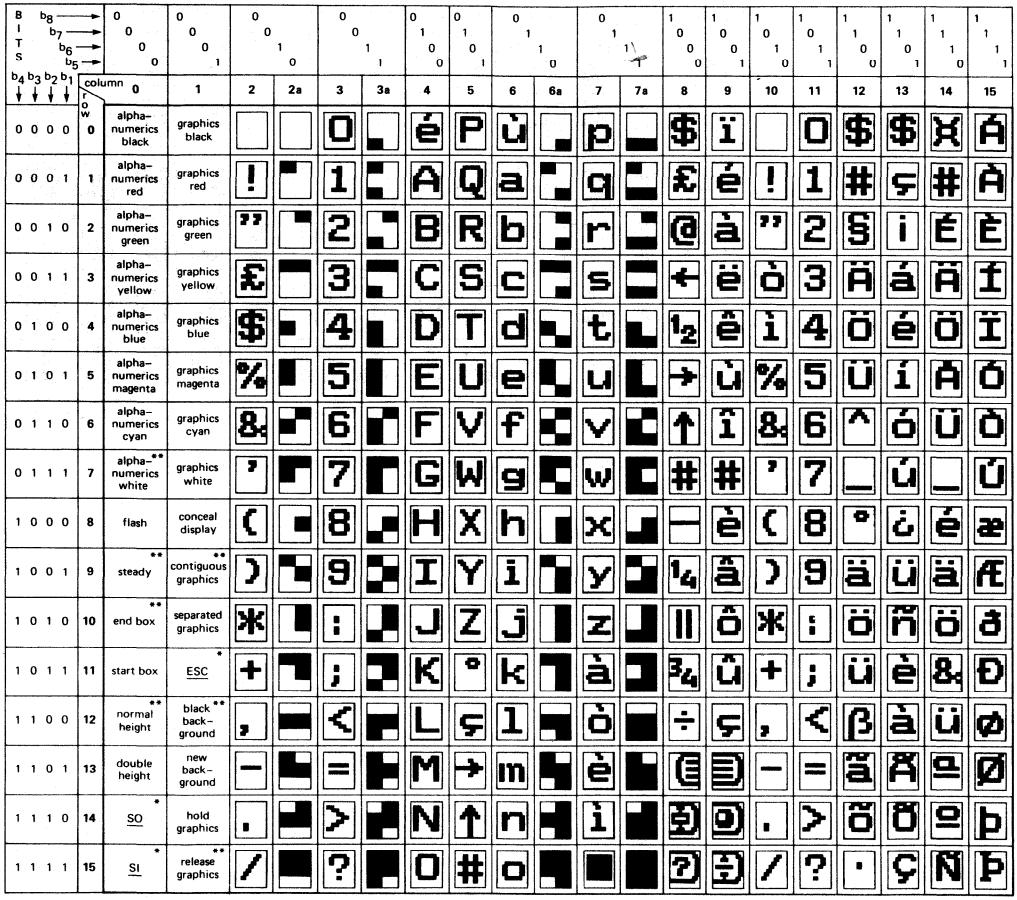


Fig. 6 Memory interface timing for read cycle from external DRAM.

DEVELOPMENT DATA



* These control characters are reserved for compatibility with other data codes

** These control characters are presumed before each row begins

Fig. 7 SAA9041A West European character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

7Z22659.1

(1) Where PHCB are the page Header Control Bits. Other combinations of PHCB default to English.

Fig. 8 SAA9041A West European national option sets.

DEVELOPMENT DATA

APPLICATION INFORMATION

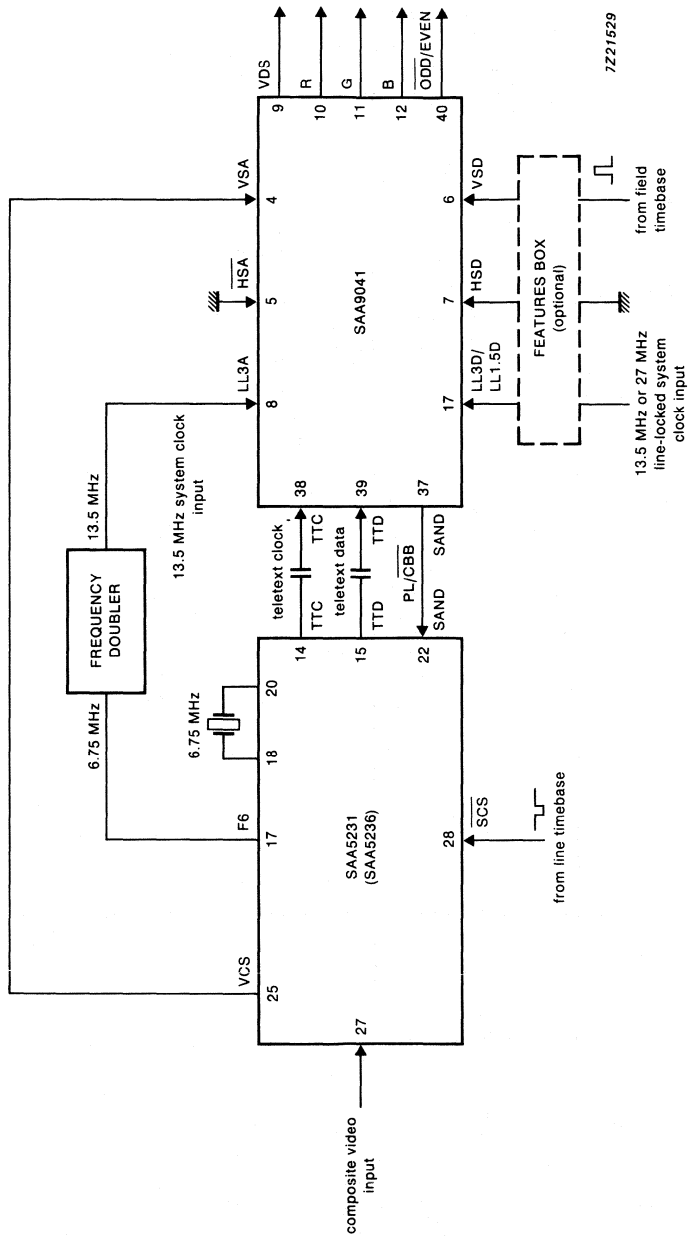


Fig. 9 SAA9041 application in analogue TV.

APPLICATION INFORMATION (continued)

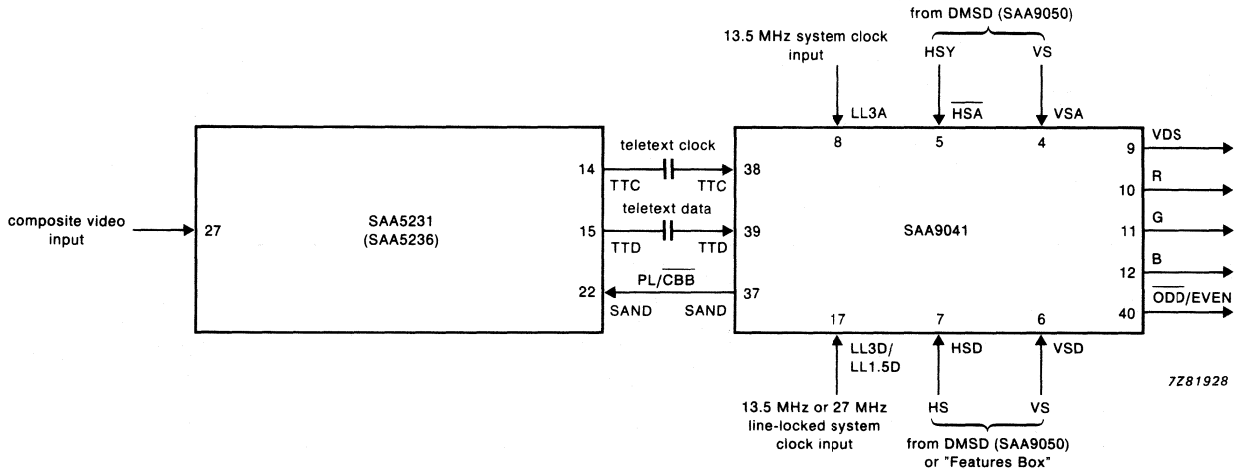


Fig. 10 SAA9041 application in digital TV.

DIGITAL MULTISTANDARD TV DECODER

GENERAL DESCRIPTION

The SAA9050 digital multistandard decoder (DMSD) performs demodulation and decoding of all quadrature modulated colour TV standards, and contains luminance and part-synchronization processing for all TV standards.

Features

- Luminance signal processing for all TV standards (PAL, NTSC, SECAM, B/W)
- Horizontal and vertical sync detection for all standards (525/625 lines)
- Chrominance signal processing for all quadrature amplitude modulated colour-carrier signals (PAL-B, G, H, I, M, N; NTSC-M)
- Requires only one crystal (24.576 MHz), which may also be used for audio processing
- Functions, settings and adjustments programmable under software control via the I^2C-bus
- User-programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Parallel (nibble) output format selectable (Y/U6, U5, V6, V5; U4, U3, V4, V3; U2, U1, V2, V1; U0, CS, V0, X)
- SECAM interface
- Cross-colour reduction by chrominance comb-filtering (NTSC)
- Comb-filters adapt automatically to line frequency
- Internal overflow protection
- Selectable chrominance amplitude control protection for non-standard signals
- Programmable horizontal position of the active video signal in each line
- Indirect I^2C control capability to select input from one of four video sources
- Indirect I^2C control capability for automatic flesh-tone correction
- Wide range hue control
- Internal coincidence detection

PACKAGE OUTLINE

40-lead DIL; plastic with internal heat spreader (SOT129).

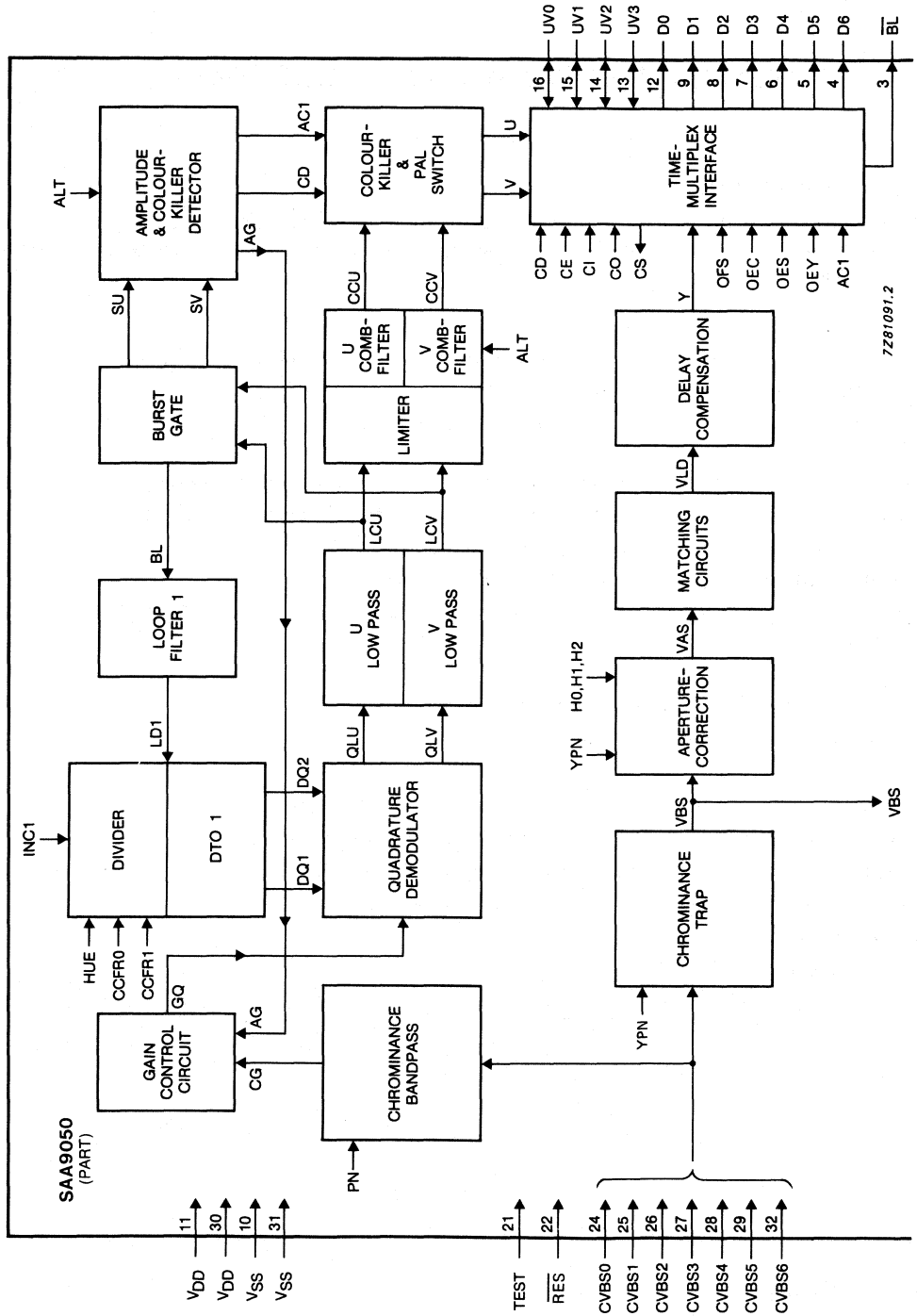


Fig.1a Block diagram; continued in Fig.1b.

DEVELOPMENT DATA

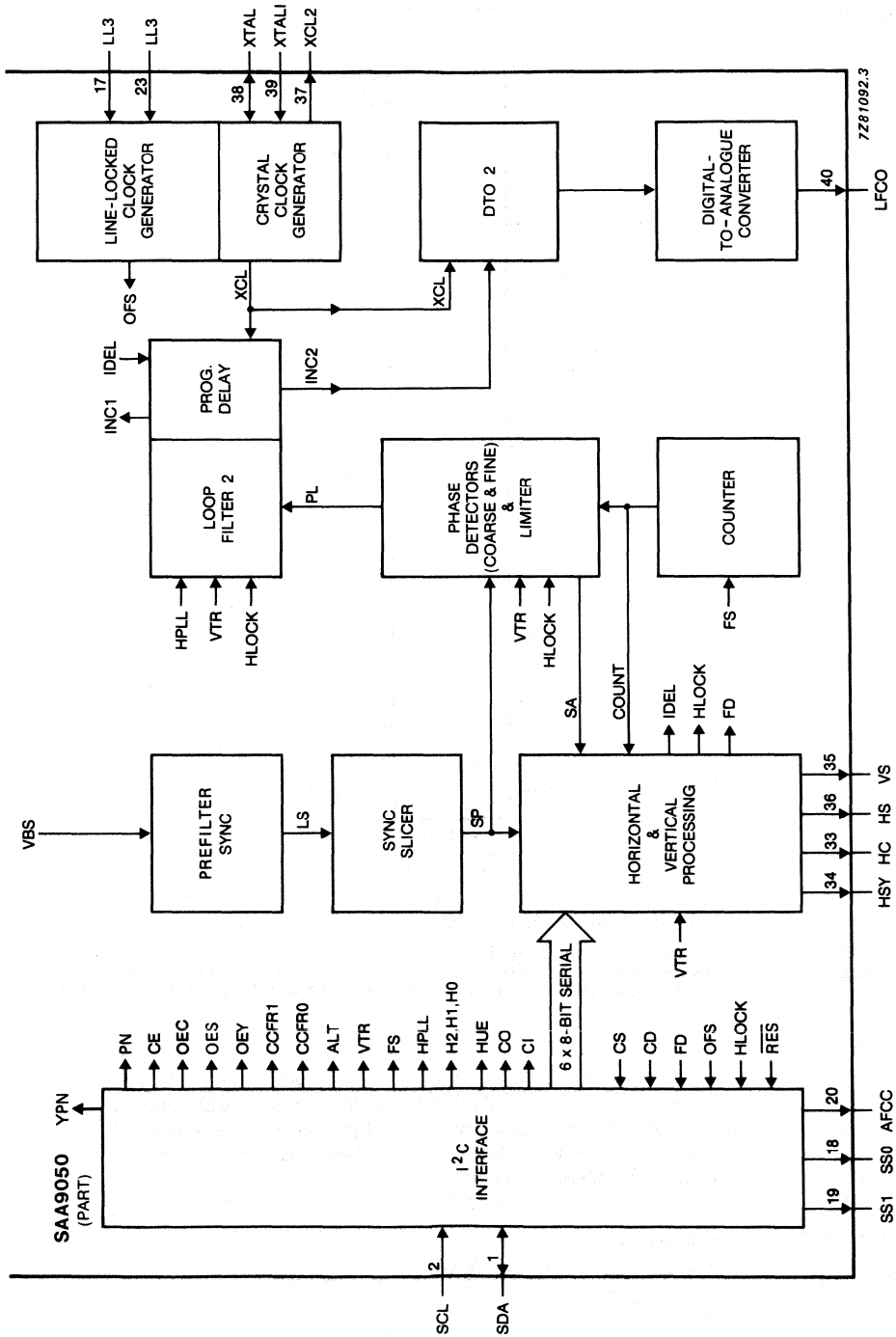


Fig.1b Block diagram; continued from Fig.1a.

PINNING

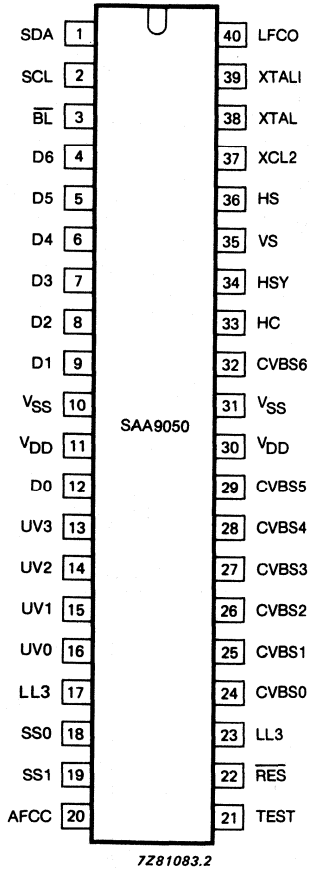


Fig.2 Pinning diagram.

1	SDA	I²C-bus serial data input/output
2	SCL	I²C-bus serial clock input
3	$\overline{BL}$	Blanking output to indicate the active video and line blanking periods. Active LOW
4	D6(MSB)	
5	D5	Luminance (Y) outputs, luminance is unipolar. The transmission
6	D4	is synchronized externally by $\overline{BL}$. The delay from CVBS input to
7	D3	D0-D6 output is 55 LL3 clocks in multiplexed format, and 58 LL3
8	D2	clocks in semi-parallel format. Luminance only is transmitted when
9	D1	LL3 = 13.5 MHz.
12	D0(LSB)	
10; 31	V_{SS}	Ground (0 V)
11; 30	V_{DD}	Positive supply voltage (+5 V)

13 14 15 16	UV3 UV2 UV1 UV0	PAL or NTSC colour difference signal output. In the input mode, CS (colour-SECAM) signals are received from the SECAM decoder. U and V signals are transmitted at 13.5 MHz. Output data format is two's complement with positive polarity
17	LL3	13.5 MHz line-locked clock
18 19	SS0 SS1	Source select output signals, set via the I^2C-bus to control the input switch (e.g. TDA9045)
20	AFCC	Automatic flesh-tone correction control activated via the I^2C-bus to control the colour track circuit of NTSC systems
21	TEST	Test input, when HIGH enables the scan-test mode
22	$\overline{RES}$	Reset input, active LOW, causes control registers 1 and 2 to be reset during the reset phase. The minimum LOW period of $\overline{RES}$ is 120 LL3 clocks
23	LL3	13.5 MHz line-locked system clock
24 25 26 27 28 29 32	CVBS0(LSB) CVBS1 CVBS2 CVBS3 CVBS4 CVBS5 CVBS6(MSB)	Digitized composite video, blanking and synchronization signal containing luminance, chrominance and all synchronization information. Two's complement format
33	HC	Horizontal clamping signal that indicates the black-level position before analogue-to-digital conversion. The start and stop time is programmable via the I^2C-bus in the range of −9.4 to + 9.5 μs in steps of 74 ns
34	HSY	Horizontal synchronization signal that indicates the sync pulse position before analogue-to-digital conversion. The start and stop time is programmable via the I^2C-bus in the range of −14.2 to + 4.7 μs in steps of 74 ns
35	VS	Vertical synchronization output that indicates the vertical position of the picture for 50 or 60 Hz field frequency
36	HS	Horizontal synchronization pulse output. Duration = 16 LL3 clocks. Synchronizes the horizontal position of the active video signal in each line and is programmable via the I^2C-bus in the range of −32 to + 32 μs in steps of 300 ns
37	XCL2	Clock output at half the crystal clock frequency (12.288 MHz). In phase with XTAL (pin 38)
38	XTAL	Crystal input/output. Input to the internal clock generator (from an external oscillator, when used), or output of the inverting amplifier to an external crystal (24.576 MHz)
39	XTALI	Input to the inverting amplifier from the external crystal (24.576 MHz); connected to ground when an external oscillator is used
40	LFCO	Line frequency control. Analogue output representing a multiple of the line frequency (6.75 MHz) with a 4-bit resolution, the phase of which is compared with the system clock by the clock generator circuit (SAA9057)

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (Fig.1)

The DMSD performs demodulation and decoding for PAL-B, G, H, I, M, N, NTSC-M TV standards and contains luminance and parts of the synchronization processing for all PAL, NTSC and SECAM TV standards. All of the controllable functions of the DMSD, user controls as well as factory adjustments, are accessed via the two-line, bidirectional I^2C-bus, so enhancing the adaptability of the digital TV concept.

Operation is based on a line-locked sampling frequency of 13.5 MHz, making the system fully adaptable to all line frequencies and requiring only one crystal for all TV standards.

Output formats (Fig.3)

The Y and U, V signals are transmitted separately, the Y signals in a data stream of 13.5 MHz from D0-D6 and the U, V signals in a nibble format from UV0 to UV3. The SECAM-decoder option also uses this clock mode.

Processing

The digital CVBS input is separated into its luminance (VBS) and chrominance (CG) parts by chrominance trap and chrominance bandpass circuits, which can be switched by the standard identification signals (PN/YPN) according to the detected PN centre frequency (3.58 or 4.43 MHz). The range of binary values for input/output signals are shown in Fig.4.

The separated luminance signal (VBS) is passed to an aperture-correction circuit that has programmable horizontal peaking. The corrected signal (VAS) is then matched to the full-scale of the appropriate word-width and limited to prevent overflow. The signal (now VLD) undergoes delay compensation to equalize the delays of the luminance and chrominance channels. Differences of delay compensation requirements in PAL and NTSC modes are catered for when switching is performed by the standard identification signal (PN).

In the chrominance channel, the amplitude of the chrominance signal (CG) is controlled to give a signal with constant burst amplitude (CQ). The control signal (AG) for gain-control is derived in the amplitude and colour-killer detection circuit. If there is a non-standard ratio between burst and chrominance amplitudes (−17% in the NTSC mode), an automatic colour-levelling circuit takes the function of amplitude detection to ensure correct chrominance amplitude and to avoid overflow and limiter defects.

Demodulation of the square-modulated chrominance signal (CQ) is performed by the quadrature demodulator which gives the baseband colour difference signals (LCU and LCV). The comb-filter stage then separates remaining luminance components from these signals and (for PAL) corrects their phase to give the signals CCU and CCV. The number of delay elements required in the comb-filter is minimized by the use of a reduced, blanked, line-locked clock. The comb-filter structure is changeable under the control of the standard-identification signal (ALT).
The colour-killer, under the control of amplitude and colour-killer detection (AC1 and CD), removes incoming signals that do not comply with the chosen standard. The PAL switch restores the correct phasing of the V signal when in PAL mode.

Regeneration of the colour carrier frequency is achieved by the phase-locked-loop comprising quadrature modulator, low pass filter, burst gate, loop filter 1 and discrete time oscillator (DTO 1). The latter is controlled by standard identification signals (CCFR0, CCFR1) and a signal (HUE) that influences the demodulation phase of the chrominance signal.

In the synchronization circuit, prefilter synchronization is implemented to normalize sync slopes. A sync-slicer provides the detected sync pulses (SP) to the H, V processing and phase detector stages.

The H and V processing comprises part of a PLL circuit for the regeneration of the horizontal synchronization (HS) and an adaptive filter for the detection of vertical sync (VS), see Fig.5. The H, V processing also generates the coincidence signal (HLOCK) which controls the mute function, and a standard identification signal (FD) which identifies nominal 625 or 525 lines per picture.

The phase detectors that receive the SP signal, also part of the PLL, control the generation of the line-locked clock (PL). Loop filter 2, which has a changeable bandwidth controlled by the video recorder/TV time constant signal (VTR), generates two increment signals (INC1 and INC2) with different delays. INC2 is programmable via the increment-delay signal (IDEL). INC1 corrects the regenerated subcarrier frequency at DTO 1 and INC2 performs phase incrementing of DTO 2. The crystal clock generator provides a stable 24.576 MHz clock input to DTO 2 which in turn supplies the 4-bit DAC with a digital control signal of 432 or 429-times the line frequency. The analogue output (LFCO) from the DAC goes to the clock generator (SAA9057).

The output signals D0 to D6 can be multiplexed under the control of an internal blanking and format signal. It is a time-multiplex interface that also provides an external blanking and format signal ($\overline{BL}$).

For real-time inputs to the DMSD, the line-locked clock LL3 is required as well as the digital CVBS signal (CVBS0 to CVBS6).

DEVELOPMENT DATA

PAL-B, G, H, I and NTSC detection

The current version of the DSMD is unable to distinguish between the PAL-B, G, H, I and NTSC 4.4 standards, if the NTSC 4.4 standard is chosen. To overcome this problem in automatic standard routine it is necessary to:

- check the NTSC 4.4 standard before the PAL-B, G, H and I standards

or

- cross check the PAL-B, G, H and I, if the NTSC 4.4 standard is detected.

FUNCTIONAL DESCRIPTION (continued)

I²C-bus interface

The following control signals are received via the I²C-bus (SDA and SCL) and the I²C-bus interface:

- standard identification signals (CCFR0, CCFR1, ALT, FS, CE, YPN)
- time constant VTR/TV (VTR)
- hue control (HUE)
- delay programming of the horizontal signals (HS, HC, HSY)
- increment-delay (IDEL)
- aperture-correction control (H0, H1, H2)
- fixed clock generation command (HPLL)
- internal colour ON/OFF (CO)
- internal colour forced ON for test purposes (CI)
- sync output enable (OES)
- luminance output enable (OEY)
- chrominance output enable (OEC)
- source select signal (SS0, SS1)
- automatic flesh-tone control (AFCC)

Signals transmitted from the DMSD via the I²C-bus are:

- standard identification signals (FD, CS)
- colour-killer status signal (CD)
- coincidence information (HLOCK)
- selected output format indicator (OFS)
- power-on-reset of DMSD (PONRES)

Time-multiplex interface (Fig.6)

The UV0 to UV3 signals from the SECAM decoder are received in a 13.5 MHz data stream in the following format:

input signal	sample 0	1	2	3	0	1	2	3
UV3						repeating		
UV2	U5	U3	U1	CS		repeating		
UV1						repeating		
UV0						repeating		

The signal CS is an information bit from the SECAM decoder:

CS = logic 0 indicates colour not detected in SECAM
CS = logic 1 indicates colour detected in SECAM
X = don't care

This bit is latched in the DMSD. The CS bit is transmitted to control circuits via the I²C-bus.

Commands that control the outputs of the time-multiplex interface are OES, OEY, OEC, CO and CI which are received via the I^2C-bus, and CD which is detected in the DMSD. The start condition of OES, OEY, OEC, CO and CI after initialization is always zero. The outputs are controlled as follows:

OES	OEY	OEC	outputs	output status
0 1	X X	X X	HS and VS	HIGH-impedance OFF-state active
X X	0 1	X X	D0 to D6 and $\overline{BL}$	HIGH-impedance OFF-state active
X X	X X	0 1	UV0 to UV3	HIGH-impedance OFF-state active

CO	CI	CD	outputs	output status
0	X	X	UV0 to UV3	colour OFF (zero)
1	0	0		colour OFF } controlled
1	0	1		colour ON } by CD
1	1	X		colour forced ON

X = don't care.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

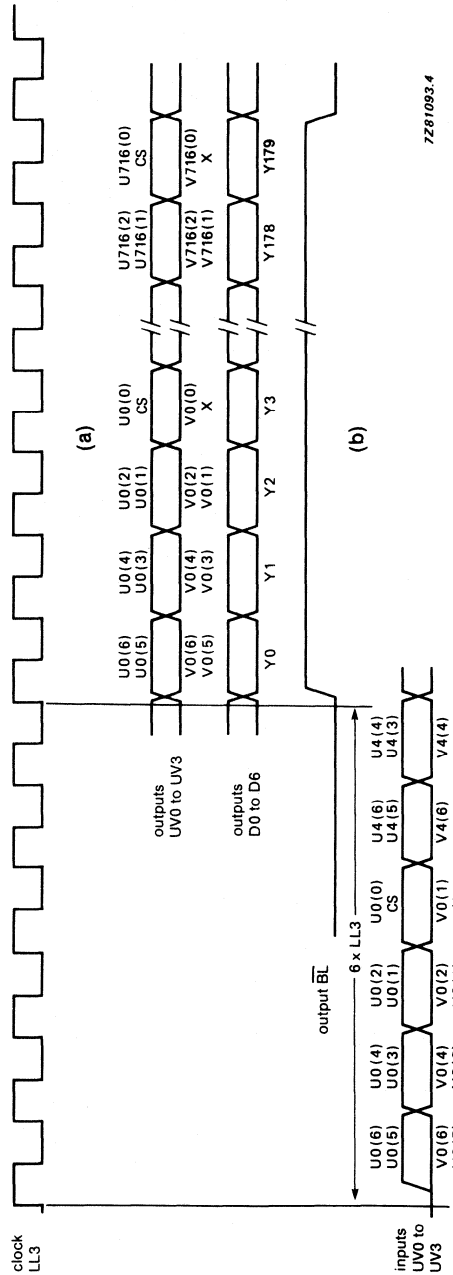
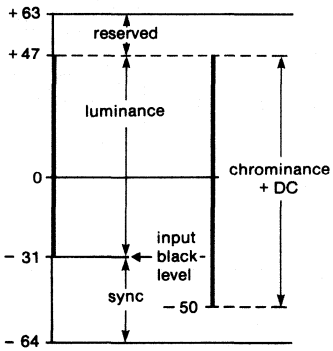
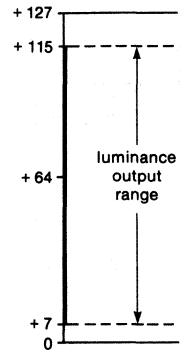


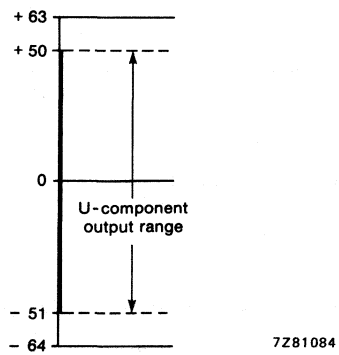
Fig.3 Correlation of signals: (a) serial mode; (b) parallel (nibble) mode when LL3 = 13.5 MHz; (c) serial mode in which SECAM chrominance signals (received via UV0 to UV3 from a SECAM decoder) are combined with DMSD luminance signals.



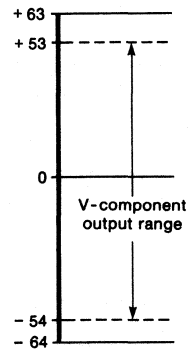
(a) CVBS0 to CVBS6 input range with 75% colour bar.



(b) Y output range.



(c) U output range (B–Y).



(d) V output range (R–Y).

Fig.4 Diagram showing input/output range of the DMSD (levels are given in binary values).

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

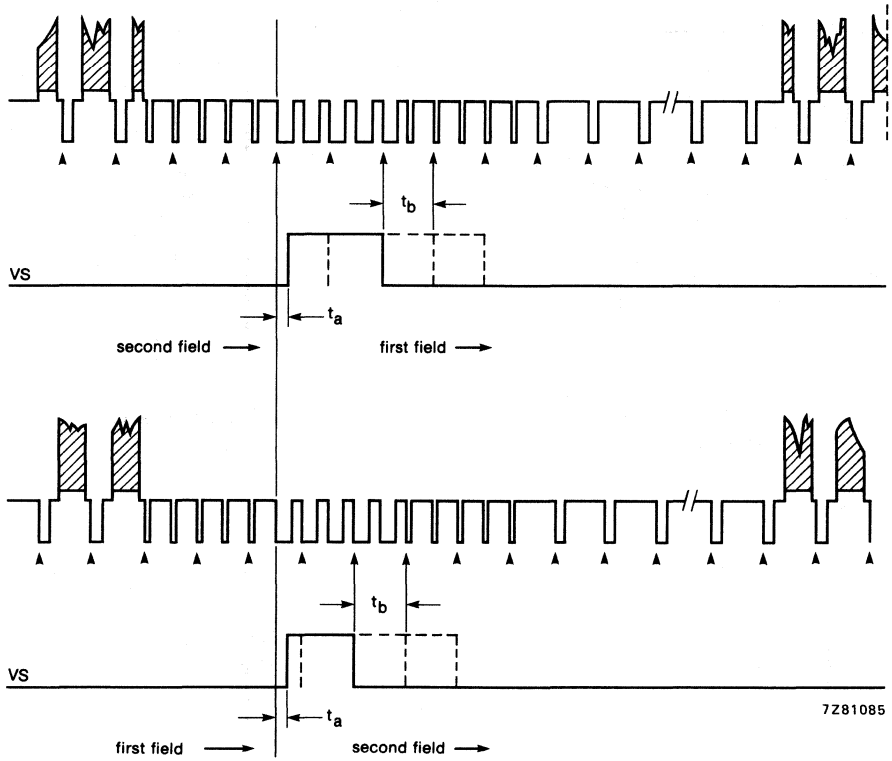


Fig.5 Vertical sync (VS): time t_a is approximately 24 μs; time t_b = 64 μs (the minimum vertical sync pulse length is 75 μs).

DEVELOPMENT DATA

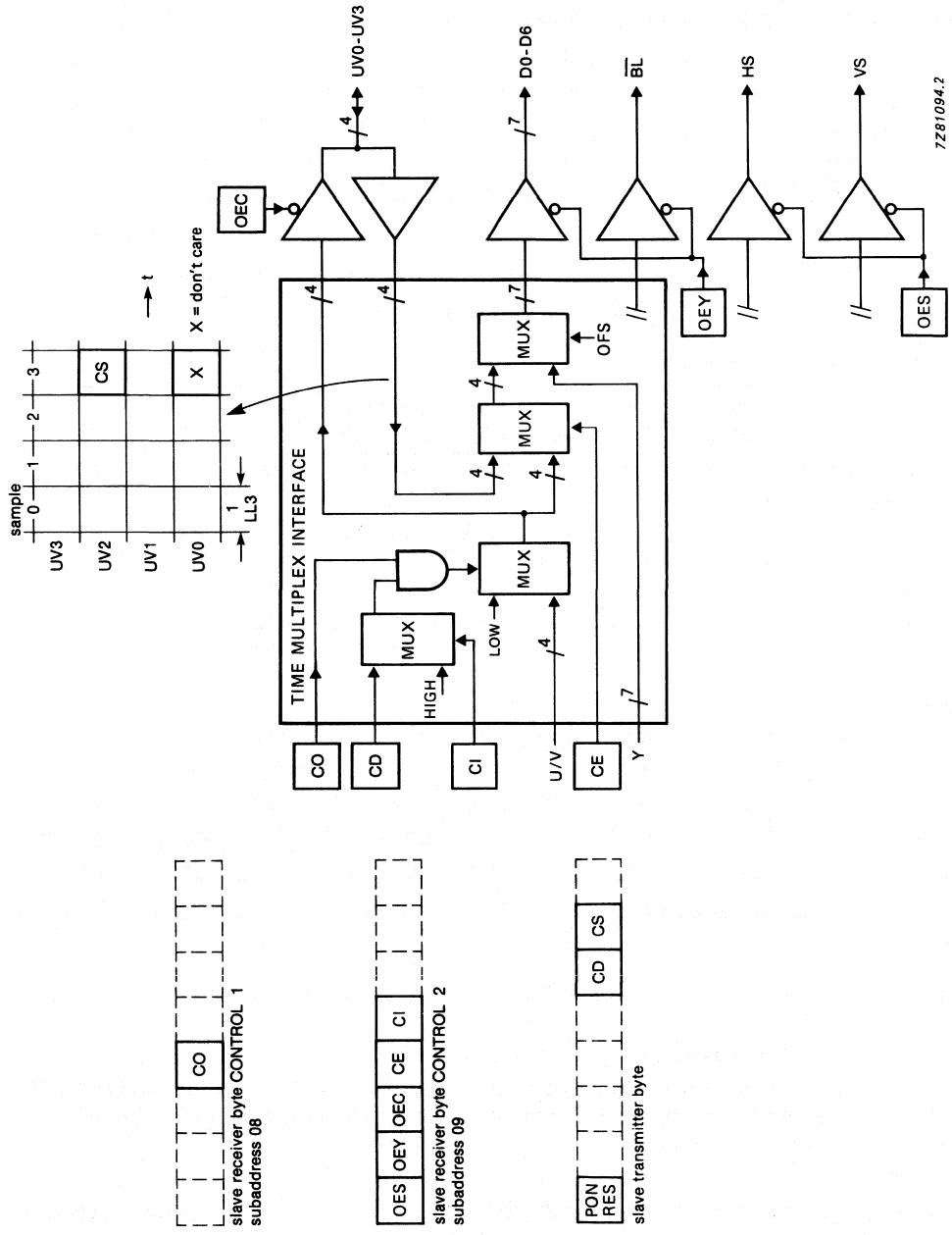


Fig.6 Schematic diagram of control signals at the time-multiplex interface and output stages.

SLAVE RECEIVER ORGANIZATION

Slave address and receiver format

Slave address for the digital multistandard decoder is:

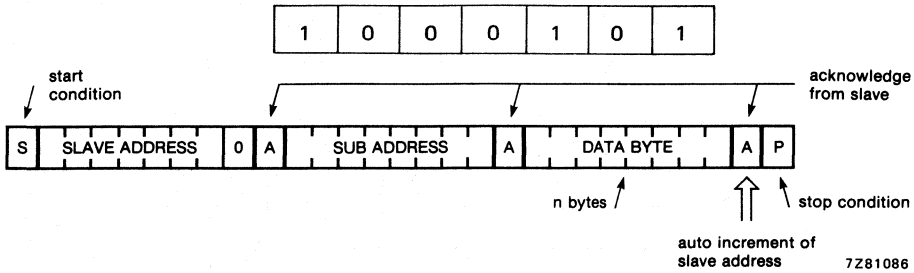


Fig.7 Slave receiver format.

Subaddress byte and data byte formats

register function	sub address	data byte D7	D6	D5	D4	D3	D2	D1	D0
Increment delay IDEL	00	A07	A06	A05	A04	A03	A02	A01	A00
Horizontal sync									
HSY start time	01	A17	A16	A15	A14	A13	A12	A11	A10
HSY stop time	02	A27	A26	A25	A24	A23	A22	A21	A20
Horizontal clamp									
HC start time	03	A37	A36	A35	A34	A33	A32	A31	A30
HC stop time	04	A47	A46	A45	A44	A43	A42	A41	A40
Horizontal sync after PHI1									
HS start time	05	A57	A56	A55	A54	A53	A52	A51	A50
Horizontal peaking	06	X	X	X	X	X	H2	H1	H0
Hue control	07	A77	A76	A75	A74	A73	A72	A71	A70
Control 1	08	HPLL	FS	VTR	CO	ALT	YPN	CCFR1	CCFR0
Control 2	09	OES	OEY	OEC	CE	CI	AFCC	SS1	SS0
Reserved	0A to 0F	X	X	X	X	X	X	X	X

Notes

The subaddress is automatically incremented. This enables quick initialization by the I^2C-bus controller within one transmission.

All eight bits of the subaddress have to be decoded by the device.

The subaddresses shown are acknowledged by the device. Subaddresses 10 to 1F (reserved for the SECAM decoder SAA9055) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.

X = don't care.

After power-on-reset the control registers 1 and 2 (subaddresses 08 and 09) are set to logic 0, all other registers are undefined.

The least significant bit of an analogue control or alignment register is defined as AX0.

Increment delay control IDEL (application dependent)

decimal multiplier	delay time (step size = 2/13.5 MHz = 148 ns)	control bits* A07	A06	A05	A04	A03	A02	A01	A00
−1	−148 ns (min. value)	1	1	1	1	1	1	1	1
to									
−110	−16.3 μs (outside available range)	1	0	0	1	0	0	1	0
−111	−16.44 μs	1	0	0	1	0	0	0	1
to									
−214	−3.17 μs (max. value if FS = logic 1)	0	0	1	0	1	0	1	0
−215	−31.85 μs (outside central counter if FS = logic 1)**	0	0	1	0	1	0	0	1
−216	−32 μs (max. value if FS = logic 0)	0	0	1	0	1	0	0	0
−217	−32.148 μs (outside central counter if FS = logic 0)**	0	0	1	0	0	1	1	1
to									
−256	−37.9 μs (outside central counter)**	0	0	0	0	0	0	0	0

* A sign bit, designated A08 and internally set to HIGH, indicates values are always negative.

** The horizontal PLL does not function in this condition: the system clock frequency is set to a value fixed by the last update and is within ± 7.1% of the nominal frequency.

Horizontal sync HSY start time (application dependent)

decimal multiplier	delay time (step size = 1/13.5 MHz = 74 ns)	control bits A17	A16	A15	A14	A13	A12	A11	A10
+ 191	−14.2 μs (max. negative value)	1	0	1	1	1	1	1	1
to									
+ 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0.074 μs	1	1	1	1	1	1	1	1
to									
−64	+ 4.7 μs (max. positive value)	1	1	0	0	0	0	0	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Horizontal sync HSY stop time (application dependent)

decimal multiplier	delay time (step size = 1/13.5 MHz = 74 ns	control bits A27	A26	A25	A24	A23	A22	A21	A20
+ 191	−14.2 μs (max. negative value)	1	0	1	1	1	1	1	1
to									
+ 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0.074 μs	1	1	1	1	1	1	1	1
to									
−64	+ 4.7 μs (max. positive value)	1	1	0	0	0	0	0	0

Horizontal clamp HC start time (application dependent)

decimal multiplier	delay time (step size = 1/13.5 MHz = 74 ns)	control bits A37	A36	A35	A34	A33	A32	A31	A30
+ 127	−9.4 μs (max. negative value)	0	1	1	1	1	1	1	1
to									
+ 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0.074 μs	1	1	1	1	1	1	1	1
to									
−128	+ 9.5 μs (max. positive value)	1	0	0	0	0	0	0	0

Horizontal clamp HC stop time (application dependent)

decimal multiplier	delay time (step size = 1/13.5 MHz = 74 ns)	control bits A47	A46	A45	A44	A43	A42	A41	A40
+ 127	−9.4 μs (max. negative value)	0	1	1	1	1	1	1	1
to									
+ 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0.074 μs	1	1	1	1	1	1	1	1
to									
−128	+ 9.5 μs (max. positive value)	1	0	0	0	0	0	0	0

Horizontal sync after PHI1 HS start time (application dependent)

50 Hz; 625-line mode and FS = logic

decimal multiplier	delay time (step size = 4/13.5 MHz = 296 ns)	control bits A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 109	forbidden; outside available central counter range	0	1	1	1	1	1	1	1
		0	1	1	0	1	1	0	1
+ 108 to + 1	−32 μs (max. neg. value)	0	1	1	0	1	1	0	0
	−0.296 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −107	+ 0.296 μs	1	1	1	1	1	1	1	1
	+ 31.7 μs (max. pos. value)	1	0	0	1	0	1	0	1
−108 to −128	forbidden; outside available central counter range	1	0	0	1	0	1	0	0
		1	0	0	0	0	0	0	0

60 Hz; 525-line mode and FS = logic

decimal multiplier	delay time (step size = 4/13.5 MHz = 296 ns)	control bits A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 107	forbidden; outside available central counter range	0	1	1	1	1	1	1	1
		0	1	1	0	1	0	1	1
+ 106 to + 1	−31.8 μs (mag. neg. value)	0	1	1	0	1	1	0	0
	−0.294 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −107	+ 0.294 μs	1	1	1	1	1	1	1	1
	+ 31.5 μs (max. pos. value)	1	0	0	1	0	1	0	1
−108 to −128	forbidden; outside available central counter range	1	0	0	1	0	1	0	0
		1	0	0	0	0	0	0	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Horizontal peaking H2, H1, H0, PN (user dependent) (see Fig.13)

aperture factor (af)	control bits H2	H1	H0	YPN
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

Chrominance trap select (system mode dependent)

YPN	chrominance trap
0	4.43 MHz
1	3.58 MHz

Hue phase (user dependent)

hue phase	control bits A77	A76	A75	A74	A73	A72	A71	A70
+ 178.6 deg to	1	1	1	1	1	1	1	1
0 deg to	1	0	0	0	0	0	0	0
−180 deg	0	0	0	0	0	0	0	0

Step size per least-significant bit (A70) = 1.4 deg.

Reference point for positive colour difference signals = 0 deg.

The hue phase may be shifted ± 180 deg from the reference point using bit A77, the colour difference signals are then switched from normal positive to negative polarity.

Horizontal clock PLL (application dependent)

function	HPLL control bit
horizontal clock PLL open, horizontal frequency fixed	1
horizontal clock PLL closed	0

Field frequency select (system mode dependent)

function	FS control bit
60 Hz; 525-line mode	1
50 Hz; 625-line mode	0

VTR/TV mode select (system mode dependent)

function	VTR control bit
VTR mode	1
TV mode	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Colour-on control (system mode dependent)

function	CO control bit
colour ON	1
colour OFF (all colour output samples zero)	0

Alternate/non-alternate mode (system mode dependent)

function	ALT control bit
alternate mode (PAL)	1
non-alternate mode (NTSC)	0

Colour carrier frequency control (system mode dependent)

colour carrier frequency	control bits CCFR1	CCFR0
4 433 618.75 Hz (PAL-B, G, H, I; NTSC-4.43)	0	0
3 575 611.49 Hz (PAL-M)	0	1
3 582 056.25 Hz (PAL-N)	1	0
3 579 545 Hz (NTSC-M)	1	1

Colour decoding table

colour standard	control bits FS				ALT		CCFR1	CCFR0
PAL-B, G, H, I		0			1		0	0
NTSC-4.43; 50 Hz		0			0		0	0
NTSC-4.43; 60 Hz		1			0		0	0
PAL-M	HPLL	1	VTR	CO	1	YPN	0	1
PAL-N		0			1		1	0
NTSC-M		1			0		1	1

Sync output enable (system mode dependent)

function	control bit OES
outputs HS and VS active	1
outputs HS and VS HIGH-Z	0

Y output enable (system mode dependent)

function	control bit OEY
outputs D0 to D6 and $\overline{BL}$ active	1
outputs D0 to D6 and $\overline{BL}$ HIGH-Z	0

Chrominance output enable (system mode dependent)

function	control bit OEC
outputs UV0 to UV3 active; chrominance signal when CD = logic 1; zero signal when CD = logic 0	1
outputs UV0 to UV3 HIGH-Z	0

External colour select (system mode dependent)

function	control bit CE
select external colour channel; serial format via inputs UV0 to UV3	1
select internal colour channel	0

Internal colour forced ON/OFF (for test or service requirements only)

function	control bit CI
colour forced ON if CO = logic 1 (CD = X) colour OFF if CO = logic 0 (CD = X)	1
colour OFF if CO = logic 0 (CD = X) colour controlled by CD if CO = logic 1	0

X = don't care

Automatic flesh-tone corrector (colour track) (user dependent)

function	AFCC control bit
colour track ON	1
colour track OFF	0

Source select (system mode dependent)

function	control bits SS1	SS0
select input CVBS0	0	0
select input CVBS1*	0	1
select input CVBS2	1	0
select input CVBS3	1	1

* Not allowed when operating with TDA9045.

DEVELOPMENT DATA

SLAVE TRANSMITTER ORGANIZATION

Slave transmitter format

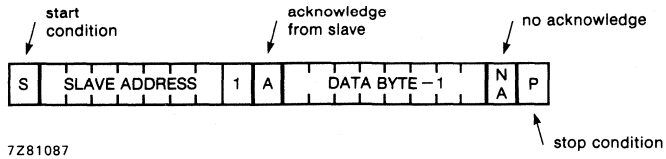


Fig.8 Slave transmitter format (a general call address is not acknowledged).

The format of data byte 1 is:

PONRES	HLOCK	OFS	FD	0	CD	CS	0

PONRES — Status bit for power-on-reset ($\overline{RES}$) and after a power failure:

logic 1 after the first power-on-reset and after a power failure. Also set to logic 1 after a severe voltage dip that may have disturbed slave receiver data in the PAL/NTSC decoder (SAA9050). PONRES sets all data bits of control registers 1 and 2 to zero.

logic 0 after a successful read of the PAL/NTSC decoder status byte.

HLOCK — Status bit for horizontal frequency lock (transmitter identification, stop or mute bit):

logic 1 if horizontal frequency is not locked (no transmitter available);

logic 0 if horizontal frequency is locked (transmitter received).

OFS — Status bit for output format selection:

logic 1 when quasi-parallel format is selected:

D0 to D6	Y				Y				Y				Y			
UV0 to UV3	U6	U5	V6	V5	U4	U3	V4	V3	U2	U1	V2	V1	U0	CS	V0	X
												→	1 LL3 clock			

← time frame →

X = don't care

FD — Detected field frequency status bit:
logic 1 when received signal has 60 Hz sync pulses;
logic 0 when received signal has 50 Hz sync pulses.

CD — PAL/NTSC colour-detected status bit:
logic 1 when PAL/NTSC colour signal is detected;
logic 0 when no PAL/NTSC colour signal is detected.

CS — SECAM colour-detected status bit:
logic 1 when SECAM colour signal is detected;
logic 0 when no SECAM colour signal is detected.

PROGRAMMING IDEL, HSY, HC and HS

These variables are programmed via data words on the I²C-bus. In the following examples decreasing numbers correspond to increasing time.

IDEL (Fig.9)

The IDEL data word compensates for the time delays in data processing between loop filter 2 and the quadrature demodulator and includes internal and external (system) signal paths. The internal path from loop filter 2 takes INC1 to the divider and DTO 1. This delay (t_{REF}) corrects the relationship between the subcarrier frequency and the line frequency. The external path accounts for the following time delays:

t_{IDEL}	programmable delay time	in LL3 periods
t_a	processing time of DTO 2 and the D-A converter	
t_b	chrominance bandpass and gain control stage delay times	
t_{CGC}	clock generator circuit delay time	
t_{ADC}	analogue-to-digital converter delay time	
t_{SRC}	sample-rate converter delay time	
t_{SECAM}	SECAM colour decoder delay time	

As the delays t_a and t_b are known constants, t_{IDEL} is programmed as follows:

$$t_{IDEL} = -115 - 0.5\,(99 - t_{CGC} - t_{ADC} - t_{SRC}^{*} - t_{SECAM}^{*})$$

Programming range: −115 to −214/−216.

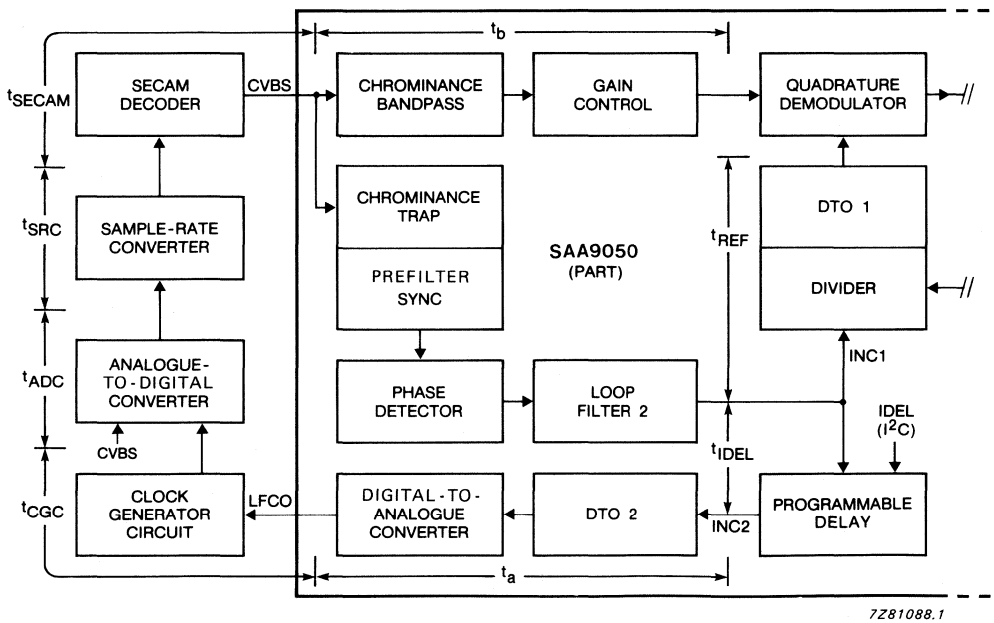


Fig.9 Compensation of delay times by increment delay control IDEL.

* When included in the application.

PROGRAMMING IDEL, HSY, HC and HS (continued)

HSY (Fig.10)

Referring to Fig.10 points (1), (2) and periods, a, b:

HSY start time = $T_{(1)-(2)} + 42 - a$ LL3 clock periods

HSY stop time = $T_{(1)-(2)} + 42 - b$ LL3 clock periods

Programming range of HSY start/stop time: + 191 to –64 LL3 clock periods.

HC (Fig.10)

Referring to Fig.10 points (1), (2) and periods c, d:

HC start time = $T_{(1)-(2)} + 42 - c$ LL3 clock periods

HC stop time = $T_{(1)-(2)} + 42 - d$ LL3 clock periods

Programming range of HC start/stop time: + 127 to –128 LL3 clock periods.

HS (Fig.10)

The reference positions of HS in PAL and NTSC modes are shown in Fig.10 at points (4) and (5) respectively. To move the HS pulse to the centre of blanking pulse $\overline{BL}$ the following equation is used:

$$\text{HS (NTSC)}: \frac{-[\text{position of HS relative to point (3)} + 17\ \text{LL3}]}{4\ \text{LL3}}$$

$$\text{HS (PAL)} : \frac{-[\text{position of HS relative to point (3)} + 14\ \text{LL3}]}{4\ \text{LL3}}$$

In the example given in Fig.10:

HS (NTSC): – [55 + 17] /4 = –18 (decimal) = 1110 1110 (bianry)

HS (PAL) : – [62 + 14] /4 = –19 (decimal) = 1110 1101 (binary)

DEVELOPMENT DATA

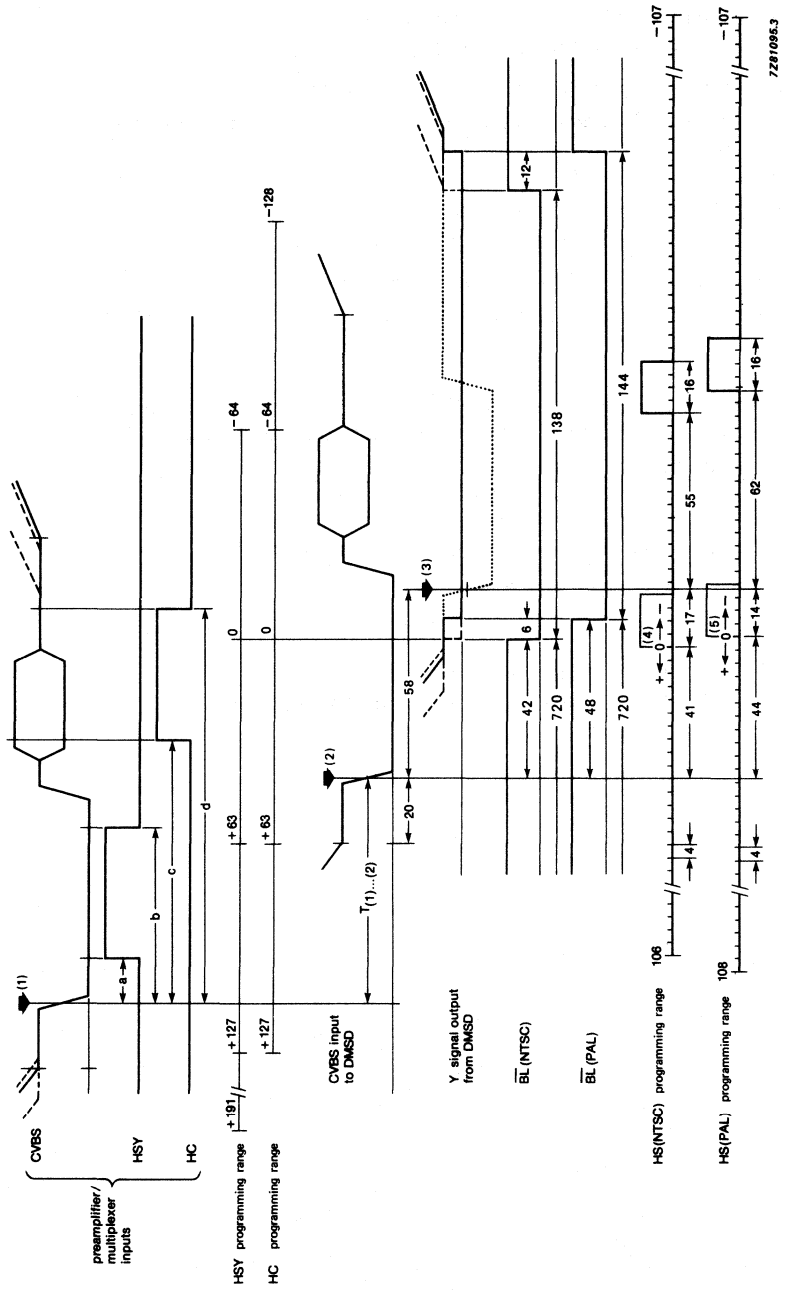


Fig.10 Signal correlation.

Notes to Fig.10

———— represents PAL signals
– – – – – represents NTSC signals (showing tolerance of active video)

HSY and HC inputs are referenced to the analogue input CVBS (1)

$\overline{BL}$ and HS outputs are referenced to the digital input CVBS (2) or to the DMSD output (3).

Waveform timing is indicated in numbers (n) of LL3 cycles (n x $1/f_{LL3}$), where n = 1 for HSY, HC, CVBS input to DMSD and $\overline{BL}$, and n = 4 for HS.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	$I_{O\,max}$ = 20 mA	V_{DD}	−0.5	+ 7.0	V
Input voltage range		V_I	−0.5	+ 7.0	V
Output voltage range		V_O	−0.5	+ 7.0	V
Maximum power dissipation per package		P_{tot}	−	*	W
Operating ambient temperature range		T_{amb}	0	+ 75	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* Value to be fixed.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		V_{DD}	4.5	–	5.5	V
Supply current	note 1	I_{DD}	–	350	450	mA
Inputs						
Input voltage LOW						
pins 13 to 17, 21 to 29, 32 and 38		V_{IL}	−0.5	–	+ 0.8	V
pins 1 and 2		V_{IL}	−0.5	–	+ 1.5	V
Input voltage HIGH						
pins 13 to 16, 21, 22, 24 to 29 and 32		V_{IH}	2.0	–	V_{DD}	V
pins 1, 2 and 38		V_{IH}	3.0	–	V_{DD}	V
pins 17 and 23		V_{IH}	2.4	–	V_{DD}	V
Input leakage current						
pins 1, 2, 13 to 17, 21 to 29 and 32		I_{LI}	–	–	10	μA
Input capacitance						
pins 13 to 16, 24 to 29 and 32		C_I	–	–	5	pF
pin 17		C_I	–	–	15	pF
pin 23		C_I	–	–	30	pF
pin 39		C_I	8	–	–	pF
pins 1, 2, 21, 22 and 38		C_I	–	–	7.5	pF
Outputs						
Output capacitance pins 4 to 9 and 12		C_O	–	–	7.5	pF
Output voltage LOW						
pins 3 to 9, 12 to 16, 18 to 20 and 33 to 37	I_{OL} = 2 mA	V_{OL}	0	–	0.6	V
pin 1	I_{OL} = 5 mA	V_{OL}	0	–	0.45	V
Output voltage HIGH						
pins 1, 3 to 9, 12 to 16, 18 to 20 and 33 to 37	$-I_{OH}$ = 0.5 mA	V_{OH}	2.2	–	V_{DD}	V
Output leakage current						
pins 3 to 9, 12 to 16, 35 and 36	note 2	I_{LO}	–	–	10	μA
LFCO output voltage (peak-to-peak value)	note 3					
	$R_L \geqslant 10$ kΩ; $C_L < 15$ pF	$V_{O(p-p)}$	1	–	–	V
	$R_L \geqslant 1$ kΩ; $C_L < 15$ pF	$V_{O(p-p)}$	0.5	–	–	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Timing (Fig.11)						
LL3 cycle time	note 4	T_{C3}	69	–	80	ns
LL3 duty factor	T_{C3H}/T_{C3}	d	43	–	57	%
LL3 rise and fall times	note 5	t_r, t_f	–	–	6	ns
Input set-up time		t_{SU}	12	–	–	ns
Input hold time		t_{IH}	5	–	–	ns
Output hold time	C_L = 7.5 to 25 pF	t_{OH}	3	–	–	ns
$\overline{BL}$ output (pin 3)						
Output hold time		t_{OH}	9	–	–	ns
Output delay time	C_L = 7.5 to 25 pF	t_d	–	–	50	ns
HC, HSY (pins 33, 34)						
Output delay time	C_L = 25 pF; V_{OH} = 2.6 V	t_d	–	–	80	ns
Crystal oscillator (Fig.12)						
Nominal frequency (third harmonic)		f_n	–	24.576	–	MHz
Permissible deviation from nominal frequency (adjustment tolerance)		$\Delta f/f_n$	–50	–	+ 50	10^{-6}
Temperature deviation		$\Delta f/f_n$	–20	–	+ 20	10^{-6}
Crystal temperature range		T_{XTAL}	0	–	+ 70	°C
Load capacitance		C_L	8	–	–	pF
Resonance resistance		R_r	–	40	–	Ω
Motional inductance		L_1	–	*	–	mH
Motional capacitance		C_1	–	1.5 ± 20%	–	fF
Parallel capacitance		C_0	–	3.5 ± 20%	–	pF

Notes to the characteristics

1. Supply current measured at f_n, inputs LOW and outputs unconnected.
2. Output leakage current measured with outputs in HIGH impedance state.
3. LIFCO output voltage measured with pin 40 AC coupled and a 4-bit triangular waveform clocked at 24.576 MHz.
4. For minimum and maximum cycle times $\Delta f = \pm 7.1\%$ of typical frequency value.
5. Difference between t_r and t_f of LL3 must be less than 1 ns; rising and falling edge are assumed to be smooth due to low pass filtering.

* Value to be fixed.

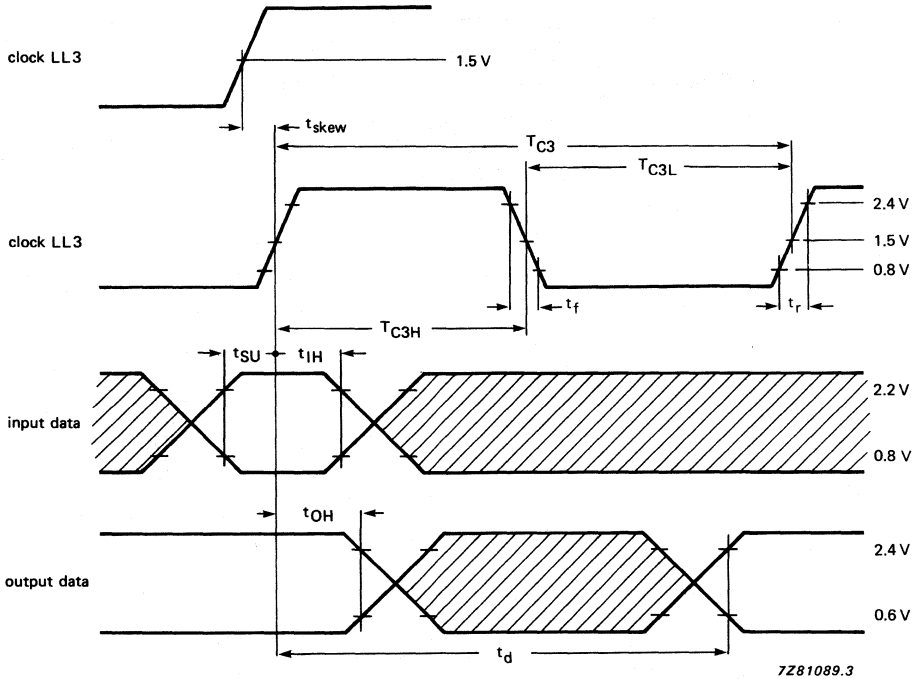


Fig.11 Timing diagram.

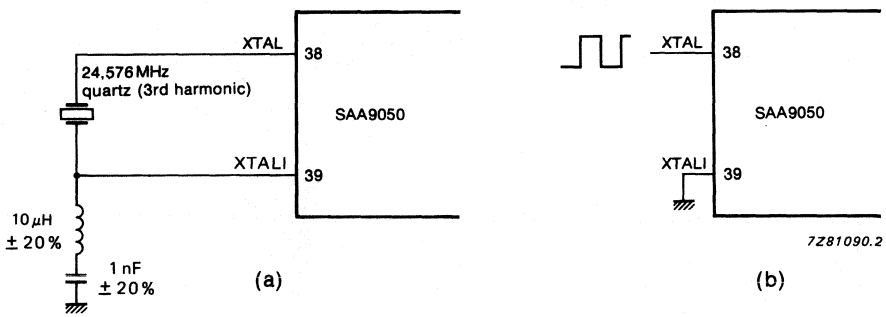
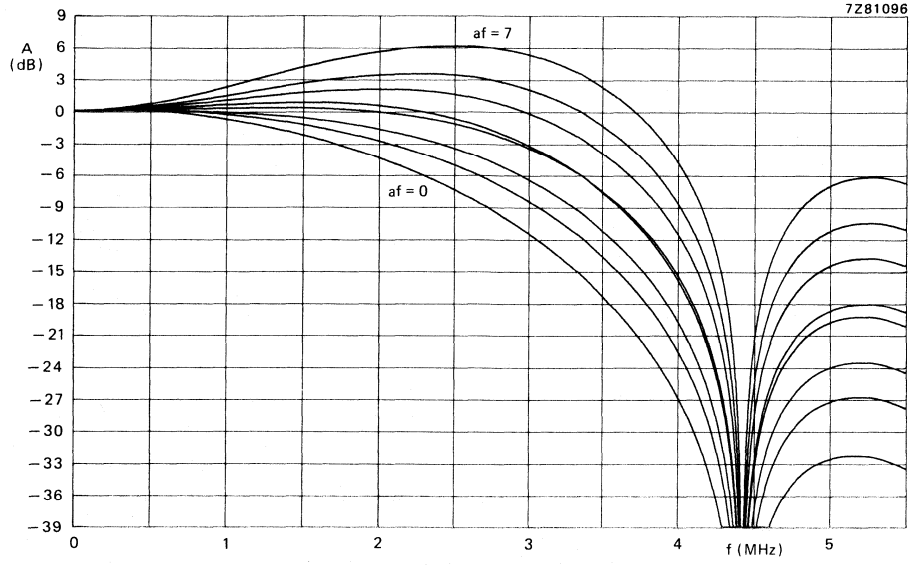
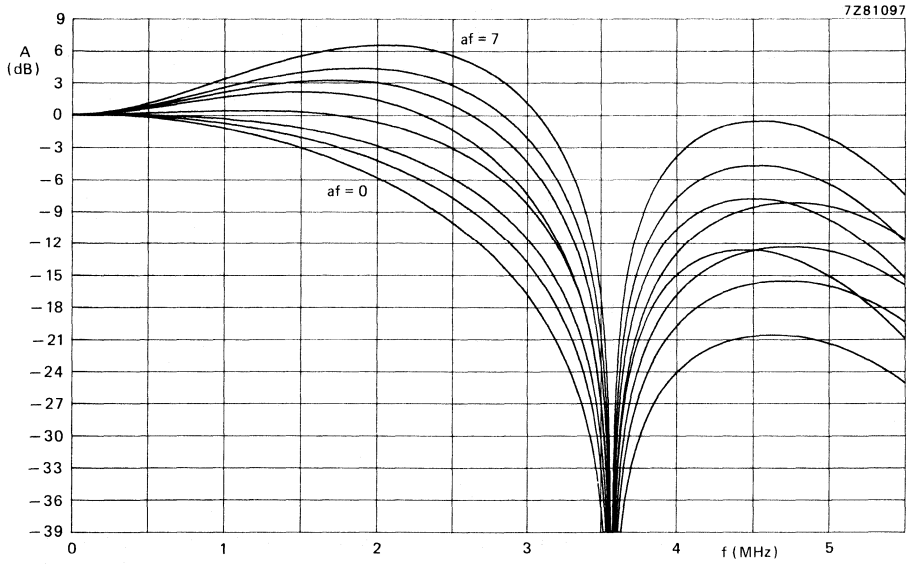


Fig.12 Oscillator circuit requirements: (a) with quartz crystal; (b) with external clock.

(a)



(b)



Aperture factor selection:

af	H2	H1	H0
0	0	0	0
– – – – – through to – – – – –			
7	1	1	1

Fig.13 Horizontal peaking aperture factors (af): (a) YPN = logic 0 (colour subcarrier = 4.43 MHz); (b) YPN = logic 1 (colour subcarrier = 3.58 MHz).

DIGITAL SECAM DECODER (DSD)

GENERAL DESCRIPTION

The SAA9055 is designed to provide colour difference signals for a digital TV signal processing system.

Features

- Phase-linear chrominance bandpass filter for cross-colour improvement
- Programmable filter characteristics for optimum adaption for different IF stages
- Recursive "Cloche" (Bell) filter
- Zero-crossing detection, FM demodulator with high AM rejection
- One demodulator for both carrier frequencies
- Base-band signal adjustment in gain and offset
- De-emphasis with recursive filter structure
- Line delay and cross-over switch for colour difference signals
- Output multiplexer for the UV format of the Digital Multistandard Secam Decoder
- Standard identification circuit with programmable sensitivity
- Programmable delay for the composite video blanking signal
- Address selection for I^2C-bus:
  SAA9055P/8A = address 8A (HEX)
  SAA9055P/8E = address 8E (HEX)

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

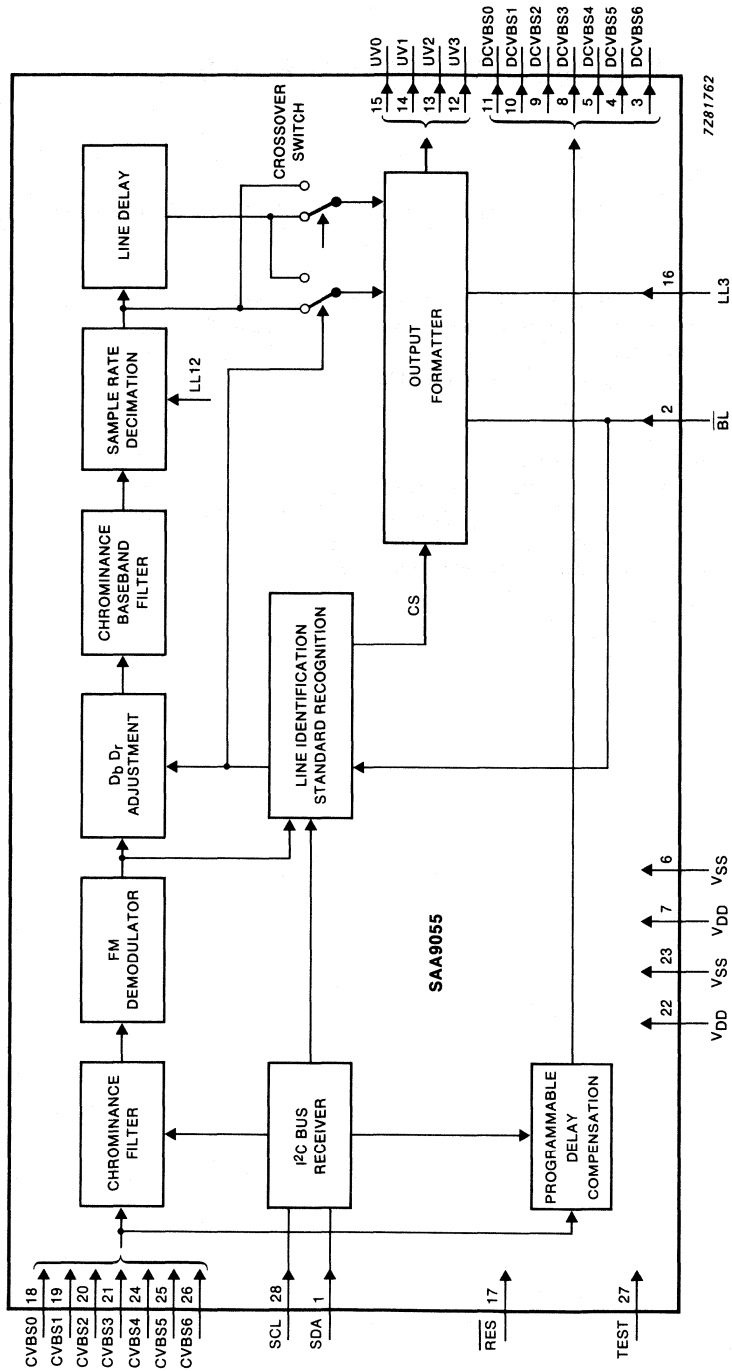


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

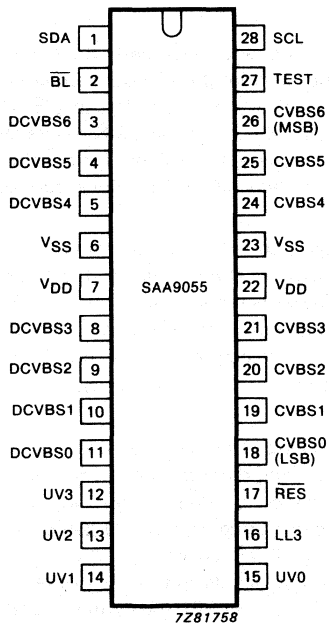


Fig. 2 Pinning diagram.

1	SDA	I^2C-bus serial data input, receive only, no data is transmitted from the DSD
2	$\overline{BL}$	This signal from the digital multistandard decoder indicates the active video and line blanking period
3	DCVBS6	Delayed composite video, blanking and synchronization output
4	DCVBS5	As pin 3
5	DCVBS4	As pin 3
6	V_{SS}	Ground
7	V_{DD}	+ 5 V supply
8	DCVBS3	As pin 3
9	DCVBS2	As pin 3
10	DCVBS1	As pin 3
11	DCVBS0	As pin 3
12	UV3	UV colour difference signals, via this port the decoded colour difference signals are transmitted to the DMSD in a mixed parallel/serial format. Additionally the status flag CS (colour in SECAM detected) is encoded in the UV data stream. The output drivers can be set to high impedance (3-state) via the I^2C-bus.
13	UV2	As pin 12
14	UV1	As pin 12
15	UV0	As pin 12
16	LL3	LL3 is the line-locked system clock at 13.5 MHz
17	$\overline{RES}$	The reset signal (active LOW) disables the UV buffers
18	CVBS0	Composite video, blanking and synchronization (LSB) input
19	CVBS1	As pin 18
20	CVBS2	As pin 18
21	CVBS3	As pin 18
22	V_{DD}	As pin 7
23	V_{SS}	As pin 6
24	CVBS4	Composite video, blanking and synchronization
25	CVBS5	As pin 24
26	CVBS6	As pin 24 (MSB)
27	TEST	This signal (active HIGH) enables the scan test mode
28	SCL	I^2C-bus serial clock input

FUNCTIONAL DESCRIPTION

The Digital Secam Decoder (DSD) forms an integral part of a digital TV signal processing system. The system incorporates a Video Processor and Input Selector (TDA9045), an A/D Converter (PNA7509), a Sample Rate Converter (SAA9058), a Digital Multi-Standard Decoder (SAA9050) or a Digital Multi-Standard Decoder with separate chrominance and luminance input (SAA9051), a Digital Deflection Controller (SAA9062/3/4)*, a Clock Generator Circuit (SAA9057), a Video Processor with DACs (SAA9060), a Colour Transient Improvement Circuit (TDA4565), a Video Control Combination Circuit (TDA4580), and an Octuple 6-bit DAC and a Feature Box. Figure 9 illustrates the timing of the input and output signals relative to the input clock (LL3).

The DMSD decodes and demodulates the colour information from all TV standards which employ a quadrature modulated colour carrier. The DMSD also processes the luminance and synchronization signals and generates auxiliary signals.

The DSD separates the colour information which it demodulates and decodes to provide the colour difference signals. These signals are subsequently encoded to produce a serial/parallel data stream at the UV output. Figure 4 illustrates the formatting and timing of the UV output port. Because SECAM colour processing takes longer than PAL/NTSC processing the CVCBS signal for the DMSD is delayed in the DSD. The length of delay can be programmed via the I^2C-bus to adapt the signal for the different design realizations of the DMSD. The possible range of variations is between 0 and 31 clock periods of LL3. The minimum delay is 55 periods of LL3.

The chrominance bandpass filter for separating the frequency modulated colour carrier consists of several phase-linear FIR filters which improve the cross-colour behaviour. The non-linear phase (Bell) filter has a recursive structure (IIR filter). Figure 3 illustrates the frequency response of the chrominance band-pass filter and Bell filter. One of the FIR filters can be programmed via the I^2C-bus to provide optimal adaption for the various IF stages. Different responses can be selected by means of a 7-bit control word. Figure 8 illustrates some examples of frequency responses of the programmable adaptive filer.

Only one FM demodulator is used to demodulate the chrominance signal; this accomodates both carrier frequencies regardless of the centre frequency. It is a zero-crossing demodulator with a real time divider which is a pipeline structure. After demodulation the baseband signal is adjusted, line sequentially, to the appropriate colour difference signal. During the clamping period, the demodulated reference carrier is compared with the previous reference signal by the line identification circuit. The identification circuit compares the phase of the two demodulated burst signals and, if the phase relationship is incorrect for several lines (not SECAM), the CS flag (colour in SECAM) will be reset.

The baseband filter consists of a linear phase low-pass filter together with a de-emphasis filter with a recursive structure. Figure 5 illustartes the frequency response of the de-emphasis and band-pass filters for the colour difference signals. After filtering, the sample rate is reduced to a quarter (LL12 = 3.375 MHz). The word length is truncated to seven bits. The resultant signal is delayed by one line period (64 μs = 216 clock periods of 3.375 MHz). The signals, delayed and non-delayed, can be switched either directly or cross-wise to two different outputs which correspond to the colour difference signals.

The cross-over switch is controlled by the line identification circuit. At the end of the chrominance path an output formatter transforms the 14 bits (2 x 7 bits clocked by 3.375 MHz) to a 4-bit wide channel which is clocked by 13.5 MHz (LL3). The bits are separated into odd and even and then serialized.

* The digital TV signal processing system has the option of using one of three Digital Deflection Controllers (SAA9062/3/4). The choice of DDC is dependent on the format of the CRT and the line/field frequency.

The format for the UV output is the same as that of the UV I/O port in the DSMD (SAA9050/51). The timing multiplexer is controlled by the external signal BL from the DSMD. Signal BL is also used as a line-locked synchronization signal to generate several internal burst gate pulses. Figure 6 illustrates the timing relationship between the line-reference signal (BL) and the composite video signal.

The CS flag is transmitted via the chrominance data-stream because the DSD has no I^2C-bus transmitter. If no SECAM colour is detected the UV port will be set to zero. After reset the UV lines will be set to high impedance (3-state) and the DSD must be re-initialized via the I^2C-bus to enable further operation.

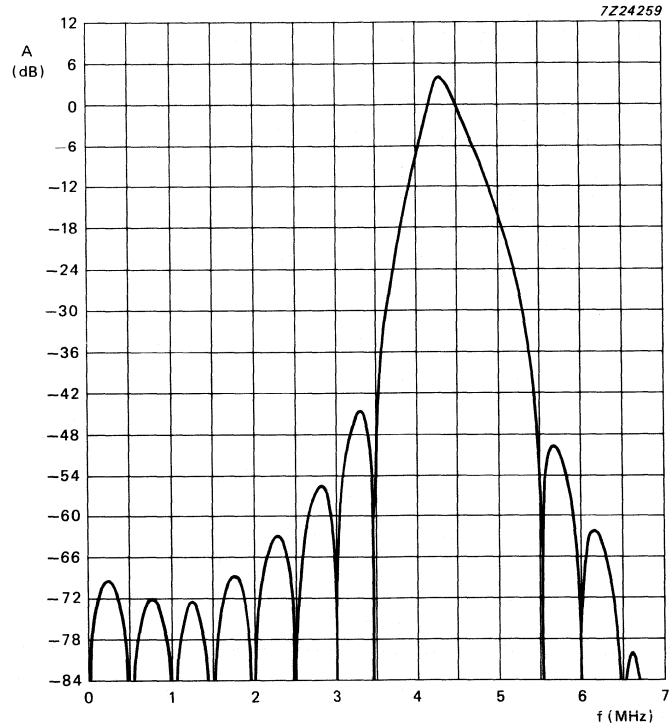


Fig. 3 Frequency response of chrominance bandpass and Bell filter.

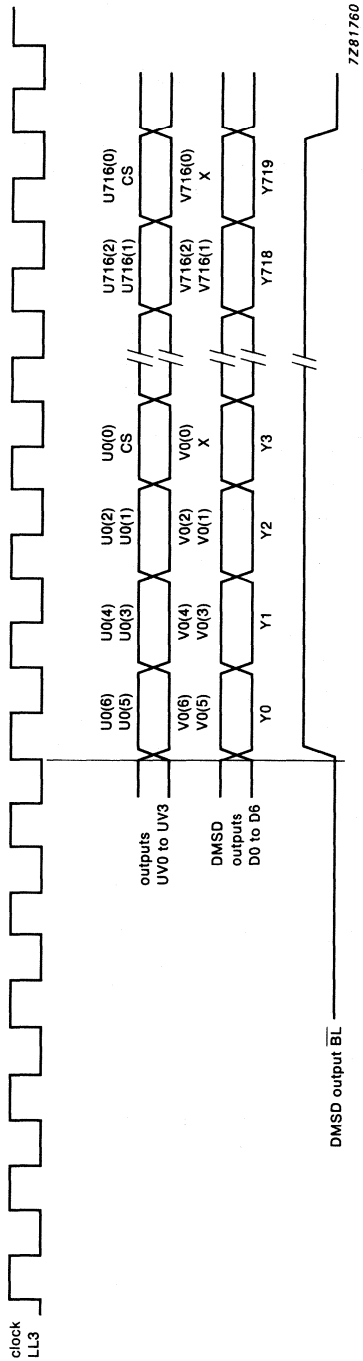


Fig. 4 Format and timing of the UV output port.

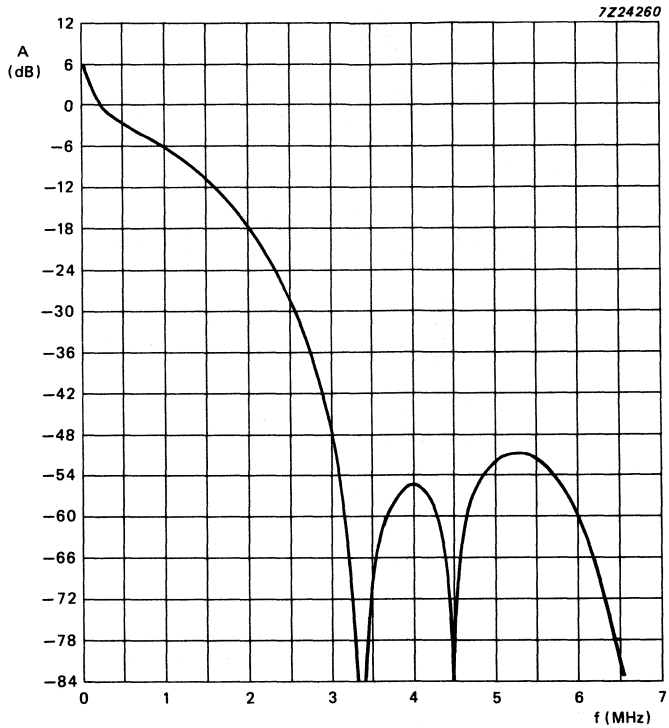


Fig. 5 Frequency response of the de-emphasis and base-band filter for the colour difference signals.

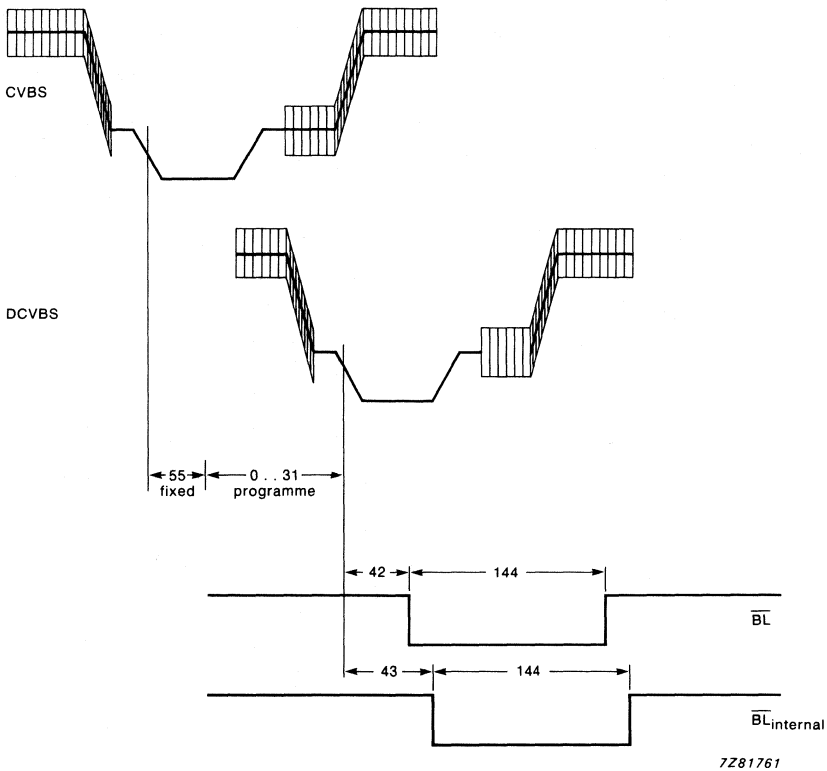


Fig. 6 Timing relationship between the line-reference signal ($\overline{BL}$) and the composite video signal.

I²C-BUS PROTOCOL

Slave receiver organization

The slave addresses for the digital SECAM decoder are shown in Figure 7.
The slave address is selected by bonding and is marked on the package.

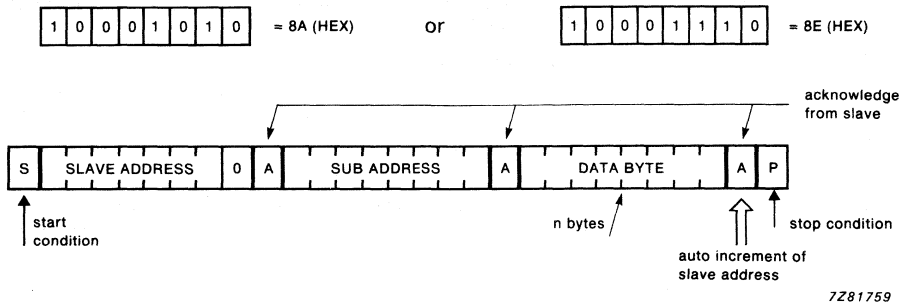


Fig. 7 Slave receiver format.

Table 1 Subaddress definition

register function	subaddress (HEX)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
CVBS delay time	10	MA1	MA0	X	DT4	DT3	DT2	DT1	DT0
Main counter start address (MA9..... MA0)	11	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2
Burst gate begin	12	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Burst gate end	13	BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0
Standard recognition sensitivity	14	R7	R6	R5	R4	R3	R2	R1	R0
Programmable adaptive filter	15	X	P6	P5	P4	P3	P2	P1	P0
Control register	16	X	X	X	X	X	C2	C1	C0
Reserved	17–1F	X	X	X	X	X	X	X	X

Notes to Table 1

1. The subaddress is automatically incremented to enable quick initialization by the I²C-bus controller within one transmission.
2. All eight bits of the subaddress are decoded by the device.
3. The subaddresses shown are acknowledged by the device. Subaddresses 00 to 0F (reserved for the Digital Multi-Standard Decoder) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.
4. X = don't care.
5. After power-on-reset the control register (subaddress 16) is set to logic 0, all other registers are undefined.

DEVELOPMENT DATA

Subaddress 10 (HEX)

Delay compensation between SECAM processing and PAL/NTSC chrominance processing.

Application dependent.

DT4	DT3	DT2	DT1	DT0	delay time
0	0	0	0	0	no additional delay for CVBS (minimum fixed delay through DSD = 55 x LL3)
0	0	0	0	1	1 x 74 ns = 74 ns
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	1	1	31 x 74 ns = 2.3 μs (maximum delay = 86 x LL3)

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

Subaddress 10 and 11 (HEX)

Main counter start address.

Application dependent.

MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	delay time	
0	1	1	1	1	1	1	1	1	1	+511	outside central counter range
—										—	
—										—	
—										—	
—										—	
0	1	1	0	1	0	0	0	1	0	+418	
0	1	1	0	1	0	0	0	0	1	+417	417 x 74 ns ≈ +31 μs (maximum positive value)
—										—	
—										—	
—										—	
0	0	0	0	0	0	0	0	0	1	+1	+74 ns
0	0	0	0	0	0	0	0	0	0	0	reference point*

* Reference point position to be fixed.

MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	delay time	
1	1	1	1	1	1	1	1	1	1	−1	−74 ns
—										—	
—										—	
—										—	
1	0	0	1	0	0	0	0	1	0	−446	−446 x 74 ns ≈ −33 μs (maximum negative value)
1	0	0	1	0	0	0	0	0	1	−447	outside central counter range
—										—	
—										—	
—										—	
—										—	
1	0	0	0	0	0	0	0	0	0	−512	

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

Internal counter range: −446 to + 417

Subaddress 12 (HEX)

Burst gate begin (start time)

Application dependent.

BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0	dec	delay time
0	0	0	0	0	0	0	0	0	zero reference point
0	0	0	0	0	0	0	1	1	74 ns
—	—	—	—	—	—	—	—	—	
—	—	—	—	—	—	—	—	—	
1	1	1	1	1	1	1	1	255	18.89 μs

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

DEVELOPMENT DATA

Subaddress 13 (HEX)

Burst gate end (stop time)

Application dependent.

BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0	dec	delay time
0	0	0	0	0	0	0	0	0	zero reference point
0	0	0	0	0	0	0	0	1	74 ns
–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–
1	1	1	1	1	1	1	1	255	18.89 μs

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

The stop time must be greater than the start time.

The reference point position of the burst gate start/stop time is identical with the main counter zero position.

Subaddress 14 (HEX)

Standard recognition sensitivity

Application dependent

R7	R6	R5	R4	R3	R2	R1	R0	function
								relationship between the number of line identification errors related to a window of 312 lines
0	0	0	0	0	0	0	0	0 : 312 theoretical highest sensitivity
0	0	0	0	0	0	0	1	1 : 312
0	0	0	1	1	0	0	1	25 : 312
1	1	1	1	1	1	1	1	255 : 312 theoretical lowest sensitivity

For programmed numbers from 0 to approximately 25 (dec) the colour signal is switched off. With the value 25 (dec) the colour signal will be enabled only when extremely good signal quality is present. If the colour signal quality is reduced, i.e. VCR signal source, bad S/N ratio, bad quantization, diminished colour carrier and insufficient IF adaption, the sensitivity should be set lower (higher programmed number up to 255 (dec) in order to prevent excessive switching and thus ensure constant colour.

DEVELOPMENT DATA

Subaddress 15 (HEX)

Programmable adaptive filter PAF (P6–P0)

Application (IF stage) dependent

The programmable adaptive filter, together with the cloche and linear bandpass filter, forms a filter-curve that treats the chrominance frequency spectra with different gain but linear phase. The frequency characteristic is a system of sinusoidal waveforms which are described by:

- Reference "knots" of constant gain (0 dB)
- Frequency points ("tops") with maximum gain
- The amount of maximum gain
  (There is also a switchable pre-amplifier in another stage of the bandpass filter).

The components of the PAF can be programmed via the I^2C-bus by using device address 8A (or 8E) and subaddress 15 thereby producing 57 different transfer functions. An example of some transfer functions is given in Figure 8 (a) to (d).

MSB	P6	P5	P4	P3	P2	P1	P0	function			
								maximum gain at tops			
–	X	X	X	X	1	1	1	19 dB			
–	X	X	X	X	1	1	0	14 dB			
–	X	X	X	X	1	0	1	9.5 dB			
–	X	X	X	X	1	0	0	6 dB			
–	X	X	X	X	0	1	1	3.5 dB			
–	X	X	X	X	0	1	0	2 dB			
–	X	X	X	X	0	0	1	1 dB			
–	X	X	X	X	0	0	0	0 dB			
								position of tops and knots (MHz)			
								top	knot	top	Figs 8a–d
–	X	1	1	1	X	X	X	3.375	4.5	5.625	+ A/dB (d)
–	X	1	1	0	X	X	X	4.5	5.625	6.75	–A/dB (d)
–	X	1	0	1	X	X	X	4.219	5.063	5.906	–A/dB (c)
–	X	1	0	0	X	X	X	3.375	4.219	5.063	+ A/dB (c)
–	X	0	1	1	X	X	X	4.05	5.4	6.75	–A/dB (b)
–	X	0	1	0	X	X	X	2.7	4.05	5.4	+ A/dB (b)
–	X	0	0	1	X	X	X	2.89	3.86	4.82	+ A/dB (a)
–	X	0	0	0	X	X	X	3.86	4.82	5.79	–A/dB (a)
								additional pre-amplification			
–	1	X	X	X	X	X	X	times two			
–	0	X	X	X	X	X	X	times one			
*	X	X	X	X	X	X	X	* MSB not used			

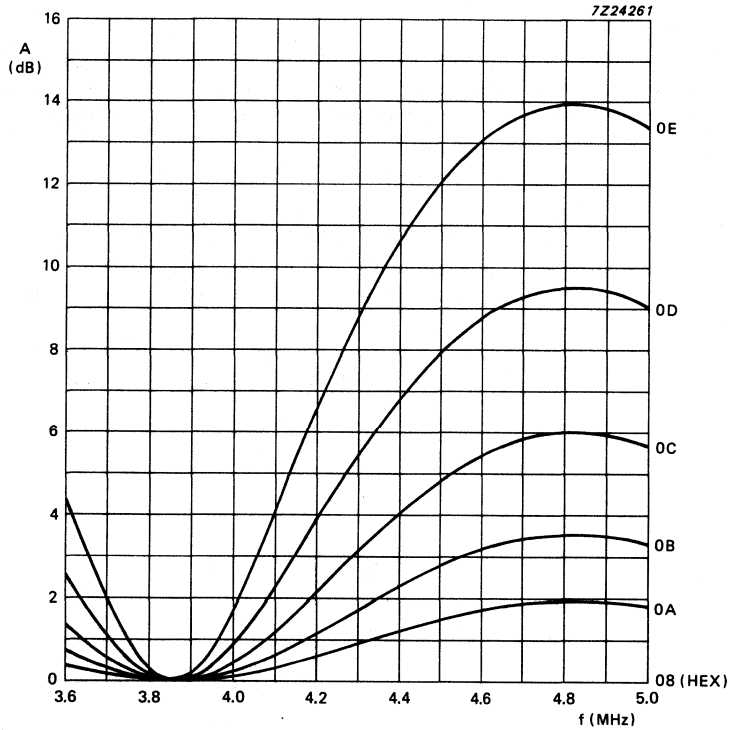


Fig. 8(a) Examples of frequency response for the programmable adaptive filter; from 08 to 0E (HEX).

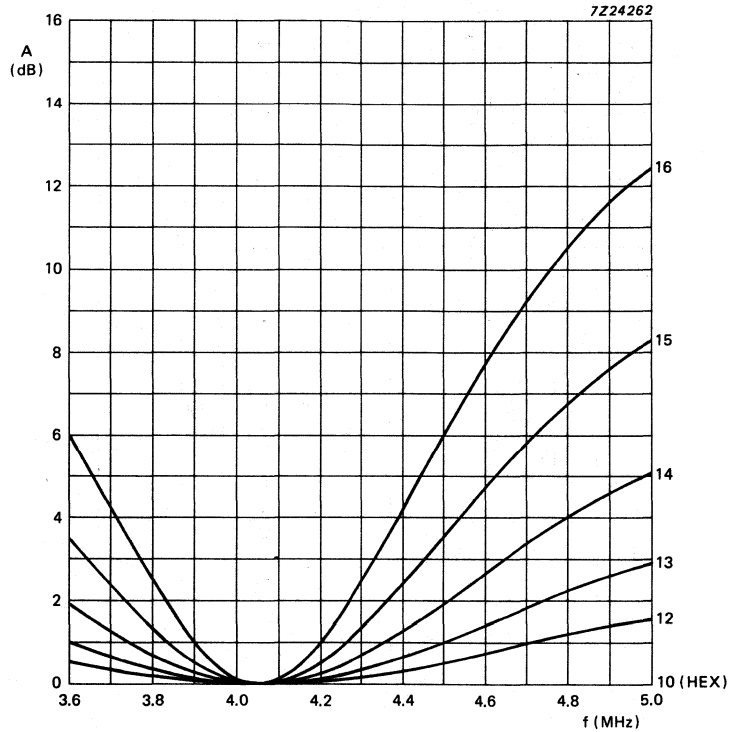


Fig. 8(b) Example of frequency response for the programmable adaptive filter; from 10 to 16 (HEX).

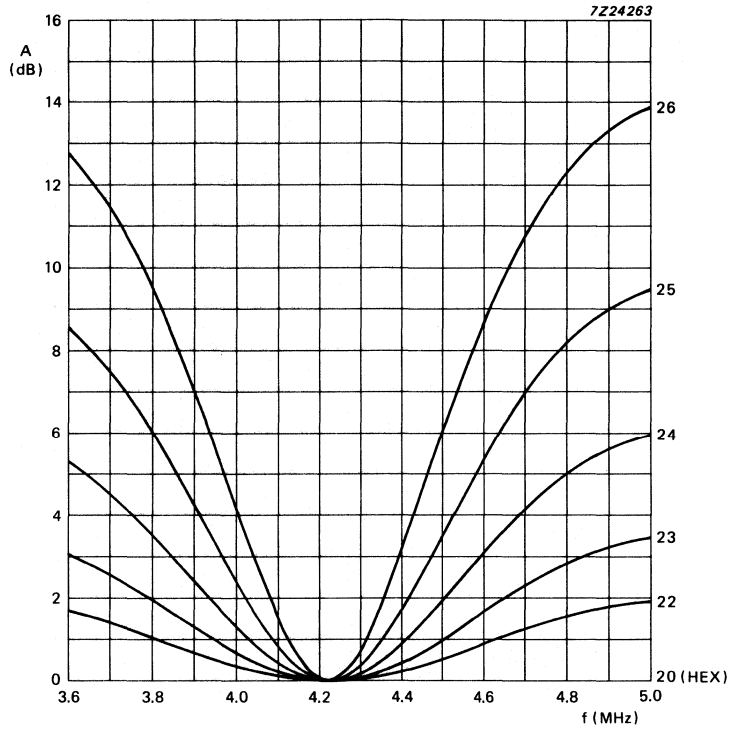


Fig. 8(c) Example of frequency response for the programmable adaptive filter; from 20 to 26 (HEX).

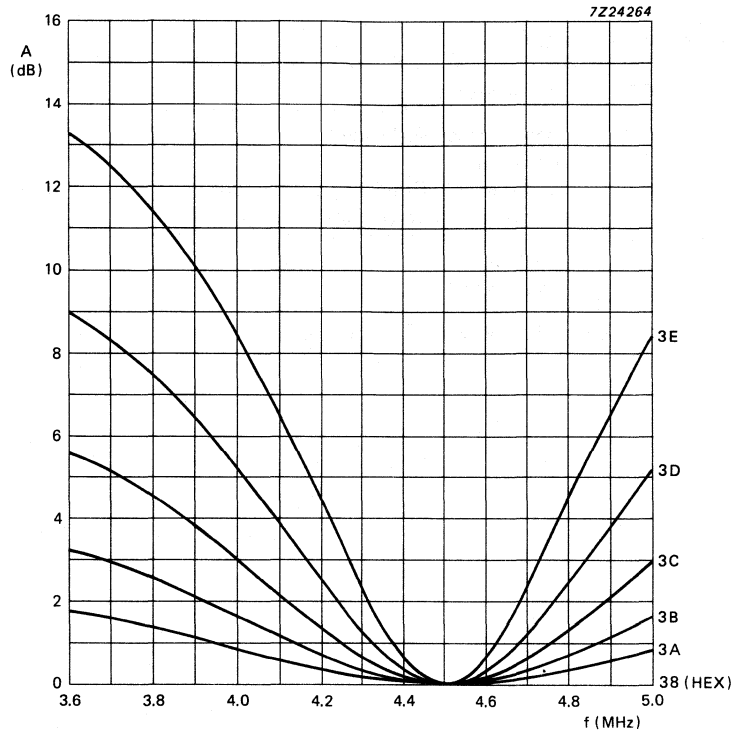


Fig. 8(d) Example of frequency response for the programmable adaptive filter; from 38 to 3E (HEX).

Subaddress 16 (HEX)

Control 3

Relevent for system configuration

C2	C1	C0	UV – output
X	0	0	high impedance (3-state)
X	0	1	active zero
X	1	0	colour enable (if CS flag then colour on)
X	1	1	colour forced on (independent of CS flag)
0	X	X	positive UV
1	X	X	negative UV

After power-on-reset the control register is set to logic 0.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	I_{max} = 20 mA	V_{DD}	−0.5	7.0	V
Voltage input		V_I	−0.5	7.0	V
Voltage output		V_O	−0.5	7.0	V
Total power dissipation		P_{tot}	−	1.2	W
Operating ambient temperature range		T_{amb}	0	70	°C
Storage temperature range		T_{stg}	−65	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 25 °C; unless otherwise specified. All voltages are referenced to ground (pins 6 and 23) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	–	5.5	V
Supply current (f_{nom})	V_{DD} = 5.5 V					
Inputs LOW; outputs with maximum load		I_{DD}	–	–	180	mA
Inputs						
Input voltage LOW (clock data) pins 2, 16, 17 to 21; and 24 to 27		V_{IL}	0	–	0.8	V
Input voltage LOW (I^2C) pins 1 and 28		V_{IL}	0	–	1.5	V
Input voltage HIGH (data) pins 2, 17 to 21; and 24 to 27		V_{IH}	2	–	V_{DD}	V
Input voltage HIGH (LL3) pin 16		V_{IH}	3.0	–	V_{DD}	V
Input voltage HIGH (I^2C) pins 1 and 28		V_{IH}	3	–	V_{DD}	V
Input leakage current pins 2, 16, 17 to 21; and 24 to 27		I_I	−10	–	10	μA
Input capacitance (data) pins 2, 18 to 21; and 24 to 27		C_I	2	–	7.5	pF
Input capacitance (clock) pin 16		C_I	15	–	40	pF
Input capacitance (reset) pin 17		C_I	2	–	10	pF
Outputs						
Output voltage LOW pins 3 to 5; 8 to 15	I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW SDA pin 1	I_{OL} = 5 mA	V_{OL}	0	–	0.45	V
Output voltage HIGH pins 3 to 5; 8 to 15	I_{OL} = −0.5 mA	V_{OH}	2.4	–	V_{DD}	V
Capacitive load of outputs in high impedance pins 12 to 15		C_Z	2	–	15	pF

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 25 °C; unless otherwise specified. All voltages are referenced to ground (pins 6 and 23) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Clock timing (LL3)						
Cycle time	note 1	t_{C3}	69	–	80	ns
Duty factor		δ	43	–	57	%
Rise time	note 2	t_r	–	–	6	ns
Fall time	note 2	t_f	–	–	6	ns
Input timing						
Data set up time		t_{SU}	12	–	–	ns
Data hold time	note 3 V_{IH}(LL3) = 4 V	t_{IH}	8	–	–	ns
Output timing						
Data load capacitance		C_L	7.5	–	25	pF
Data hold time	V_{IH}(CLK) = 3 V	t_{OH}	3	–	–	ns
Data delay time	C_L = 25 pF	t_{OD}	–	–	50	ns

Notes to the characteristics

1. Static deviation = ±4%; dynamic deviation = ±7% for signal path CVBS-DCVBS (this is required for the running-in of the DMSD sync processor).
2. The rising and falling edges of the clock signal are assumed to be smooth due to roll-off low-pass filtering.
3. Matches to SAA9050/SAA9057 for V_{IH}(LL3) ⩾ 3 V.

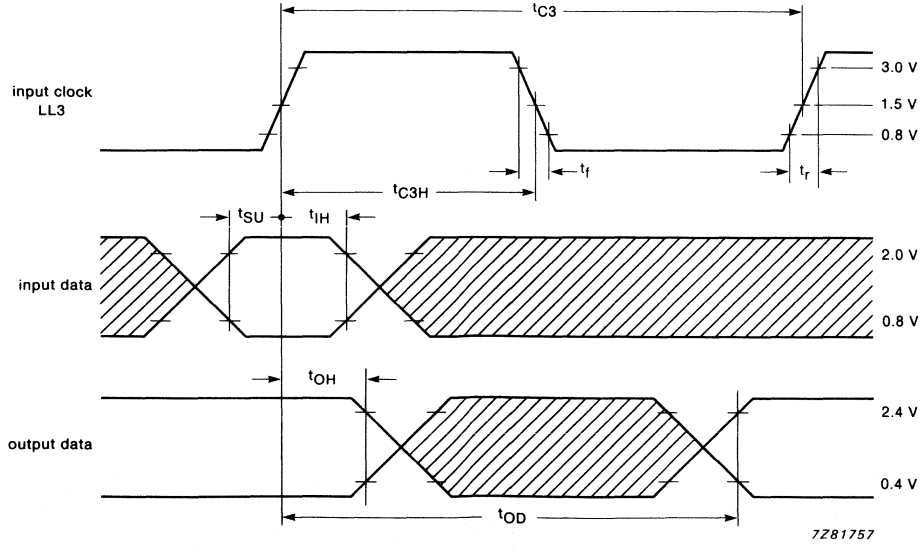


Fig. 9 Timing diagram.

PICTURE-IN-PICTURE CONTROLLER (PIPCO)

GENERAL DESCRIPTION

The SAA9068 is a controller for picture-in-picture applications. The PIPCO receives time multiplexed YUV data from an external analogue-to-digital converter (ADC) or from the Digital Vertical Filter (SAA9069). The device provides YUV data, via an internal digital-to-analogue converter (DAC), to the external filters. The device automatically detects the 50/60 Hz acquisition. Picture data is stored in an external 10 k by 8-bit SRAM. The device also produces the control signal for the SAA9069 (DVF). All features of the PIPCO are software controlled via an I^2C bus.

Features

- Automatic detection of acquisition signals
- Automatic detection of display signals
- The following features are software controlled via an I^2C bus:
  PIP ON/OFF
  border colour, one out of eight
  freeze PIP
  PIP top or bottom of screen
  PIP left or right of screen
  blank PIP
- Y-delay to compensate for delay differences in the pre-filters

QUICK REFERENCE DATA

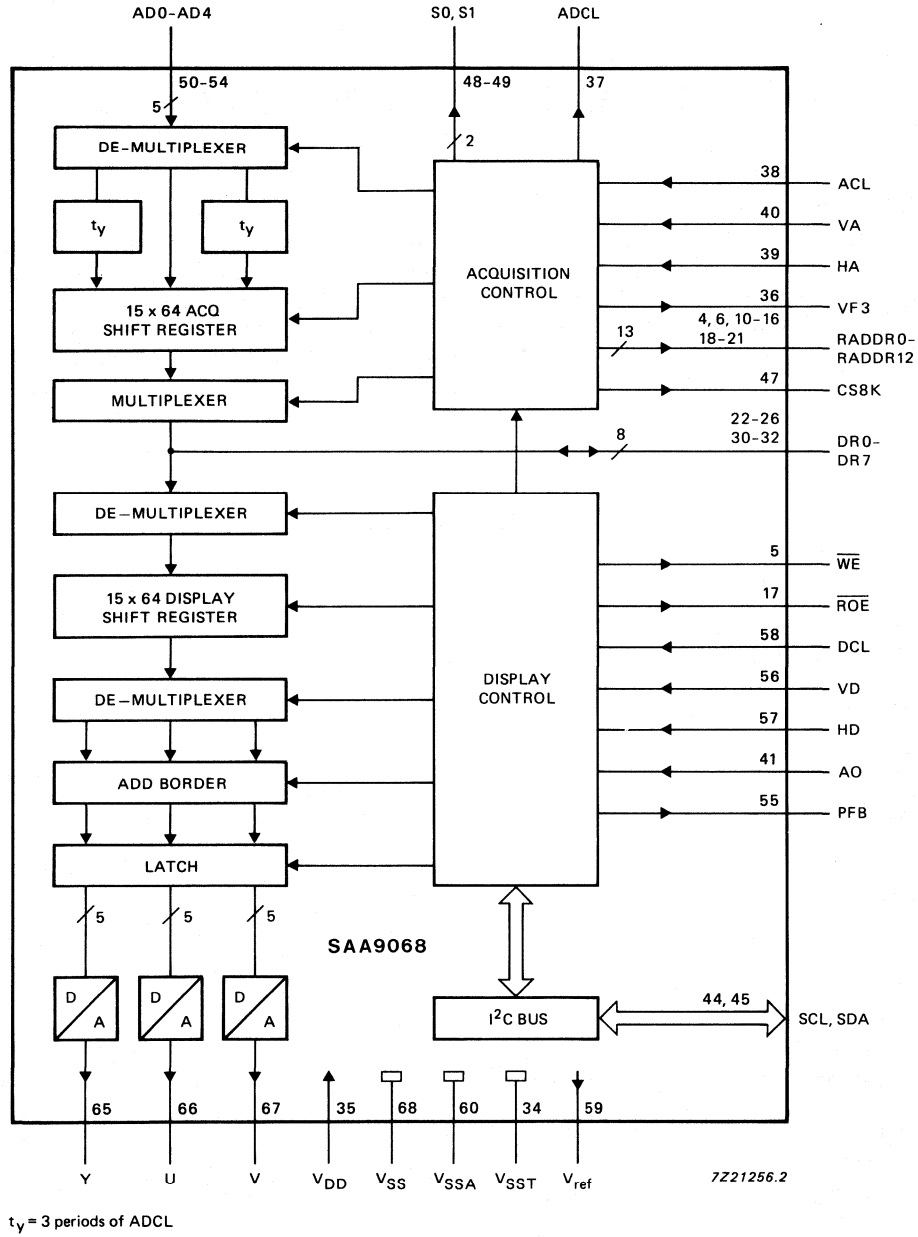
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	−0,5	–	7,0	V
Input voltage range	note 1	V_I	−0,5	–	V_{DD}+0,5	V
Maximum input current		I_{IM}	–	–	±10	mA
Maximum output current		I_{OM}	–	–	±10	mA
Inputs						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	V_{DD}	V
Input leakage current	T_{amb} = 25 °C	$\pm I_I$	–	–	1	μA
Outputs	except analogue outputs					
Output voltage LOW	I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,8 mA	V_{OH}	V_{DD}−0,4	–	V_{DD}	V

Note to the Quick Reference Data

1. V_{DD} + 0,5 V must not exceed 7,0 V

PACKAGE OUTLINE

68-lead plastic leaded chip-carrier (SOT-188)



t_y = 3 periods of ADCL

Fig. 1 Block diagram.

DEVELOPMENT DATA

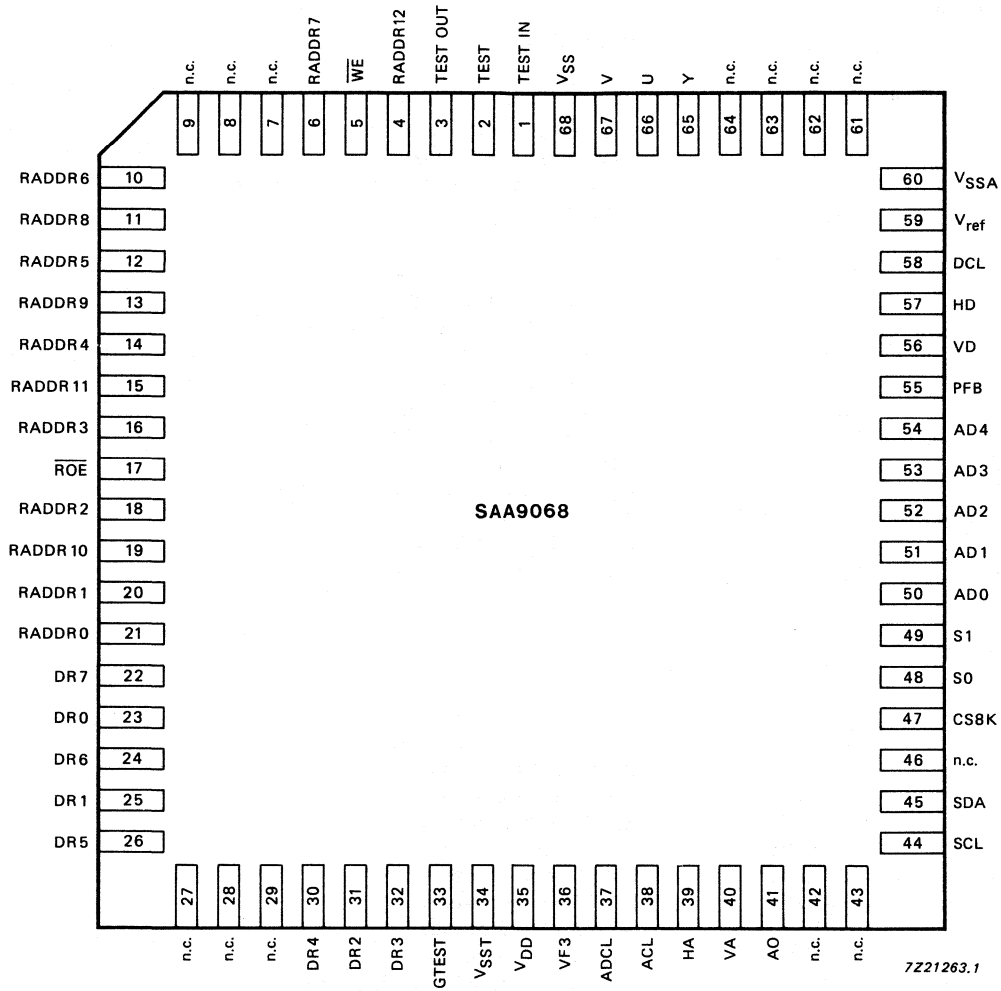


Fig. 2 Pinning diagram.

PINNING

pin	mnemonic	description
Power supplies		
34	V_{SST}	ground for dynamic shift registers
35	V_{DD}	positive supply voltage
60	V_{SSA}	ground for digital-to-analogue converters
68	V_{SS}	ground (0 V)
Inputs		
1	TEST IN	data input for testing the DAC
2	TEST	when HIGH, test mode for DAC enabled
33	GTEST	when LOW GTEST returns all memory elements to a known state, except for line memories
38	ACL	acquisition clock, typ. 10,9 MHz
39	HA	start of line in acquisition mode
40	VA	start of field in acquisition mode
41	A0	programming of I^2C bus slave address
50 to 54	AD0 to AD4	YUV data stream from ADC or SAA9069
56	VD	start of field in display mode
57	HD	start of line in display mode
58	DCL	display clock, typ. 15,8 MHz
Outputs		
3	TEST OUT	test data to DAC
4	RADDR12	SRAM address output
5	$\overline{WE}$	write enable (active LOW)
6	RADDR7	SRAM address output
10	RADDR6	SRAM address output
11	RADDR8	SRAM address output
12	RADDR5	SRAM address output
13	RADDR9	SRAM address output
14	RADDR4	SRAM address output
15	RADDR11	SRAM address output
16	RADDR3	SRAM address output
17	$\overline{ROE}$	RAM output enable (active LOW)
18	RADDR2	SRAM address output
19	RADDR10	SRAM address output
20	RADDR1	SRAM address output
21	RADDR0	SRAM address output
36	VF3	line selection to SAA9069
37	ADCL	acquisition clock signal (ACL/2) to ADC or SAA9069
47	CS8k	chip select for 8 k SRAM
48 to 49	S0 and S1	Y, U and V selection signal to analogue switch or SAA9069
55	PFB	picture-in-picture fast blanking
Inputs/outputs		
22 to 26, 30 to 32	DR0 to DR7	data to and from SRAM
44	SCL	I^2C bus clock
45	SDA	I^2C bus data signals

Analogue outputs

59	V_{ref}	voltage reference level for DAC
65	Y	analogue video signal from 5-bit DAC
66	U	analogue video signal from 5-bit DAC
67	V	analogue video signal from 5-bit DAC

Others

7 to 9, 27 to 29, 42, 43, 62 to 64	n.c.	not internally connected

FUNCTIONAL DESCRIPTION (see Fig. 1)

The YUV data stream is converted from analogue-to-digital data by the 5-bit ADC, this data is then stored in an acquisition line memory every third line. When enabled by the display section of the PIPCO, the data is transferred to the external SRAM. Data from the SRAM is transferred to the display line memory after which it is converted from digital to analogue by the DAC.

I²C bus (SDA; SCL)

The I²C bus provides bidirectional 2-line communication between different ICs or modules. The SDA is the serial data line; SCL is the serial clock line. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C bus format (slave address and receiver formats)

All 8 bits of the subaddress have to be decoded by the device. After power-on reset all control bits are set to zero. This device does not respond to the general call address.

0	0	1	0	0	1	A0	0

Fig. 3 Slave address.

DETAILED INFORMATION ON I²C BUS SPECIFICATION IS AVAILABLE ON REQUEST.

Table 1 Data byte format

	function							
	D7	D6	D5	D4	D3	D2	D1	D0
control	PIPON	STILL	BLPIP	TOP	LEFT	BOC2	BOC1	BOC0

Table 2 Definition of bits D7 to D3

bit	definition
PIPON	PIPON = 1, picture-in-picture is ON PIPON = 0, picture-in-picture is OFF
STILL	STILL = 1, still picture-in-picture STILL = 0, moving picture-in-picture
BLPIP	BLPIP = 1, blanking of picture-in-picture BLPIP = 0, display picture-in-picture
TOP	TOP = 1, picture-in-picture in upper part of screen TOP = 0, picture-in-picture in lower part of screen
LEFT	LEFT = 1, picture-in-picture in left part of screen LEFT = 0, picture-in-picture in right part of screen

Table 3 Colour reproduction

colour	BOC2	BOC1	BOC0	−U	−V
dark pink	0	0	0	0,00	−0,50
reddish brown	0	0	1	0,25	−0,50
light brown	0	1	0	0,50	−0,50
light purple	0	1	1	−0,25	−0,50
dark grey	1	0	0	0,00	0,00
dark green	1	0	1	0,25	0,00
green	1	1	0	0,50	0,00
medium blue	1	1	1	−0,20	0,00

If a function is not implemented, the bit related to this function is transmitted as a logic 0 and the general call address is not accepted. If no supply voltage is present, inputs SCL and SDA are in a high ohmic state.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	7,0	V
Input voltage range	note 1	V_I	−0,5	V_{DD}+0,5	V
Input current		I_I	−	±10	mA
Output current		I_O	−	±10	mA
Supply current in V_{SS}		I_{SS}	−	60	mA
Supply current in V_{DD}		I_{DD}	−	60	mA
Power dissipation per output		P	−	40	mW
Total power dissipation		P_{tot}	−	300	mW
Storage temperature range		T_{stg}	−55	+ 150	°C
Operating ambient temperature range		T_{amb}	−25	+ 70	°C

Note

1. V_{DD}+0,5 must not exceed 7,0 V.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 5 V ± 5%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply current						
Quiescent current	T_{amb} = 25 °C; all inputs to V_{DD} or V_{SS}	I_{DD}	–	–	175	μA
Inputs						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	V_{DD}	V
Input leakage current	T_{amb} = 25 °C; except GTEST	$\pm I_I$	–	–	1	μA
Input leakage current	GTEST	$\pm I_I$	–	–	30	μA
Outputs	except analogue outputs					
Output voltage LOW	I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,8 mA	V_{OH}	V_{DD}–0,4	–	V_{DD}	V
Analogue outputs	Y, U, V at output load = 22 kΩ					
Output voltage LOW		V_{OL}	0,80	–	1,45	V
Output voltage HIGH		V_{OH}	3,75	–	4,75	V
Output level n+1 (step)	note 1	V_n	level n	level n + V_s	level n + $2V_s$	V
Output voltage HIGH to output voltage LOW with 1 kΩ load		V_{OH}-V_{OL}	1,75	1,95	2,15	V
Voltage reference						
Output voltage	V_{DD} = 5 V	V_O	0,7	–	1,3	V

Note to the DC characteristics

1. $V_s = \frac{V_{OH}-V_{OL}}{31}$

AC CHARACTERISTICS

V_{DD} = 5 V ± 5%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance		C_i	–	–	3	pF
AD0 - AD4 to ACL	Fig. 8					
data set-up time		$t_{SU;DAT}$	30	–	–	ns
data hold time		$t_{HD;DAT}$	10	–	–	ns
DR0 - DR7 to DCL	Fig. 7					
data set-up time		$t_{SU;DAT}$	30	–	–	ns
data hold time		$t_{HD;DAT}$	10	–	–	ns
HA, HD, VA, VD	notes 1 to 4					
ACL	note 5					
pulse width LOW		t_{WL}	25	–	–	ns
pulse width HIGH		t_{WH}	25	–	–	ns
rise time		t_r	–	–	7	ns
fall time		t_f	–	–	7	ns
frequency		f_{ACL}	–	10,9	–	MHz
DCL	note 6					
pulse width LOW		t_{WL}	18	–	–	ns
pulse width HIGH		t_{WH}	18	–	–	ns
rise time		t_r	–	–	4	ns
fall time		t_f	–	–	4	ns
frequency		f_{DCL}	–	15,8	–	MHz
Outputs	DCL = 15,8 MHz					
Load capacitance		C_L	–	–	20	pF
DCL to DR0 - DR7 propagation delay	Fig. 6	t_d	10	–	135	ns
DCL to RADDR0 - RADDR12 and CS8K propagation delay	Fig. 6	t_d	0	–	70	ns
DCL to $\overline{ROE}$ propagation delay	Fig. 6	t_d	0	–	150	ns
DCL to $\overline{WE}$ (falling edge) propagation delay	Fig. 6	t_d	70	–	105	ns
DCL to $\overline{WE}$ (rising edge) propagation delay	Fig. 6	t_d	195	–	235	ns
DCL to PFB propagation delay	Fig. 7	t_d	0	–	50	ns
ACL to ADCL propagation delay	Fig. 8	t_d	0	–	115	ns
ACL to S0 and S1 propagation delay	Fig. 8	t_d	0	–	115	ns

Notes to the AC characteristics

1. Pulse width HA (typ. 250 ns): the first sample of a line occurs after approximately 124 periods of ACL (counted on the negative edge of HA). The internal horizontal acquisition off-set value is chosen in such a way that ACL = 10,9 MHz, when this condition is satisfied the acquired picture is centralized within the PIP. The off-set value is dependent upon the acquisition frequency, 50 Hz or 60 Hz (124 ACL periods of 50 Hz and 108 ACL periods of 60 Hz). If the pulse width of HA increases, the acquired picture will shift to the left within the PIP picture (see Fig. 4).

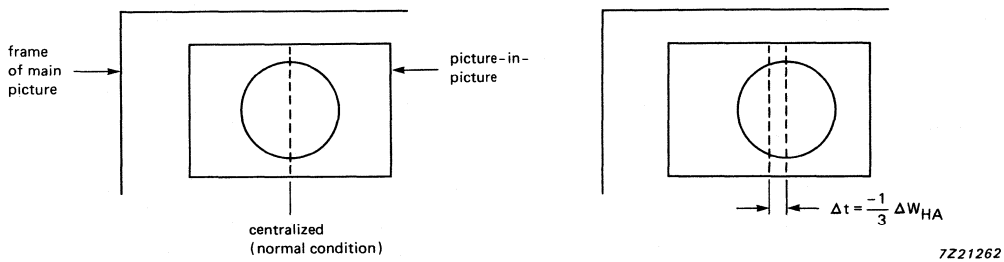


Fig. 4 PIP position; (a) ACL = 10,9 MHz, (b) $\Delta t = -1/3\ \Delta W_{HA}$.

2. Pulse width HD (typ. 250 ns): the first sample of a line is displayed after XXX periods of DCL with respect to the negative edge of HD. The internal horizontal display off-set is fixed in the hardware and depends upon the frequency (50 Hz or 60 Hz) and the right/left position of the display.
   The following values are implemented:

   - 50 Hz; position of display, right; t = 574 periods of DCL
   - 50 Hz; position of display, left; t = 134 periods of DCL
   - 60 Hz; position of display, right; t = 558 periods of DCL
   - 60 Hz; position of display, left; t = 126 periods of DCL

   If the pulse width of HD increases the distance between screen border and the left border of the PIP will enlarge and the picture will shift to the right. The width of the complete PIP, inclusive of border, is 268 clock pulses.

3. VA pulse width, minimum 8 pulses of ACL.

4. VD pulse width, minimum 5 pulses of DCL.

DEVELOPMENT DATA

5. If ACL = k x 10,9 MHz, the effects are shown in Fig. 5:
   - if $k > 1$ then the acquired picture will be expanded horizontally and its centre will shift to the right.
   - if $k < 1$ then the acquired picture will be reduced horizontally and its center will shift to the left.

(a) (b)

Fig. 5 PIP geometry; (a) $k > 1$, (b) $k < 1$.

6. DCL: if DCL $\neq$ 15,8 MHz but DCL = k x 15,8 MHz the effects are:
   - all horizontal sizes and values are multiplied by k.

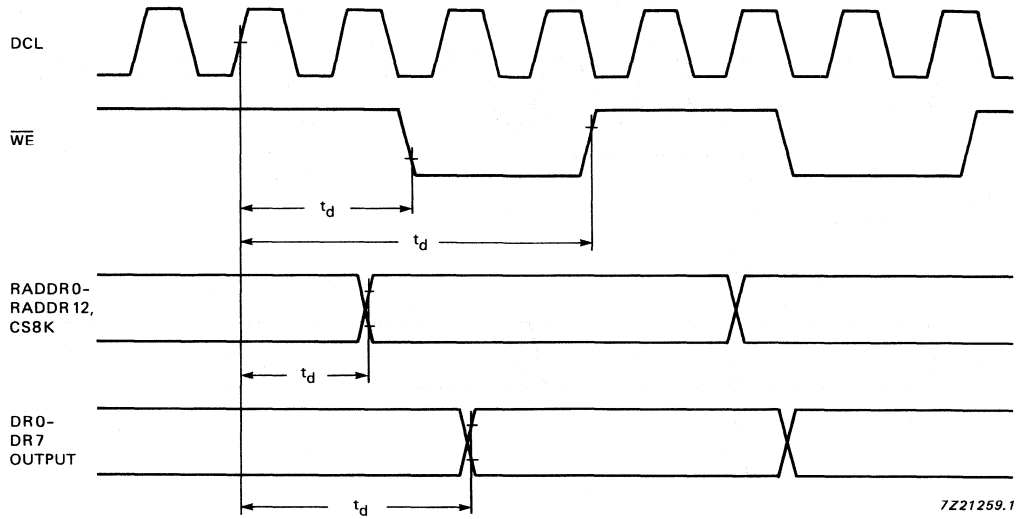


Fig. 6 Data and display clock timing waveform.

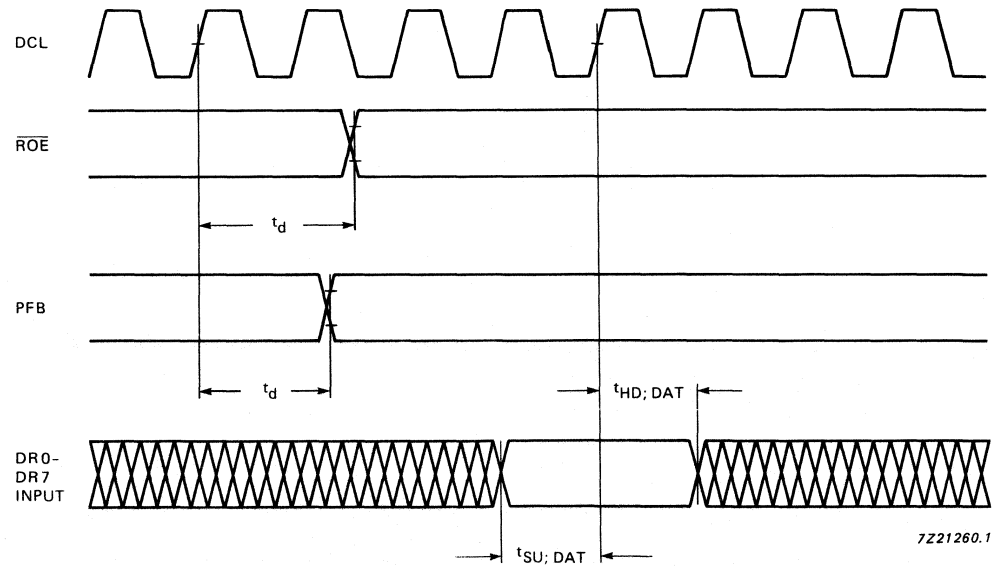


Fig. 7 Data and display clock timing waveform.

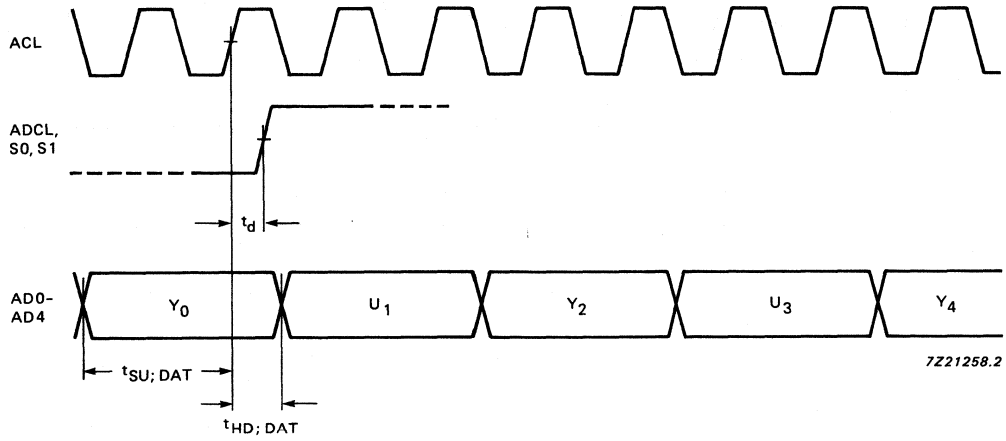


Fig. 8 Input data and acquisition clock waveform.

APPLICATION INFORMATION

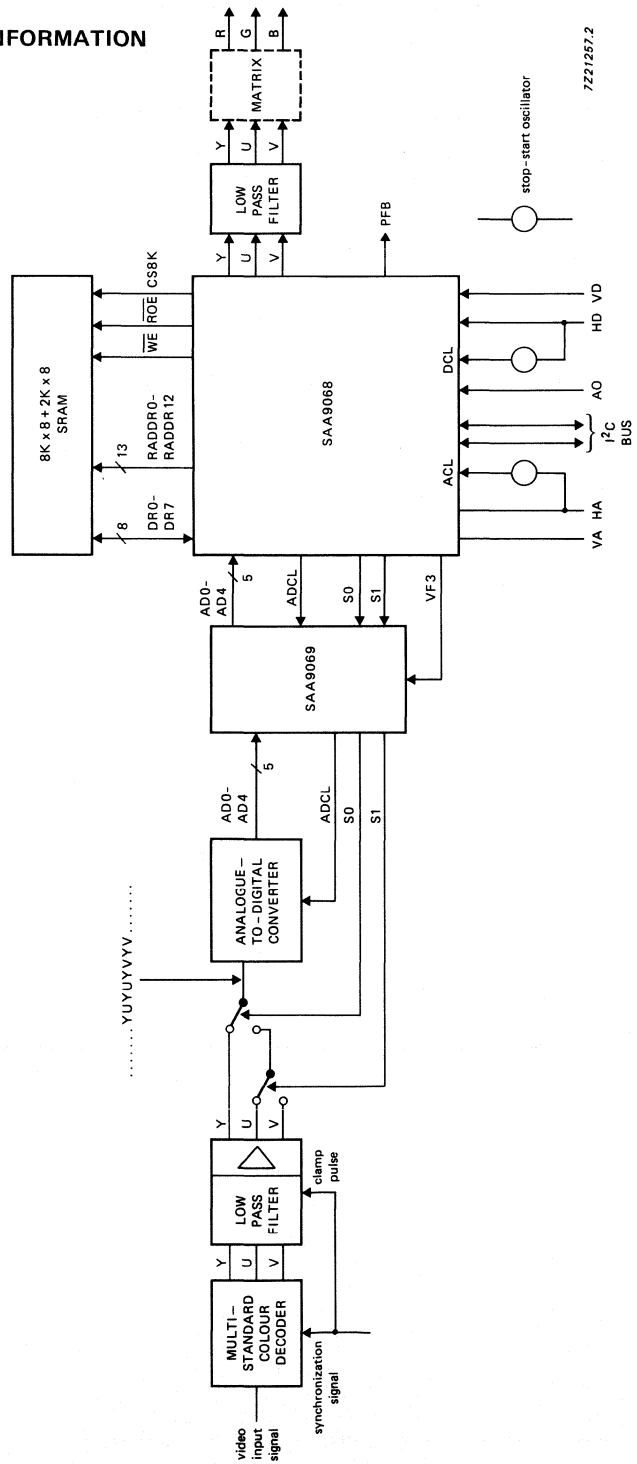


Fig. 9 Application diagram, using SAA9069.

DEVELOPMENT DATA

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3035 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 8 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 8 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 16)	V_{P1}	typ.	12 V
(pin 22)	V_{P2}	typ.	13 V
(pin 17)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 16)	I_{P1}	typ.	32 mA
(pin 22)	I_{P2}	typ.	0,1 mA
(pin 17)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	400 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

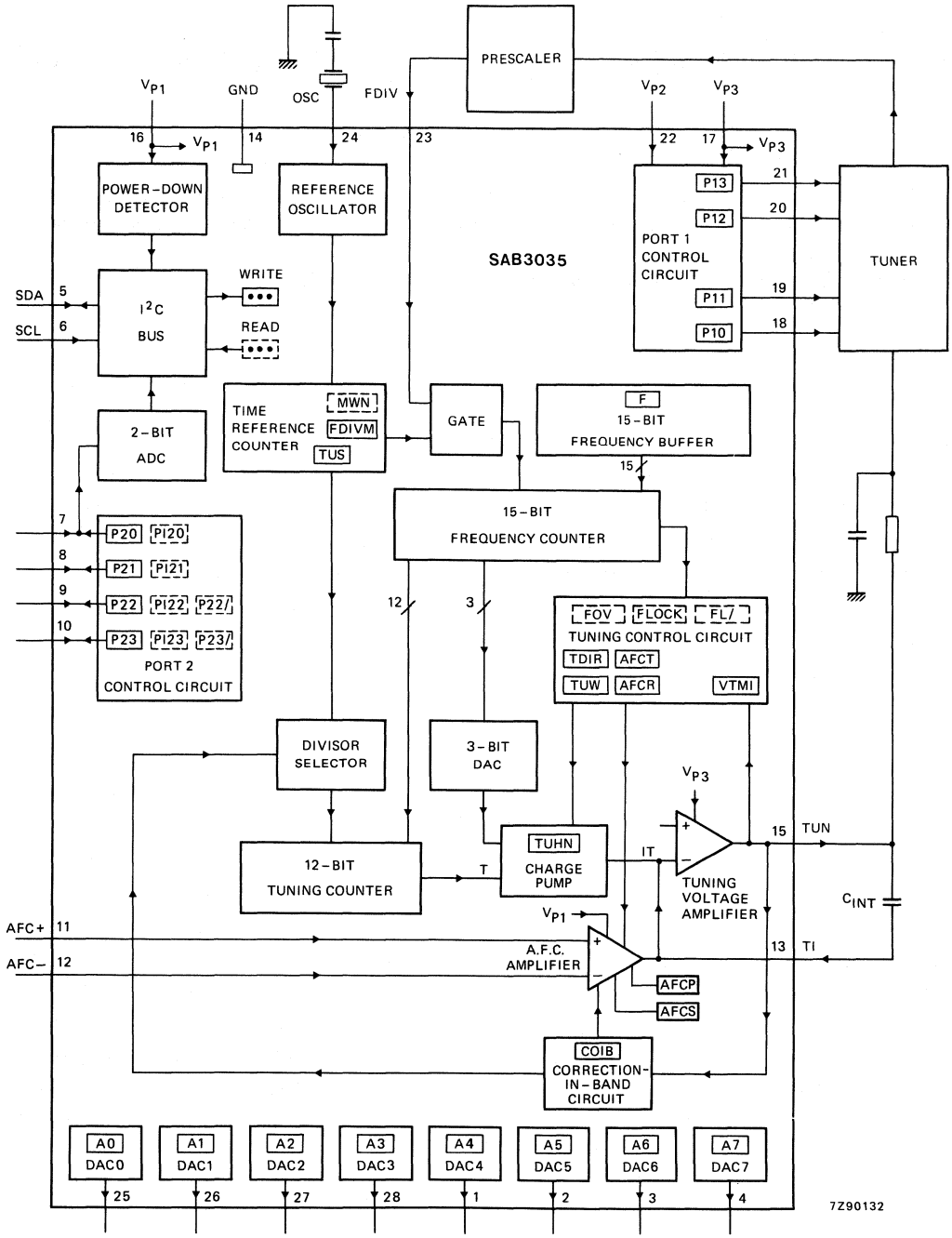


Fig. 1 Block diagram.

DEVELOPMENT DATA

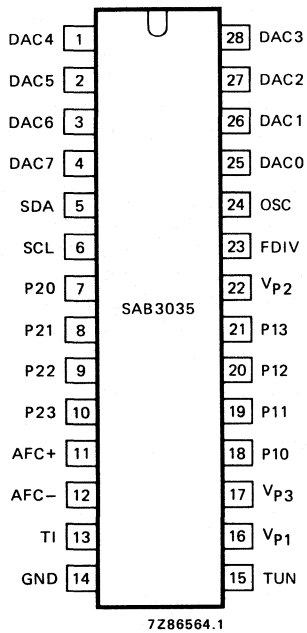


Fig. 2 Pinning diagram.

PINNING

1	DAC4	outputs of static DACs
2	DAC5	
3	DAC6	
4	DAC7	
5	SDA	serial data line (I^2C bus)
6	SCL	serial clock line (I^2C bus)
7	P20	general purpose input/output ports
8	P21	
9	P22	
10	P23	
11	AFC+	a.f.c. inputs
12	AFC−	
13	TI	tuning voltage amplifier inverting input
14	GND	ground
15	TUN	tuning voltage amplifier output
16	V_{P1}	+12 V supply voltage
17	V_{P3}	+32 V supply for tuning voltage amplifier
18	P10	High-current band-selection output ports
19	P11	
20	P12	
21	P13	
22	V_{P2}	positive supply for high-current band-selection output circuits
23	FDIV	input from prescaler
24	OSC	crystal oscillator input
25	DAC0	outputs of static DACs
26	DAC1	
27	DAC2	
28	DAC3	

FUNCTIONAL DESCRIPTION

The SAB3035 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50$ kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50$ kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Eight 6-bit digital-to-analogue converters DAC0 to DAC7 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

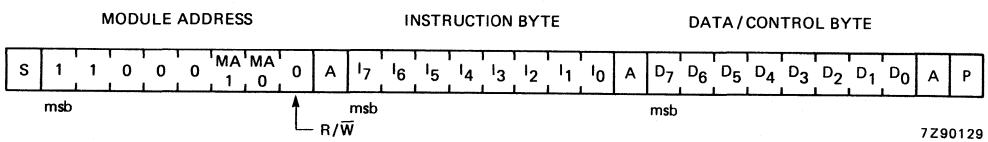


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

DEVELOPMENT DATA

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X2, X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

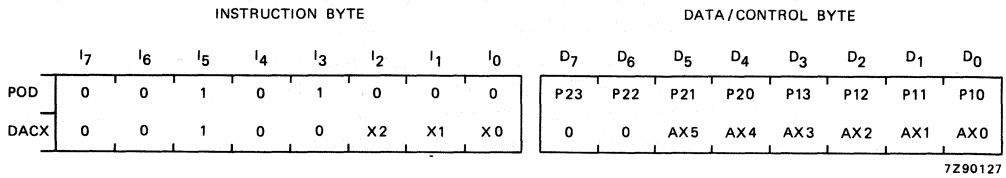


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

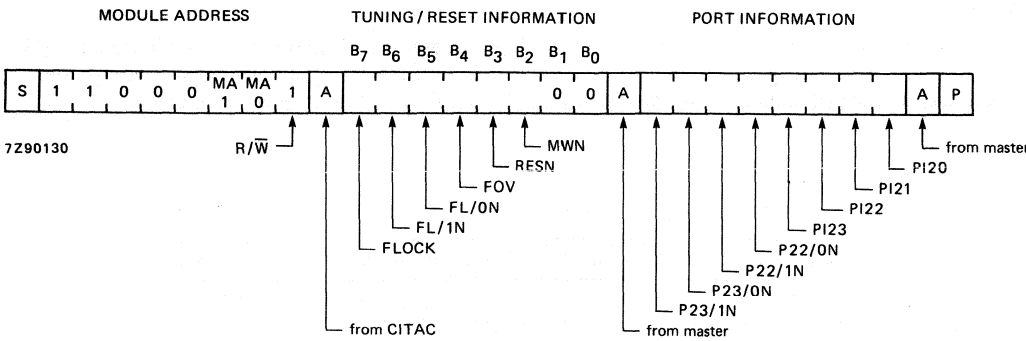


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

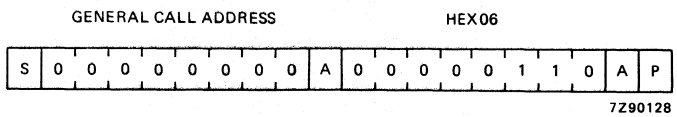


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 16)	V_{P1}	−0,3 to +18	V
(pin 22)	V_{P2}	−0,3 to +18	V
(pin 17)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 5)	V_{SDA}	−0,3 to +18	V
(pin 6)	V_{SCL}	−0,3 to +18	V
(pins 7 to 10)	V_{P2X}	−0,3 to +18	V
(pins 11 and 12)	$V_{AFC+, AFC-}$	−0,3 to V_{P1}*	V
(pin 13)	V_{TI}	−0,3 to V_{P1}*	V
(pin 15)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 18 to 21)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 23)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 24)	V_{OSC}	−0,3 to +5	V
(pins 1 to 4 and 25 to 28)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

DEVELOPMENT DATA

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	20	32	50	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	−2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	400	–	mW
Operating ambient temperature	T_{amb}	−20	–	+70	°C
I^2C bus inputs/outputs					
SDA input (pin 5); SCL input (pin 6)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 5, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 7 to 10, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 11, 12)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 13, 15)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 18 to 21)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 23)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 7 (pins 25 to 28 and 1 to 4)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 7) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

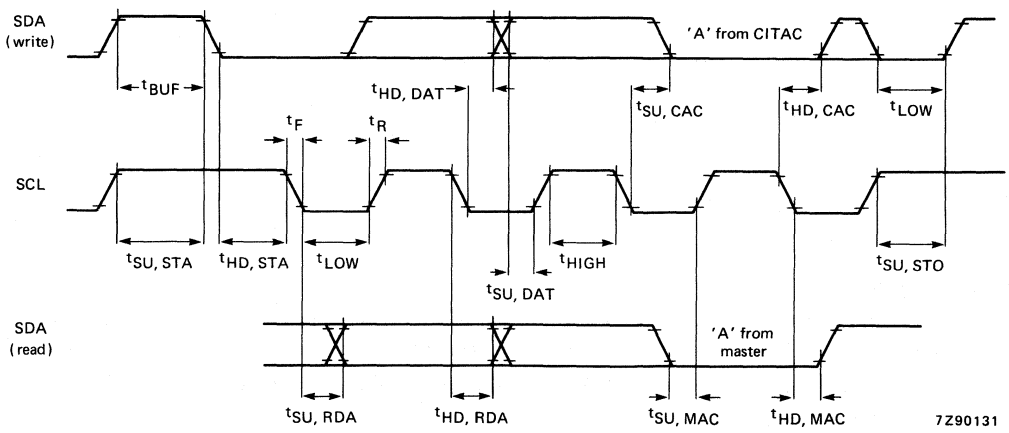


Fig. 8 I²C bus timing SAB3035.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3036 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 5)	V_{P1}	typ.	12 V
(pin 14)	V_{P2}	typ.	13 V
(pin 9)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 5)	I_{P1}	typ.	23 mA
(pin 14)	I_{P2}	typ.	0,1 mA
(pin 9)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	300 mW
Operating ambient temperature range	T_{amb}		−20 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

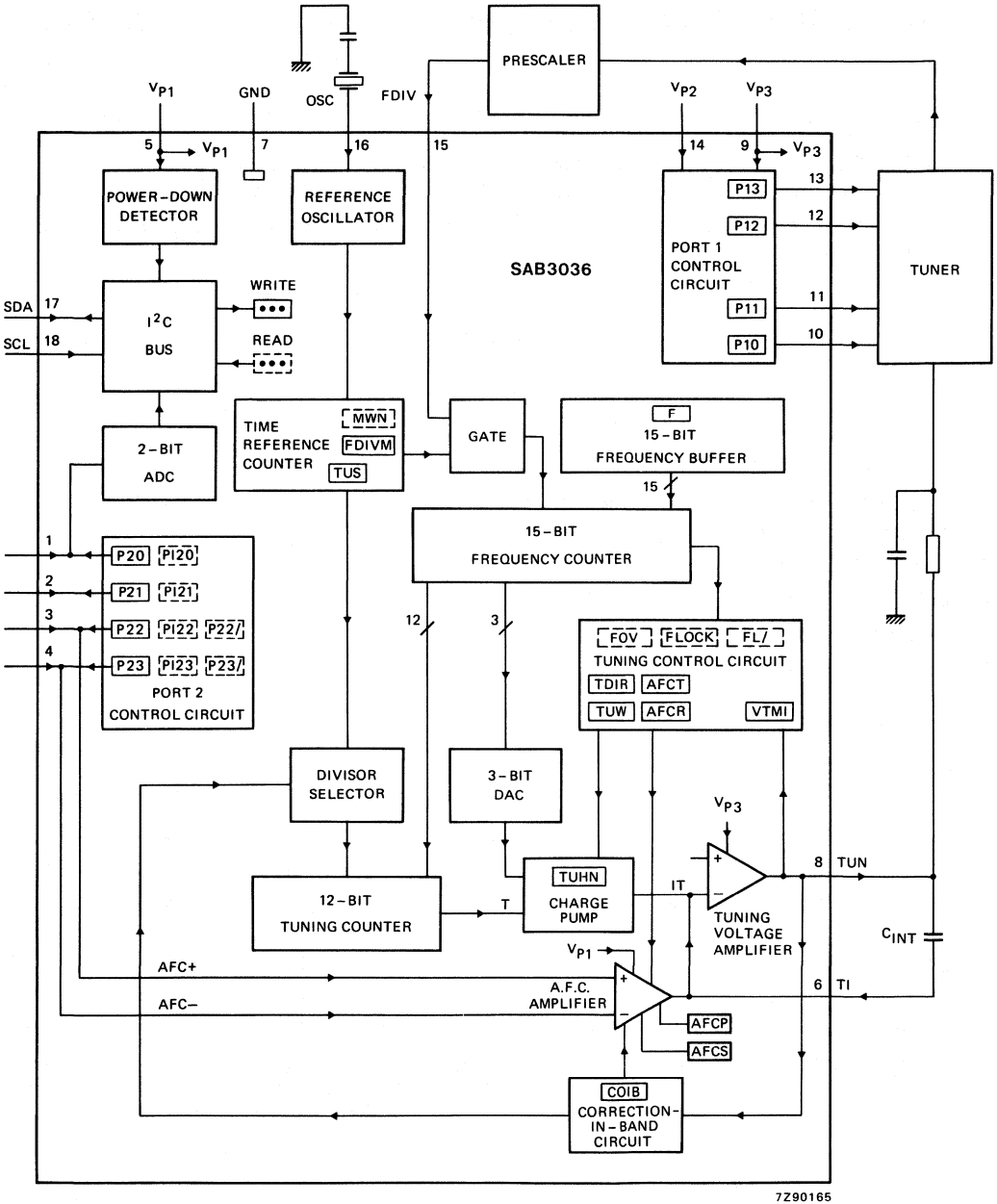


Fig. 1 Block diagram.

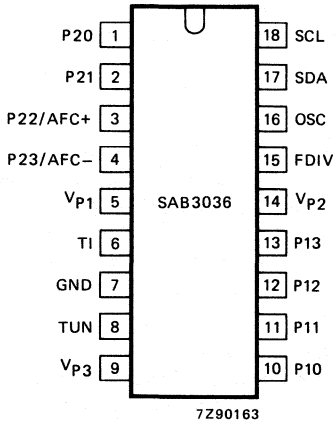


Fig. 2 Pinning diagram.

PINNING

1	P20	general purpose input/output ports
2	P21	
3	P22/AFC+	general purpose input/output ports and a.f.c. inputs
4	P23/AFC−	
5	V_{P1}	+ 12 V supply voltage
6	TI	tuning voltage amplifier inverting input
7	GND	ground
8	TUN	tuning voltage amplifier output
9	V_{P3}	+ 32 V supply for tuning voltage amplifier
10	P10	high-current band-selection output ports
11	P11	
12	P12	
13	P13	
14	V_{P2}	positive supply for high-current band-selection output circuits
15	FDIV	input from prescaler
16	OSC	crystal oscillator input
17	SDA	serial data line, I^2C bus
18	SCL	serial clock line, I^2C bus

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The SAB3036 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals and are connected with the AFC+ and AFC− inputs respectively. The a.f.c. amplifier must be switched off when P22 and/or P23 are used. When a.f.c. is used, P22 and P23 must be programmed HIGH (high impedance state). With the aid of port P20, up to three independent module addresses can be programmed.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

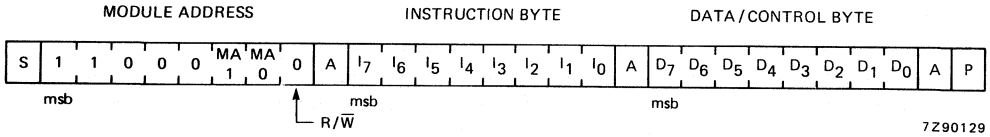


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

OPERATION (continued)

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at $\Delta f = 50$ kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

$\Delta f = 50$ kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at $C_{INT} = 1\,\mu F$ mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

DEVELOPMENT DATA

OPERATION (continued)

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction byte POD (port output data) is shown in Fig. 5, together with the corresponding data/control byte. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

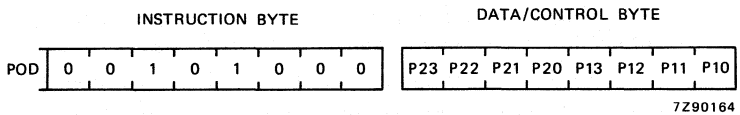


Fig. 5 Control programming.

OPERATION (continued)

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

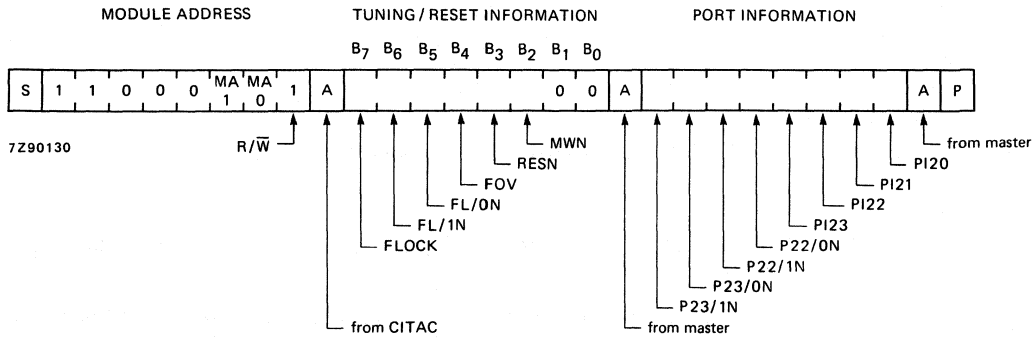


Fig. 6 Information byte format.

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

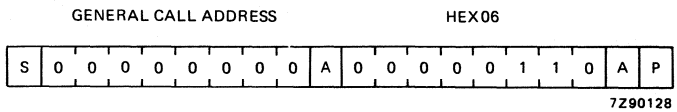


Fig. 7 Reset programming.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:		
(pin 5)	V_{P1}	−0,3 to + 18 V
(pin 14)	V_{P2}	−0,3 to + 18 V
(pin 9)	V_{P3}	−0,3 to + 36 V
Input/output voltage ranges:		
(pin 17)	V_{SDA}	−0,3 to + 18 V
(pin 18)	V_{SCL}	−0,3 to + 18 V
(pins 1 and 2)	$V_{P20, P21}$	−0,3 to + 18 V
(pins 3 and 4)	$V_{P22, P23, AFC}$	−0,3 to V_{P1}* V
(pin 6)	V_{TI}	−0,3 to V_{P1}* V
(pin 8)	V_{TUN}	−0,3 to V_{P3}* V
(pins 10 to 13)	V_{P1X}	−0,3 to V_{P2}** V
(pin 15)	V_{FDIV}	−0,3 to V_{P1}* V
(pin 16)	V_{OSC}	−0,3 to + 5 V
Total power dissipation	P_{tot}	max. 1000 mW
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature	T_{amb}	−20 to + 70 °C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.
** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	14	23	40	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	300	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 17); SCL input (pin 18)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 17, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 1 to 4, open collector)					
Input voltage HIGH (P20, P21)	V_{IH}	2	–	16	V
Input voltage HIGH (P22, P23) AFC switched off	V_{IH}	2	–	$V_{P1}-2$	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 3, 4)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current (P22 and P23 programmed HIGH)	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 6, 8)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter		symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)						
Minimum charge IT to tuning voltage amplifier						
TUHN1	TUHN0					
0	0	CH_{00}	0,4	1	1,7	μA μs
0	1	CH_{01}	4	8	14	μA μs
1	0	CH_{10}	15	30	48	μA μs
1	1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used		ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier						
TUHN1	TUHN0					
0	0	I_{T00}	1,7	3,5	5,1	μA
0	1	I_{T01}	15	29	41	μA
1	0	I_{T10}	65	110	160	μA
1	1	I_{T11}	530	875	1220	μA
Correction-in-band						
Tolerance of correction-in-band levels 12 V, 18 V and 24 V		ΔV_{CIB}	−15	–	+15	%
Band-select output ports						
P10, P11, P12, P13 (pins 10 to 13)						
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)		V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA		V_{OL}	–	–	0,4	V
Maximum output source current (note 3)		$-I_{OH}$	–	130	200	mA
Maximum output sink current		I_{OL}	–	5	–	mA
FDIV input (pin 15)						
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)		$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle		–	40	–	60	%
Maximum input frequency		f_{max}	16	–	–	MHz
Input impedance		Z_i	–	8	–	kΩ
Input capacitance		C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 1) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

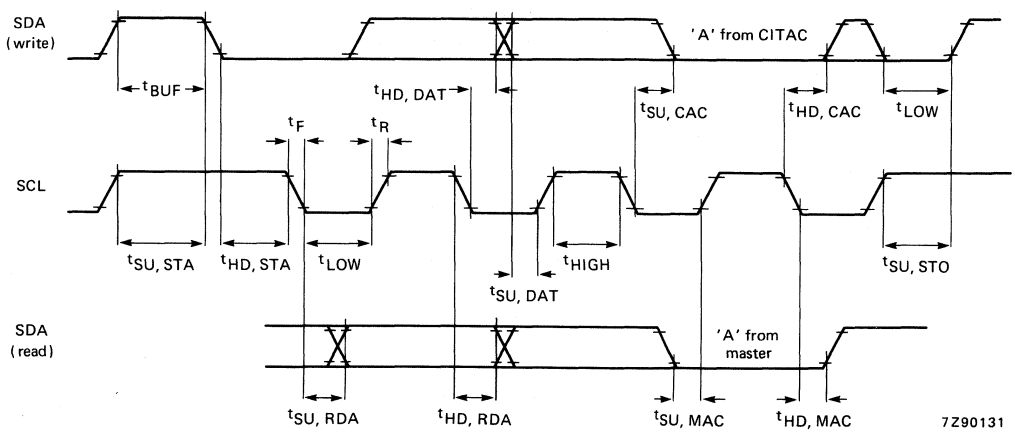


Fig. 8 I²C bus timing SAB3036.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 4 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 4 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 13)	V_{P1}	typ.	12 V
(pin 19)	V_{P2}	typ.	13 V
(pin 14)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 13)	I_{P1}	typ.	30 mA
(pin 19)	I_{P2}	typ.	0,1 mA
(pin 14)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	380 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

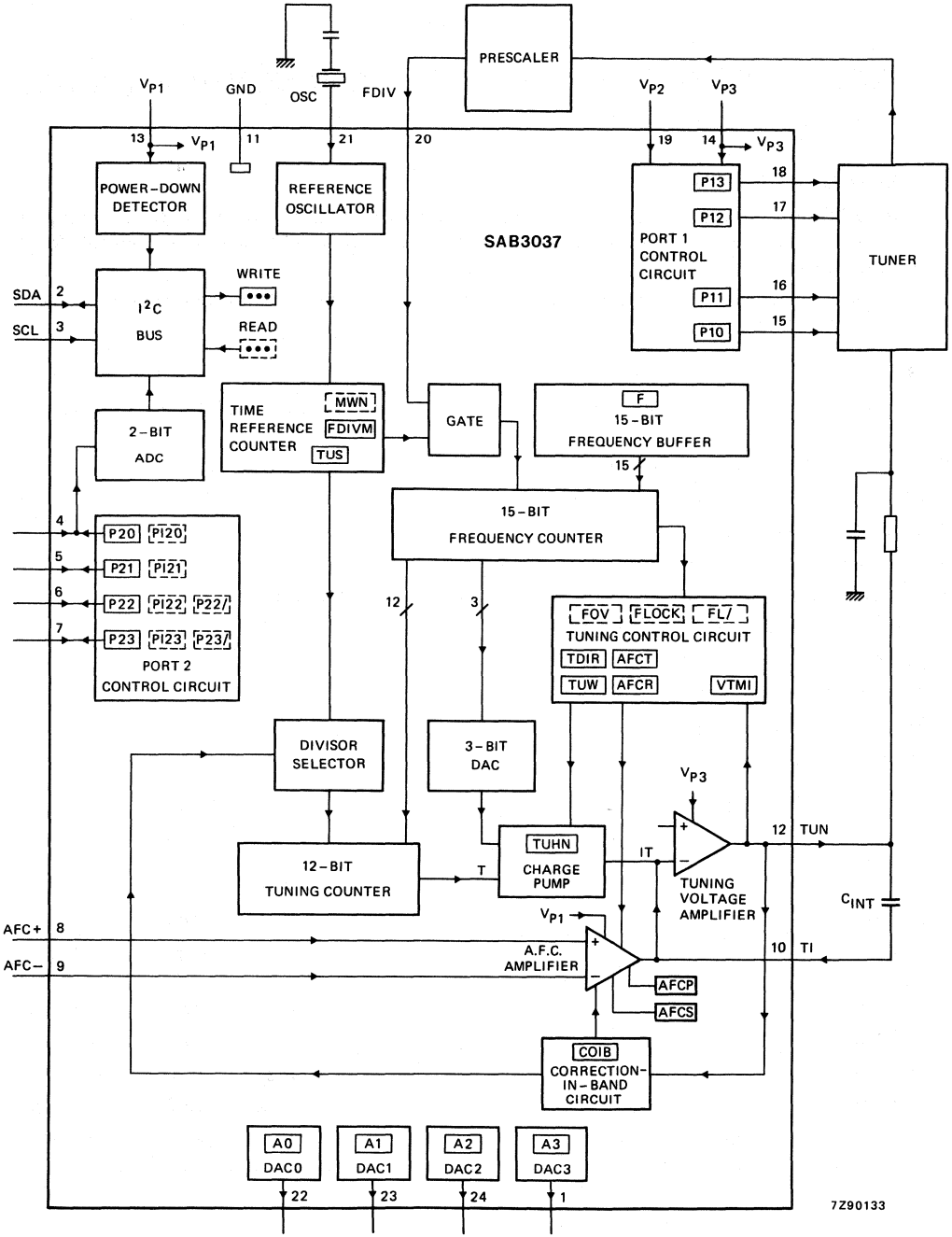


Fig. 1 Block diagram.

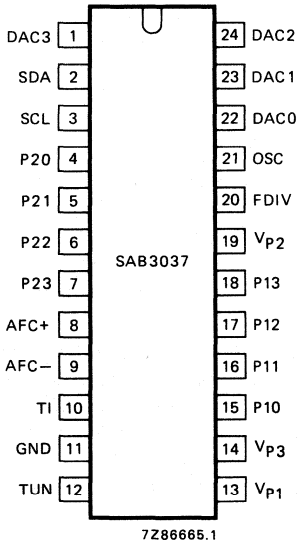


Fig. 2 Pinning diagram.

PINNING

1	DAC3	output of static DAC
2	SDA	serial data line (I²C bus)
3	SCL	serial clock line (I²C bus)
4	P20	general purpose input/output ports
5	P21	general purpose input/output ports
6	P22	general purpose input/output ports
7	P23	general purpose input/output ports
8	AFC+	a.f.c. inputs
9	AFC−	a.f.c. inputs
10	TI	tuning voltage amplifier inverting input
11	GND	ground
12	TUN	tuning voltage amplifier output
13	V_{P1}	+ 12 V supply voltage
14	V_{P3}	+ 32 V supply for tuning voltage amplifier
15	P10	high-current band-selection output ports
16	P11	high-current band-selection output ports
17	P12	high-current band-selection output ports
18	P13	high-current band-selection output ports
19	V_{P2}	positive supply for high-current band-selection output circuits
20	FDIV	input from prescaler
21	OSC	crystal oscillator input
22	DAC0	outputs of static DACs
23	DAC1	outputs of static DACs
24	DAC2	outputs of static DACs

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analogue converters DAC0 to DAC3 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

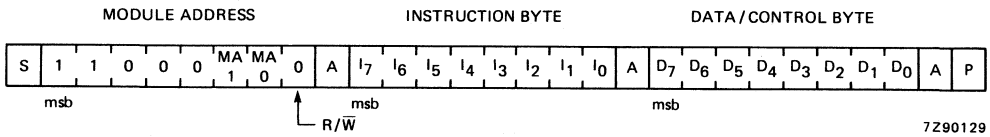


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

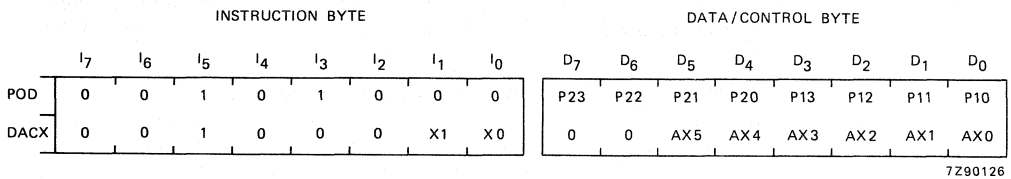


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

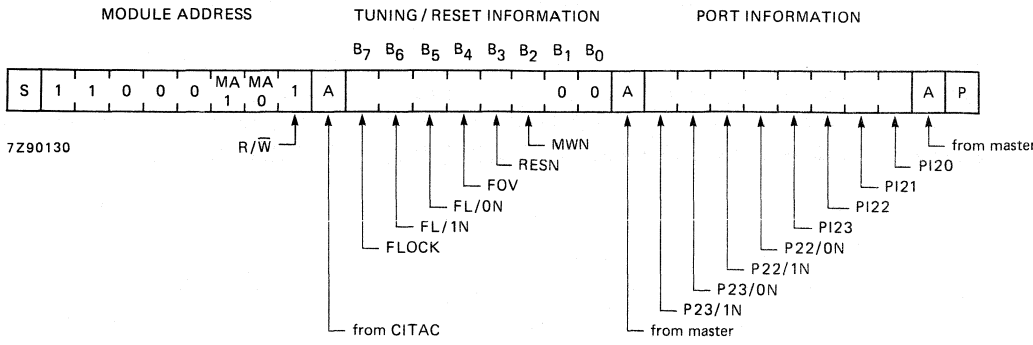


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

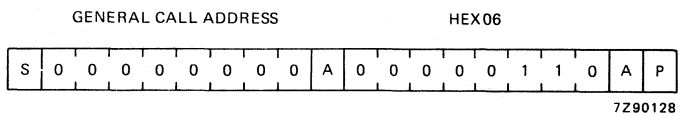


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 13)	V_{P1}	−0,3 to +18	V
(pin 19)	V_{P2}	−0,3 to +18	V
(pin 14)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 2)	V_{SDA}	−0,3 to +18	V
(pin 3)	V_{SCL}	−0,3 to +18	V
(pins 4 to 7)	V_{P2X}	−0,3 to +18	V
(pins 8 and 9)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 10)	V_{TI}	−0,3 to V_{P1}*	V
(pin 12)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 15 to 18)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 20)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 21)	V_{OSC}	−0,3 to +5	V
(pins 1 and 22 to 24)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

DEVELOPMENT DATA

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	18	30	45	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	−2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	380	–	mW
Operating ambient temperature	T_{amb}	−20	–	+70	°C
I^2C bus inputs/outputs					
SDA input (pin 2); SCL input (pin 3)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 2, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 4 to 7, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 8, 9)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 10, 12)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current i into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 15 to 18)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 20)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 21)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 3 (pins 22 to 24 and pin 1)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 4) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification.
After reset has been activated, transmission may only be started after a 50 μs delay.

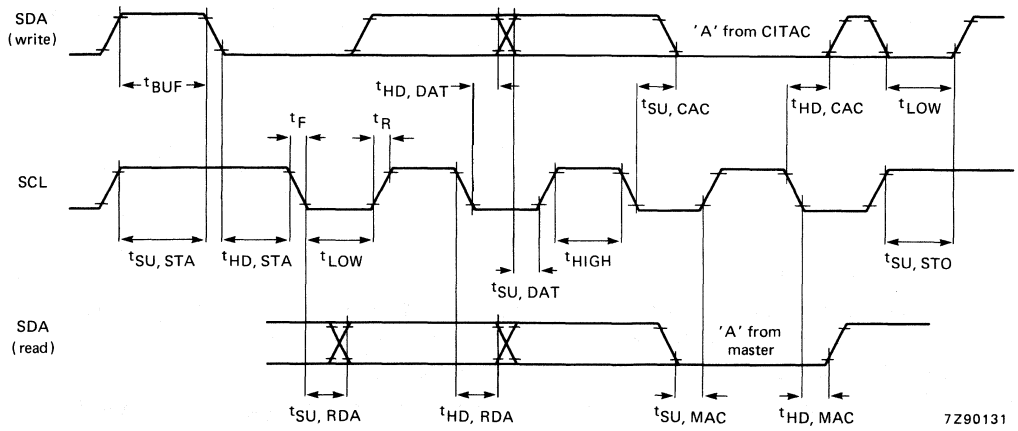


Fig. 8 I²C bus timing SAB3037.

DATA LINE DECODER

GENERAL DESCRIPTION

The SAF1135 is a data line decoder, designed in CMOS technology, which operates in conjunction with the data line processor (SAA5235) to form a data line receiver system.

This system receives and decodes binary data that is transmitted in line 16 of every first field of a standard television signal. The decoded information is accessed via the built-in I²C bus interface. This information can be used to program a video tape recorder to start and stop the recording of a television program at the correct time, regardless of a delay or extension in the transmission time of the required television program.

Valid Video Programming System (VPS) data is transmitted in line 16 only. There is no VPS information in line 329.

The data transmission is biphase modulated and the bit transfer rate is 2,5 Mbit/s.

Features

- Field selection
- Line 16 decoding
- Start code check
- Biphase check
- Storage of data line information
- Generation of data reset pulse
- I²C bus transmitter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 14)	I_{DD}	–	1	–	mA
Bit transfer rate at input DLD (pin 8)	BR_{DLD}	–	2,5	–	Mbits/s
Clock frequency at input DLCL (pin 11)	f_{DLCL}	–	5	–	MHz
Storage temperature range	T_{stg}	−65	–	+150	°C
Operating ambient temperature range	T_{amb}	0	–	70	°C

PACKAGE OUTLINES

14-lead DIL; plastic (SOT-27).

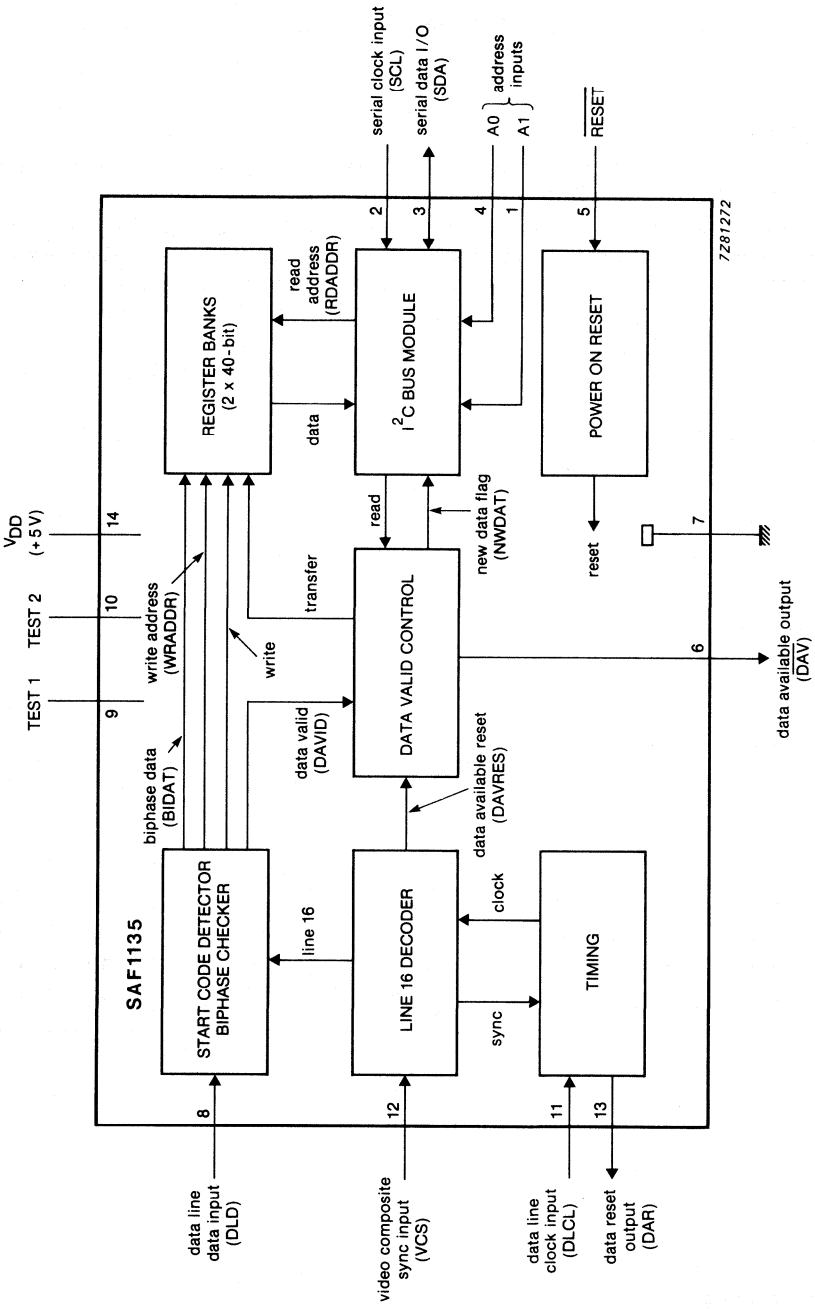


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The SAF1135 is designed to receive and decode Video Tape Recorder (VTR) control information which is transmitted in line 16 of every first field of a standard television signal. The following description refers to the block diagram Fig. 1 unless otherwise stated.

Data line 16

The total information of data line 16 consists of fifteen 8-bit words. The contents of the information is shown in Fig. 2, a timing diagram of the data line in Fig. 3 and a survey of VTR control labels in Fig. 4.

From the total fifteen 8-bit words, the SAF1135 extracts words 5, 11, 12, 13 and 14. The contents of these words can be requested via the built-in I^2C bus interface (see Fig. 9). The circuit is fully transparent, thus each bit is transferred without modification. Only the sequence of the words is changed; words 11 to 14 being transmitted first followed by word 5.

By evaluation of the Video Composite Sync (VCS) signal at pin 12 the SAF1135 identifies the beginning of line 16 in the first field. The line 16 decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection, see Fig. 5) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in register bank R (Receive). If no biphase error has occurred, the contents of register bank R are transferred to register bank T (Transmit) by the data valid control signal (DAVID). If the system has been addressed, this transfer is delayed until the next start or stop condition of the I^2C bus has been received.

The last correct data line information remains available until it is read via the I^2C bus. After it is read once the stored information is no longer considered to be valid, the internal new data flag (NWDAT) is reset and if the circuit is addressed, the only VPS data sent back is "FFF...F". The same conditions apply after power-up. Then no data can be read out.

New data is available after reception of another error-free line 16.

Power-on Reset

Reset pulses applied externally to pin 5 ($\overline{\text{RESET}}$; active LOW) are latched internally by the power-on reset circuit.

$\overline{\text{RESET}}$ = LOW influences:

- I^2C bus logic to no acknowledge
- NWDAT flag and internal timing to reset
- Data available output ($\overline{\text{DAV}}$; active LOW) at pin 6 forced to LOW
- Data reset output (DAR) at pin 13 forced to HIGH
- Serial data (SDA) input/output at pin 3 released

When $\overline{\text{RESET}}$ changes to HIGH the reset period is terminated with the next negative-going transition of the data line clock (DLCL) input at pin 11. Then, the data available ($\overline{\text{DAV}}$) output at pin 6 will go HIGH.

When an external reset is not used pin 5 is connected to V_{DD}. If an external reset is required, the rise time (t_r) of $\overline{\text{RESET}}$ voltage must be greater than 50 μs. An external 10 kΩ resistor connected between pin 5 and V_{DD} and an external 2,7 nF capacitor connected to V_{SS} will result in $t_r \geqslant 50$ μs.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Word	Content
1	Run in
2	Start code
3	Program source identification (binary coded)
4	Program source identification (ASCII sequential)
5	Sound and VTR control information
6	Program/Test picture identification
7	Internal information exchange
8	Address assignment of signal distribution
9	
10	Messages/Commands
11	VTR Control Information
12	
13	
14	
15	Reserve

Fig. 2 Total information of data line 16.

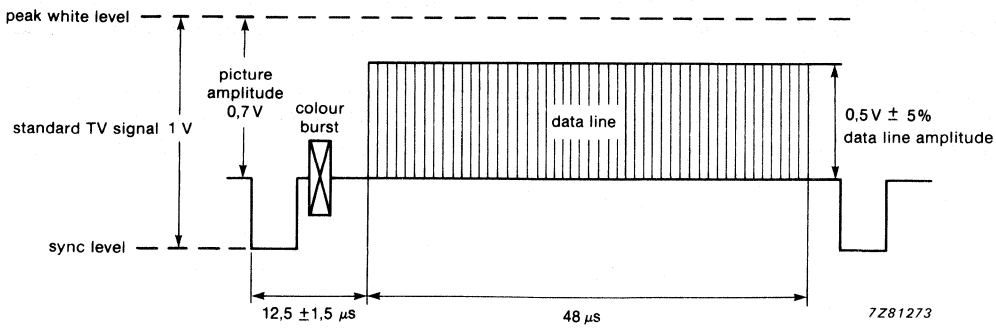


Fig. 3 Timing diagram of data line 16; modulation depth 71,4%.

VTR Control Information

Word-no. 5 (Bit-no. 1–8):

	Bit 1	Bit 2	Status
Label binary	0	0	2-Channel
	0	1	Mono
	1	0	Stereo
	1	1	2-Channel
	Bit 3	**Bit 4**	
Pause Code	1	0	not for children
Interrupt Code	0	1	free

Word-no. 11–14 (Bit-no. 0–31):

Word-no.	11								12								13								14	
Bit-no.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24–25	26–31
Label binary	Address range		Day					Month				Hour					Minute						Nation			Program Source
			Special System Code																							
System Status Code	1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	NC . . NC			PC . . . . PC
Pause Code	1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	NC . . NC			PC . . . . PC
Interrupt Code	1	X	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	NC . . NC			PC . . . . PC

Where:

X = 0 or 1 (bit)

NC is the Nation Code

PC is the Program Source Code

Fig. 4 VTR control information of data line 16.

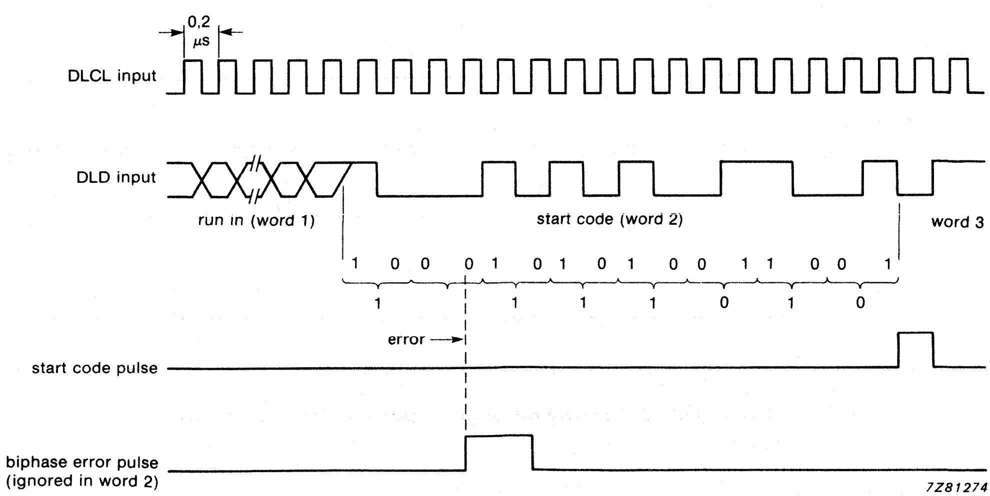


Fig. 5 Timing diagram of start code detection.

FUNCTIONAL DESCRIPTION (continued)

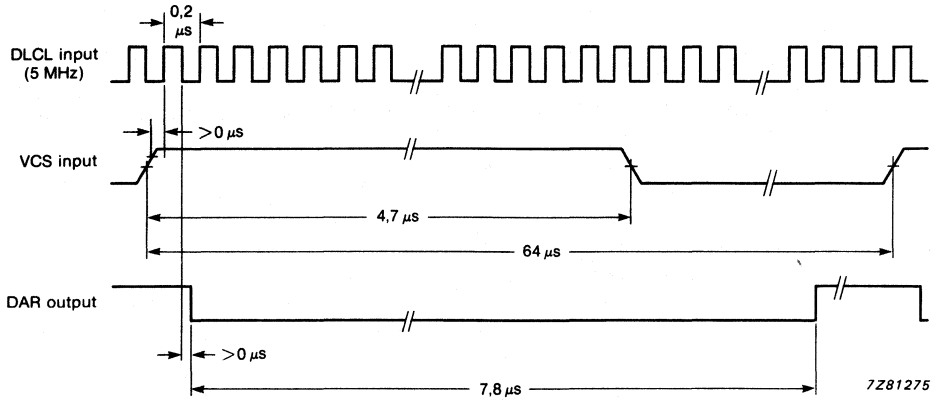


Fig. 6 Timing diagram of the data reset pulse generation.

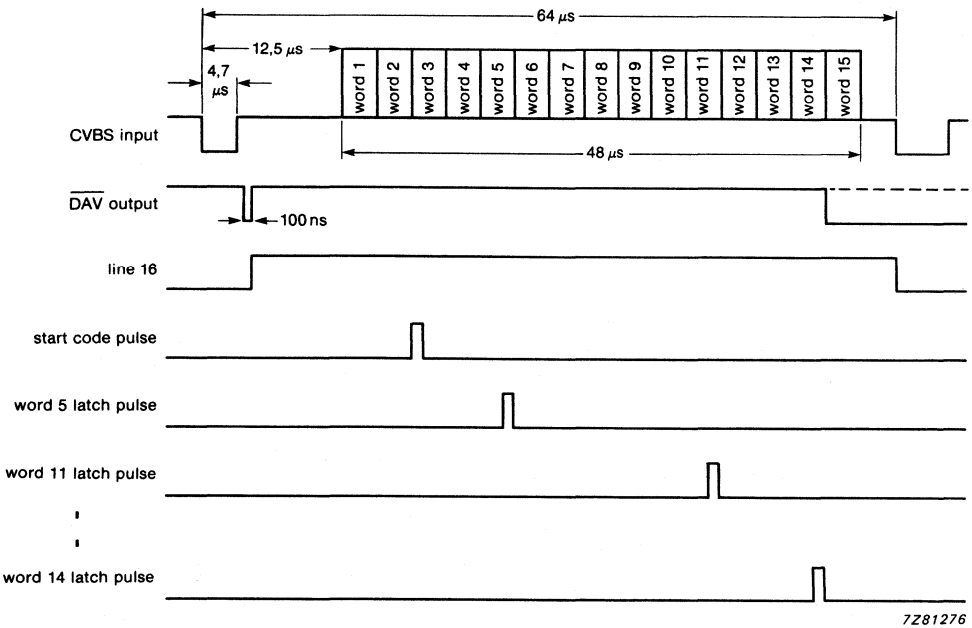


Fig. 7 Timing diagram of the data available output and word latch pulses.

Data line data and clock inputs (DLD; DLCL)

The data line data and clock signals from the SAA5235 are input at pins 8 and 11 respectively. The data transmission is biphase modulated, the bit transfer rate is 2,5 Mbit/s and the clock frequency is 5 MHz.

Input DLD incorporates an internal active clamping circuit. DLCL is internally a.c. coupled.

Video composite sync input (VCS)

The VCS input pulse at pin 12 is used for:

- Generation of the data reset pulse (DAR)
- Identification of the first field
- Selection of line 16

The timing of the data reset pulse generation is shown in Fig. 6.

I^2C bus address inputs (A0; A1)

The two I^2C address inputs at pins 4 and 1 respectively, provide the four different addresses 20H, 22H, 24H and 26H.

Data reset output (DAR)

The DAR output at pin 13 is a line frequency pulse with a 0,88 duty factor derived from the VCS pulse. The DAR pulse is fed to the SAA5235 to reset the data slicer circuit and the clock phase detector circuit.

Data available output ($\overline{DAV}$)

The $\overline{DAV}$ active LOW output at pin 6 is set to LOW after reception of one error-free data line 16. $\overline{DAV}$ returns to HIGH after at the beginning of the next first field.

If no valid data is available $\overline{DAV}$ remains HIGH. However, a short duration (100 ns) pulse inserted at the beginning of line 16 ensures that a HIGH-to-LOW transition occurs, which can be used for triggering.

The timing of $\overline{DAV}$ output and word latch pulses is shown in Fig. 7.

I^2C bus

The internally latched data from words 5 and 11 to 14 can be clocked out via the I^2C interface by a bus master. The lines are the serial clock input (SCL) at pin 2 and the serial data input/output (SDA) at pin 3.

The SAF1135 can operate only as a slave transmitter on the bus.
Data format is shown in Fig. 8.

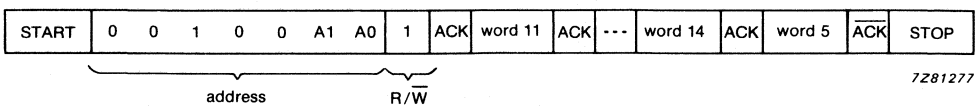


Fig. 8 I^2C bus data format.

- The MSB of each word is transmitted first.
- There is no restriction on the number of words to be transmitted, but if more than five words are requested, word 5 will be repeated.
- Noise pulses less than 200 ns duration are ignored on the bus lines.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 14)	V_{DD}		−0,5 to +7,0	V
Supply current (pin 14)	I_{DD}	max.	20	mA
Supply current (pin 7)	I_{SS}	max.	20	mA
Input voltage (pins 8 and 11)	V_I		−0,5 to +12	V
Input voltage on all other pins	V_I		−0,5 to V_{DD} +0,5*	V
Input current	$\pm I_I$	max.	10	mA
Output current	$\pm I_O$	max.	10	mA
Power dissipation per package**	P_{tot}	max.	400	mW
Power dissipation per output	P	max.	100	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* V_{DD} +0,5 not to exceed 7,0 V.
** Above +60 °C: derate linearly with 8 mW/K.

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 14)						
Supply voltage	–	V_{DD}	4,5	5	5,5	V
Supply current	Quiescent at 25 °C All inputs at V_{DD} or V_{SS} $\overline{RESET}$ at V_{SS} TEST 1 and $\overline{TEST\ 2}$ at V_{DD} I_O = 0 mA	I_{DD}	–	–	10	μA
	During normal operation (without LED at $\overline{DAV}$, V_{DD} = 5 V)	I_{DD}	–	1	–	mA
Inputs						
A0, A1, TEST 1, TEST 2, SCL						
Input voltage LOW		V_{IL}	–	–	$0{,}2V_{DD}$	V
Input voltage HIGH		V_{IH}	$0{,}7V_{DD}$	–	–	V
Leakage current		I_{LI}	–	–	1	μA
DLCL						
Input voltage	Clock internally a.c. coupled	V_I	–	–	12	V
Leakage current	V_I = 0 to 10 V	I_{LI}	–	–	10	μA
$\overline{RESET}$	During normal operation pin 5 connected to V_{DD}					
Input voltage LOW		V_{IL}	–	–	$0{,}3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0{,}9V_{DD}$	–	–	V
Input current HIGH		I_{IH}	–	–	15	μA
Leakage current		I_{LI}	–	–	10	μA
VCS						
Input voltage LOW		V_{IL}	–	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	–	V
Leakage current		I_{LI}	–	–	1	μA

D.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs/Outputs						
DLD	Internal active clamping circuit, open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	2,0	–	12	V
Leakage current		I_{LI}	–	–	1	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
SDA	open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	3,15	–	–	V
Leakage current	V_{DD} = 6 V; V_I = 0 or V_{DD}	I_{LI}	–	–	6	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Outputs						
DAR						
Output voltage LOW	I_{OL} = 1 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V
$\overline{DAV}$						
Output voltage LOW	I_{OL} = 10 mA	V_{OL}	–	–	1,0	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs						
Input capacitance		C_I	–	–	10	pF
A0, A1, TEST 1, TEST 2, SCL						
Rise time	$V_{IL(max)}$ to $V_{IH(min)}$	t_r	50	–	–	µs
DLCL						
Clock frequency	sinusoidal input signal	f_{DLCL}	–	5	–	MHz
Input voltage	peak-to-peak value	$V_{I(p-p)}$	1	–	–	V
DLD						
Coupling capacitor		C_{EXT}	—	1	4,7	nF
Set-up time	relative to rising edge of DLCL	t_{SU}	40	–	–	ns
Hold-up time	relative to rising edge of DLCL	t_{HD}	40	–	–	ns
Outputs						
DAR, $\overline{DAV}$						
Rise and fall times	C_L = 50 pF	t_r, t_f	–	–	50	ns
DAR-time LOW		$t_{DAR,L}$	–	7,8	–	µs
SDA						
Fall time	C_L = 400 pF	t_f	–	–	300	ns
I²C bus - Input/Output						
	For both SDA and SCL valid					
Input current HIGH	0,9 V_{DD}, including I_{LI} of possible output stage	I_{IH}	–	–	10	µA
Input capacitance		C_I	–	–	10	pF
Rise time		t_r	–	–	1	µs
Fall time		t_f	–	–	0,3	µs
Clock frequency		f_{CL}	–	–	100	kHz
Pulse duration LOW		t_{LOW}	4,7	–	–	µs
Pulse duration HIGH		t_{HIGH}	4,0	–	–	µs

APPLICATION INFORMATION

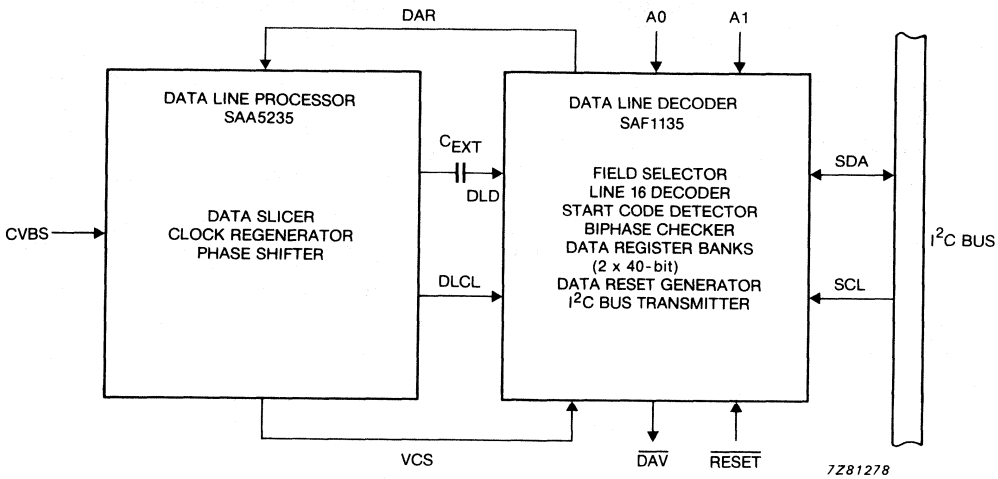


Fig. 9 Data line receiver.

16/32-BIT MICROPROCESSOR

GENERAL DESCRIPTION

The SCC68070 is a 16/32-bit central processing unit suitable for use in a large variety of applications. It is fully object code compatible with the 68000. By integrating standard and advanced peripheral functions on the SCC68070, system costs are drastically reduced.

The internal architecture is built around a bus interconnecting the CPU and the various on-chip peripheral functions. Each function has several dedicated connections to the external circuitry. The SCC68070 includes powerful programmable interrupt processing circuitry for interrupts generated by internal and external sources. An on-chip clock generator provides a half crystal frequency clock signal for CPU and peripheral interfaces.

The on-chip MMU, if selected takes care of address translation and memory protection. Two DMA channels increase data throughput and the I²C-bus interface allows easy and low-cost addition of peripherals. The SCC68070 also includes a UART interface. A built-in timer/counter with two independently programmable match/count/capture registers, means that the SCC68070 can be programmed with two of the following options simultaneously:

- pulse generator
- external event counter
- reference timer

This document gives an overview of the basic functions, internal structure and electrical characteristics. For further details on the features and operation of the SCC68070 refer to 'User Manual, Part 1 - Hardware'.

Features

- CMOS technology
- 32-bit internal structure
- Enhanced bus error handling
- 4 decoded interrupt inputs
- 2 programmable interrupt inputs
- Decoded interrupt acknowledge
- Built-in clock generator - maximum 30 MHz crystal
- On-chip MMU; supporting virtual memory
- 2-channel DMA controller
- I²C serial bus interface
- UART serial bus interface
- 16-bit timer/counter
- Two 16-bit match/count/capture registers
- Fully 68000 object code compatible
- Bus interface similar to 68000
- 56 powerful instruction types
- 5 basic data types
- 16 Mbyte addressing range
- 14 addressing modes
- Memory mapped I/O
- Vectored and auto-vectored interrupts
- 7 interrupt levels
- Maximum internal clock frequency: 15 MHz
- 84-pin PLCC or a 120-pin QFP package

ORDERING INFORMATION

extended type number	temperature range (°C)	clock frequency (MHz)	package code
SCC68070CAA84	0 to 70	10.0	PLCC84
SCC68070CBA84	0 to 70	12.5	PLCC84
SCC68070CCA84	0 to 70	15.0	PLCC84
SCC68070AAA84	−40 to 85	10.0	PLCC84
SCC68070ABA84	−40 to 85	12.5	PLCC84
SCC68070ACA84	−40 to 85	15.0	PLCC84
SCC68070CAB	0 to 70	10.0	QFP120
SCC68070CBB	0 to 70	12.5	QFP120
SCC68070CCB	0 to 70	15.0	QFP120
SCC68070AAB	−40 to 85	10.0	QFP120
SCC68070ABB	−40 to 85	12.5	QFP120
SCC68070ACB	−40 to 85	15.0	QFP120

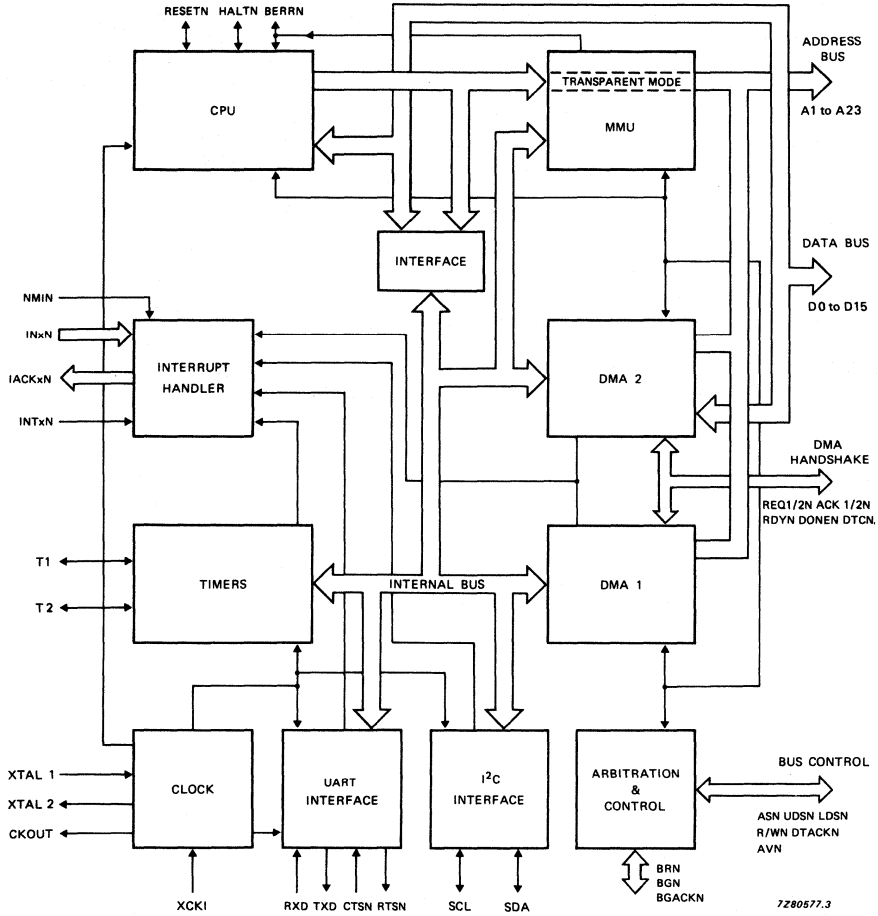


Fig.1 Block diagram.

DEVELOPMENT DATA

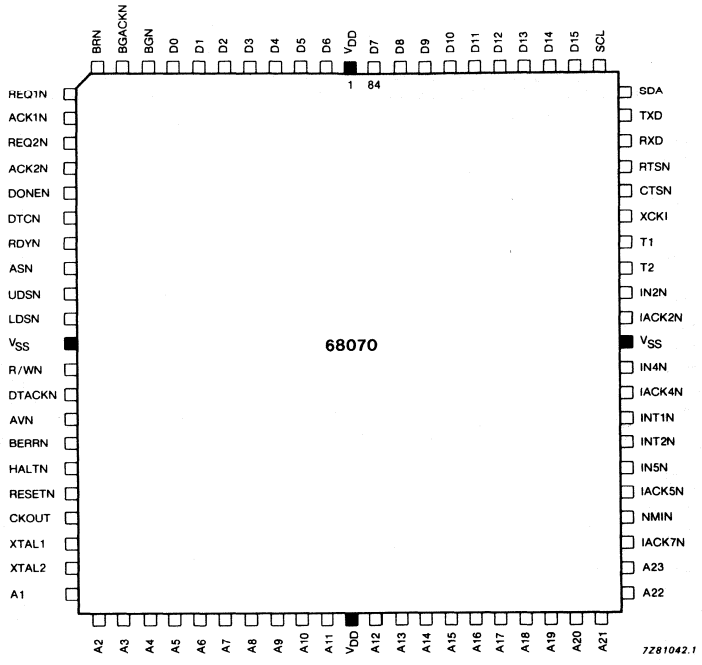
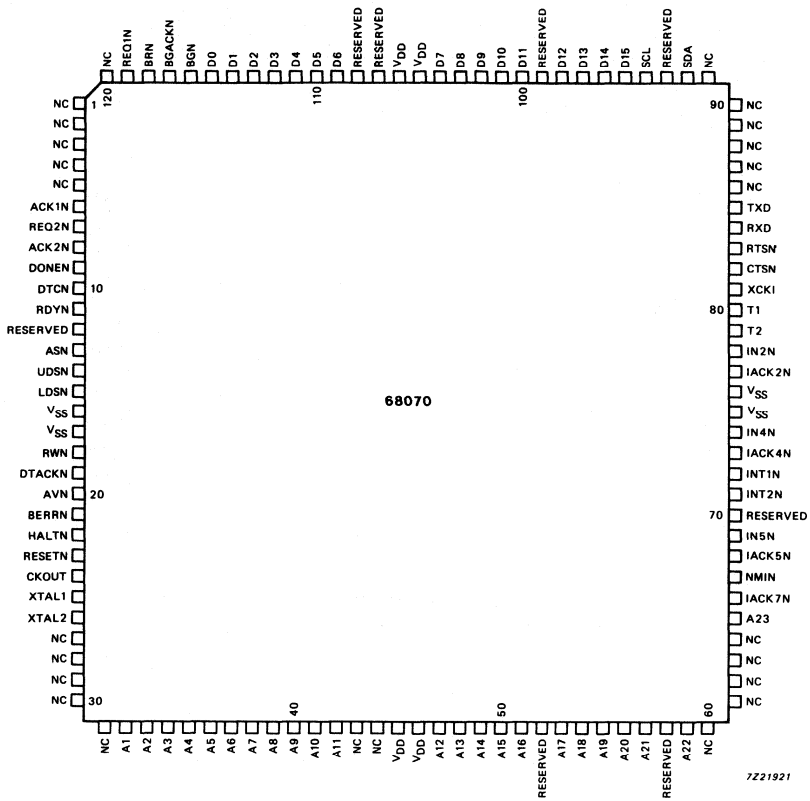


Fig.2 Pinning diagram for PLCC84.



All pins designated 'NC' or 'RESERVED' must not be connected externally.

Fig.3 Pinning diagram for QFP120.

Signal description (PLCC84)

mnemonic	type	pin no.	function
A1 to A23	O	32-42, 44-55	**Address bus** (active HIGH, 3-state). For direct addressing of 16 Mbytes of memory.
D0 to D15	I/O	82, 8476	**Data bus** (active HIGH, 3-state, bidirectional). 16bit wide.
ASN	O	19	**Address Strobe** (active LOW, 3-state). Indicates a valid address on the bus.
LDSN	O	21	**Lower Data Strobe** (active LOW, 3-state). Indicates that: – For a WRITE cycle, the data is valid on the lower half of the data bus (D0 to D7). – For a READ cycle, the data is to be placed on the lower half of the bus (D0 to D7).
UDSN	O	20	**Upper Data Strobe** (active Low, 3-state). Indicates that: – For a WRITE cycle, the data is valid on the lower half of the data bus (D8 to D15). – For a READ cycle, the data is to be placed on the upper half of the bus (D8 to D15).
R/WN	O	23	**Read** (active HIGH)/Write (active LOW). This controls the direction of data flow.
DTACKN	I	24	**Data Transfer Acknowledge** (active LOW). Asserted by the peripheral during CPU or DMA bus cycles when data is either received from or placed on the bus. If not asserted punctually, it causes the CPU or DMA controller to insert wait states.
BRN	I	11	**Bus Request** (active LOW). Asserted by wired-ORed external DMA devices that request bus ownership.
BGN	O	9	**Bus Grant** (active LOW). A daisy chain output that is asserted by the SCC68070 when the bus is granted by the CPU and the DMA does not have a bus request pending.
BGACKN	I/O	10	**Bus Grant Acknowledge** (active LOW, open drain). Asserted by any DMA device (internal or external) that has control of the bus. As long as this line is held LOW externally, the SCC68070 will hold the bus signals in the high impedance state. When BGACKN is released, the SCC68070 will have access to the bus. Interrupts cannot be serviced while BGACKN is held LOW.
RESETN	I/O	28	**Reset** (active LOW, open drain, bidirectional). If asserted externally together with the HALTN line, it will cause the processor to enter the Reset state. It is driven LOW by the processor when the Reset instruction resets external hardware.
HALTN	I/O	27	**Halt** (active LOW, open drain, bidirectional). If asserted externally together with RESETN, it causes the SCC68070 to enter the Reset state. If asserted alone, it will cause the CPU or DMA controller to stop after completion of the current bus cycle. If HALTN and BERRN are asserted together, the CPU will complete the current bus cycle, stop operation, and place all 3-state lines in their high impedance state until HALTN and BERRN have been released, and then it will rerun the same bus cycle. BERRN should be released before HALTN. As long as HALTN is held LOW all control signals are inactive and all 3-state lines are placed in their high impedance state. When the processor has stopped executing instructions (e.g. after a double bus fault) the processor drives this line LOW.

Signal description (continued)

mnemonic	type	pin no.	function
BERRN	I/O	26	Bus Error (active LOW, open drain). If this line is asserted during a bus cycle, it indicates that there was a fault in the bus cycle access. If asserted together with HALTN, the same bus cycle will re-run after both HALTN and BERRN have been released. If BERRN is asserted alone, the SCC68070 will start bus-error exception processing. BERRN is driven LOW by the SCC68070 when the MMU indicates a bus error.
INT1N, INT2N	I	61, 60	Latched Interrupt inputs (active LOW). A LOW level of 1 clock pulse will be stored as a pending interrupt request. Priority levels are programmable.
IN2N, IN4N, IN5N	I	66, 63, 59	Decoded Interrupt priority inputs (active LOW). IN2N has the lower and IN5N has the higher priority.
NMIN	I	57	Non-maskable interrupt (level 7) (active LOW). While the other interrupts may be masked (disabled), this interrupt is always enabled.
IACK2N, IACK4N, IACK5N, IACK7N	0	65, 62, 58, 56	Decoded Interrupt acknowledge (active Low). Asserted during an interrupt acknowledge sequence to indicate to a peripheral that its interrupt request is being serviced.
AVN	I	25	Autovectored interrupts (active LOW). If held LOW during the interrupt acknowledge sequence, the processor calculates the appropriate vector from a fixed vector table. If kept HIGH, the peripheral must provide an 8-bit vector number.
V_{DD}	–	1, 43	Supply voltage + 5.0 V nominal.
V_{SS}	–	22, 64	Ground.
XTAL1, XTAL2	I	30, 31	External crystal inputs. XTAL1 can be used as a clock input if an external clock generator is used. The crystal or external clock frequency is divided by 2 to obtain the internal clock and CKOUT signals.
CKOUT	O	29	Clock out. This is the reference from the internal system clock.
REQ1N, REQ2N	I	12, 14	DMA Request (active LOW). These are inputs from I/O devices requesting service from the DMA controller and causes it to request control of the bus. In burst mode, the inputs are level sensitive and the DMA controller releases the bus after REQ1N (or REQ2N) becomes active and the current DMA cycle is completed. In cycle-stealing mode, REQ1N or REQ2N inputs are triggered by a negative pulse. This pulse must occur at least one clock cycle before DTCN is asserted to ensure continuous transfer.
ACK1N, ACK2N	O	13, 15	DMA Request Acknowledge (active LOW). ACK1N (or ACK2N) is asserted by the DMA controller to indicate that it has acquired the bus and the requested device bus cycle is now beginning. It is active at the beginning of every device cycle together with ASN, and is deactived at the end of every device bus cycle.
RDYN	I	18	Device Ready (active LOW). The requesting device asserts RDYN to indicate to the DMA controller that valid data has either been stored or put on the bus. If RDYN remains inactive, it indicates that the data has neither been stored nor put on the bus, causing the DMA controller to insert wait states. RDYN can be held LOW permanently if the device is fast enough, indicating that the device is always ready and so no wait states are required. RDYN is not monitored by Channel 2 in the dual address mode.

Signal description

mnemonic	type	pin no.	function
DTCN	O	17	Device Transfer Complete (active LOW, open drain). In DMA mode DTCN is asserted by the DMA controller to indicate to the device that the requested data transfer is complete. On a write-to-memory operation, it indicates that the data provided by the device has been stored successfully. On a read-from-memory operation, it indicates that the data from memory is present on the data bus and should be latched.
DONEN	I/O	16	Done (active LOW, open drain). With DONEN as an output, the DMA controller asserts it simultaneously with the ACK1N (or ACK2N) output to indicate to the device that the transfer count is zero and therefore, the DMA controller's operation is complete. If, as an input, DONEN is asserted by the device before the transfer count reaches zero, it causes the DMA controller to abort the operation and generate an interrupt request (if the interrupts are enabled).
SCL	I/O	75	Serial Clock (open drain). SCL is the clock signal for the I^2C-bus operation. It is either driven by the SCC68070 when the I^2C interface is in the master mode, or is the clock input if the I^2C interface is in the slave mode.
SDA	I/O	74	Serial Data (open drain). SDA is the data signal for the I^2C-bus.
T1, T2	I/O	68, 67	Timers 1 and 2 (3-state). These are the I/O signals for the capture timers of channels 1 and 2 respectively. They can be programmed as either outputs for pulses or inputs for count cycles and events.
RXD	I	72	Receive Data. RXD is the data input for the UART serial interface.
TXD	O	73	Transmit Data. TXD is data output for the UART serial interface.
RTSN	O	71	Request To Send (active LOW). This output of the UART serial interface indicates that the receiver is ready to accept data on the RXD line.
CTSN	I	70	Clear To Send (active LOW). This input to the UART serial interface indicates that the remote receiving device is ready. RTSN and CTSN can be connected together if no control lines are needed.
XCKI	I	69	External clock. When selected, XCKI is the clock input for the UART serial interface. This signal can be used either: – to generate special baud rates or, – when a crystal frequency other than 19.6608 MHz is used by the SCC68070, an external clock of 4.9152 MHz (or 9.8304 for 38200 bauds) can be connected to this input to generate the standard baud rates.

Note

The signal descriptions given for the PLCC84 package also apply to the QFP120 package. However, the pinning arrangement for the QFP120 is different, as can be seen in Fig.3.

CPU FUNCTIONAL DESCRIPTION

General

The CPU of the SCC68070 is software compatible with the 68000, consequently programs written for the 68000 will run on the SCC68070 unchanged. However, for certain applications the following differences between the processors should be noted:

- Differences exist in the exception error processing since the SCC68070 can provide full bus-error recovery.
- The timing is different because of the SCC68070's new architecture and technology. Although the bus timing is similar to the 68000, instruction execution timing is completely different. For execution timing see Tables 7 to 19.

Programming model and data organization

The programming model is identical to that of the 68000 and is shown in Fig.4. It contains seventeen 32-bit registers, a 32-bit Program Counter and a 16-bit Status Register (see Fig.6). The first eight registers (D0 to D7) are used for data registers for byte, word and long-word operations. The second group of registers (A0 to A6) and the system stack pointer (A7) can be used as software stack pointers and base address registers. In addition, these registers can be used for word and long-word address operations. All seventeen registers can be used as index registers.

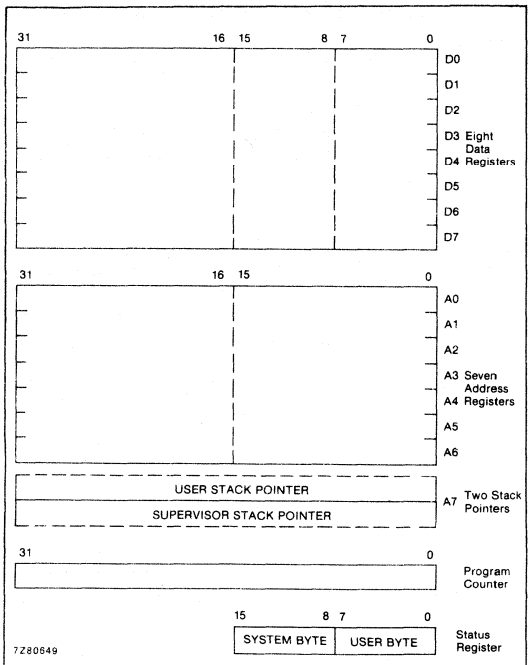
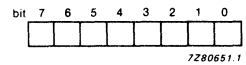
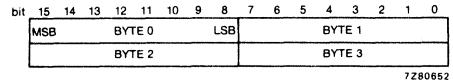


Fig.4 Programming Model.

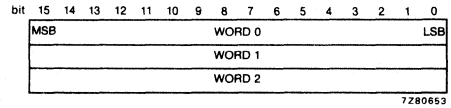
The SCC68070 supports bit data, integer data of 8, 16 and 32 bits, 32-bit addresses and BCD data. Each data type is arranged in the memory as shown in Fig.5.



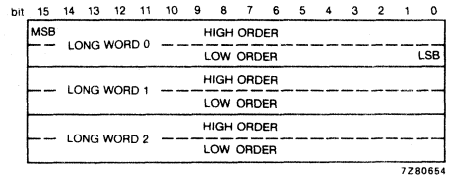
(a) Bit data (1 byte = 8 bits).



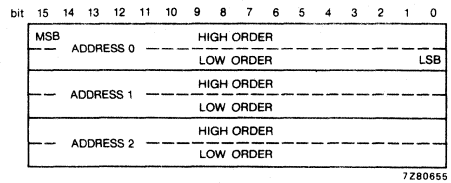
(b) Integer data(1byte = 8 bits).



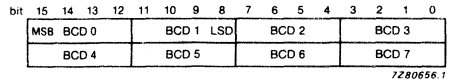
(c) Word data (16 bits).



(d) Long-word data (32 bits).



(e) Addresses (1 address = 32 bits).



(f) BCD data (2 BCD digits = 1 byte).

Fig.5 Memory data organization.

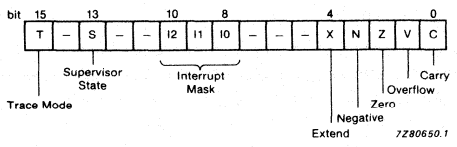


Fig.6 Status Register.

Internal and external operation

The SCC68070 operates with a maximum internal clock frequency of 15 MHz and a minimum of 4 MHz. Each clock cycle is divided into 2 states. A non-access machine cycle has 3 clock cycles or 6 states (S0 to S5). An on-chip or external bus access normally consists of 3 clock cycles plus 1 clock cycle (2 SB states). When DTACKN is not asserted, indicating that data has not been received or put on the bus, wait states (SW) are inserted in multiples of 2.

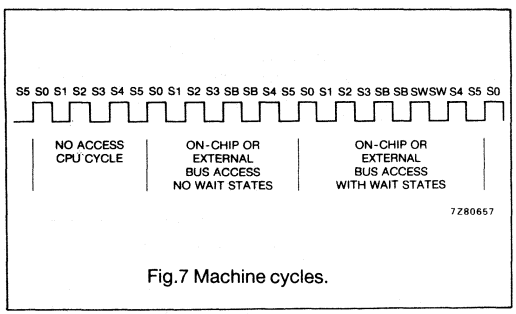


Fig.7 Machine cycles.

Bus timing

Bus cycles in the SCC68070 are similar to those of a 68000 running at a CKOUT frequency. However, if the DTACKN signal is not asserted by the time the SCC68070 is ready to transmit or receive data, it will insert wait cycles. Upper and lower data strobes (UDSN and LDSN) are asserted independently with respect to the type of transfer (low byte - LDSN asserted, high byte - UDSN asserted, and word - both strobes asserted).

Bus arbitration

Because a DMA controller is integrated on the SCC68070 as a possible bus master, the bus arbitration needs a priority protocol. This is done by a daisy-chain using the BUS GRANT (BGN) of the CPU such that Channel 1 of the DMA controller has highest priority, followed by Channel 2 and then the external devices. The CPU grants bus acquisition and therefore has lowest priority. Once the DMA controller has submitted the internal bus grant to an outside master it will not interrupt the line until BUS GRANT ACKNOWLEDGE (BGACKN) has been negated externally. If the DMA controller has a DMA request pending, it will acquire the bus as soon as the external device has negated BGACKN. In this event, it will not submit BGN to an outside master, even if the prospective masters BRN signal had been asserted before the DMA controller's pending request.

DEVELOPMENT DATA

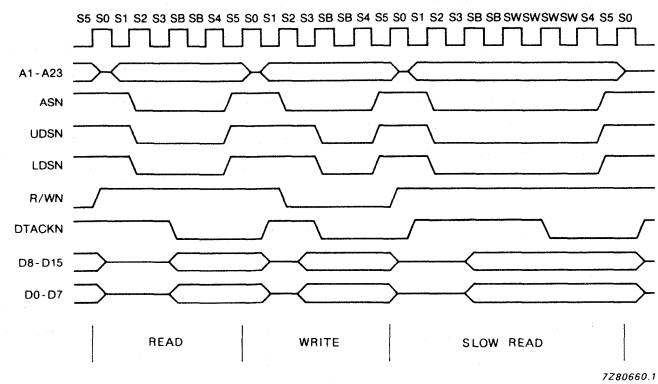


Fig.8 Read, write and slow read cycle timing.

Processing states

The CPU is always in one of three processing states: normal, exception or halted.

The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further memory accesses are made by the CPU.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be generated internally by an instruction or an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by bus error or by a reset. Exception processing is designed to provide an efficient context switch so that the processor can handle unusual conditions.

The halted processing state is an indication of a catastrophic hardware failure. For example, if during exception processing of a bus error another bus error occurs, the CPU assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a CPU in the stopped state is not in the halted state or vice versa.

The processor can work in the 'user' or 'supervisor' state determined by the state of the S-bit in the Status Register. Accesses to the on-chip peripherals must be in the supervisor state.

Exception processing

Exception processing occurs in four steps. First, a copy is made of the contents of the Status Register and then the S-bit is asserted, putting the processor into the privileged supervisor state. Second, the vector number of the exception is determined; this is used to generate the address of the exception routine. The next step saves the current processor status. Copies of the current program counter, the Status Register and the Format plus vector number are saved on the supervisor stack using the supervisor stack pointer. Finally the contents of the exception vector location are fetched and loaded into the Program Counter and the exception handling routine starts normal instruction execution.

Exception vectors

Exception vectors are memory locations from which the CPU fetches the address of a routine that will handle that exception. All exception vectors are 2 words in length (see Fig.9) except the reset vector, which is made up of 4 words. All exception vectors are contained in the supervisor data space. When the reset vector is fetched after a RESETN, the MMU is disabled and the reset vector is located at physical address 0. A vector number is an 8-bit number that, when multiplied by 4, gives the address of an exception vector. Vector numbers are generated internally or externally depending on the cause of the exception. During the interrupt acknowledge bus cycle, an external peripheral may send the CPU an 8-bit vector number (see Fig.10) on the data bus lines D0 to D7. The CPU translates the vector number into the full 24-bit address as shown in Fig.11. The memory layout for the exception vectors is given in Table 1.

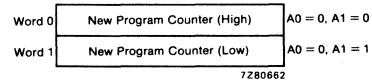


Fig.9 Exception vector format.

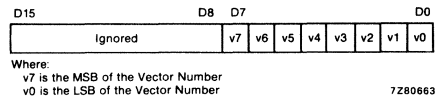


Fig.10 External peripheral vector format.

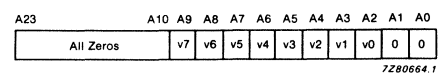


Fig.11 Address translated from 8-bit vector number.

Table 1 Exception vector assignment

vector Nos.	DEC	HEX	assignment
0	0	000	Reset:initial SSP
1	4	004	Reset:initial PC
2	8	008	Bus error
3	12	00C	Address error
4	16	010	Illegal instruction
5	20	014	Zero divide
6	24	018	CHK instruction
7	28	01C	TRAPV instruction
8	32	020	Privilege violation
9	36	024	Trace
10	40	028	Line 1010 emulator
11	44	02C	Line 1111 emulator
12*	48	030	(Unassigned, reserved)
13*	52	034	(Unassigned, reserved)
14	56	038	Format error
15	60	03C	Uninitialized vector interrupt
16-23*	64	040	(Unassigned, reserved)
-	95	05F	-
24	96	060	Spurious interrupt
25	100	064	Level 1 interrupt autovector
26	104	068	Level 2 interrupt autovector
27	108	06C	Level 3 interrupt autovector
28	112	070	Level 4 interrupt autovector
29	116	074	Level 5 interrupt autovector
30	120	078	Level 6 interrupt autovector
31	124	07C	Level 7 interrupt autovector
32-47	128	080	TRAP instruction vectors
-	191	0BF	-
48-56*	192	0C0	(Unassigned, reserved)
-	227	0E3	-
57	228	0E4	Level 1 on-chip interrupt autovector
58	232	0E8	Level 2 on-chip interrupt autovector
59	236	0EC	Level 3 on-chip interrupt autovector
60	240	0F0	Level 4 on-chip interrupt autovector
61	244	0F4	Level 5 on-chip interrupt autovector
62	248	0F8	Level 6 on-chip interrupt autovector
63	252	0FC	Level 7 on-chip interrupt autovector
64-255	256	100	User interrupt vectors

* Vectors 12, 13, 16 to 23, and 48 to 56 are reserved for future enhancements. No user peripheral devices should be assigned to these numbers.

Multiple exceptions

As two or more exceptions can occur simultaneously, exceptions are grouped in order of priority; as is shown in Table 2.

Table 2 Exception grouping and priority

group	exception	processing
0	RESET ADDR.ERROR BUS ERROR	Exception processing begins at the next machine cycle
1	TRACE iNTERRUPT ILLEGAL PRIVILEGE	Exception processing begins before the next instruction
2	TRAP,TRAPV, CHK, ZERO, DIVIDE, FORMAT ERROR	Exception processing is started through normal instruction execution

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Reset operation

When the CPU executes a RESET instruction, the RESETN signal is driven LOW for 146 clock cycles to reset internal and external peripherals. The CPU itself is not affected but all on-chip peripherals are reset. When both the RESETN and HALTN signals are driven LOW by an external device, the CPU and on-chip peripherals are reset. The CPU responds by reading the reset vector table entry (vector number zero, address 000000H) and loads it to the Supervisor Stack Pointer (SSP). Vector table entry number one (at address 000004H) is read next and loaded into the Program Counter (PC). The CPU then initializes the Status Register (SR) to an interrupt level of seven and instruction execution is started (see Fig.12).

All 3-state output signals are placed in the high-impedance state for as long as the RESETN and HALTN signals are externally driven. When the RESETN and HALTN signals are released, the CPU will execute 4 read cycles after start-up time, to load the SSP High, SSP Low, PC High and PC Low. Then the first instruction is fetched and executed. The HALTN signal must be driven LOW at the same time as the RESETN signal. The SCC68070 will only start to read the stack and the initial Program Counter after both signals have been released. RESETN should not be released after HALTN.

When V_{DD} is initially applied to the SCC68070, an external RESET must be applied to the RESETN pins for at least 100 ms.

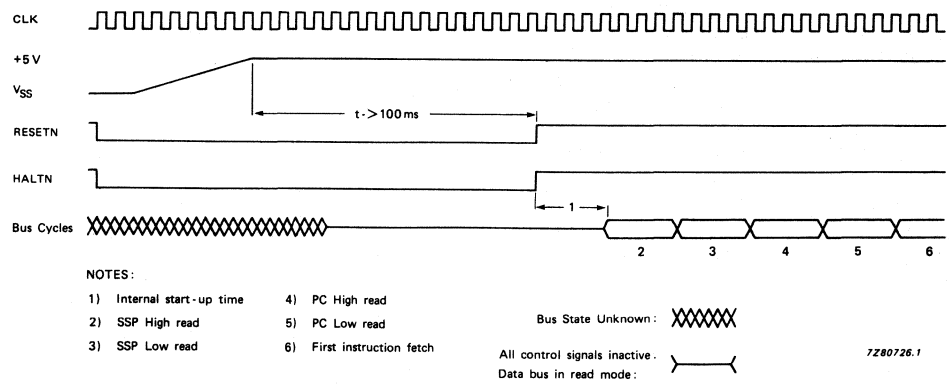


Fig.12 Reset timing.

Bus error processing

Like the 68000 the SCC68070 uses the BUS ERROR (BERRN) and the HALT signals to distinguish between two bus-error handling routines. If the BERRN and HALTN signals are asserted, the SCC68070 will re-run the last bus cycle as soon as both BERRN and HALTN lines are released. This is valid for both the CPU and DMA controller. BERRN should become inactive before HALTN (see Fig.13). If just the BERRN signal is asserted, bus error exception processing is entered. If the DMA controller is the affected master, it will:

- stop the DMA service after the current bus cycle is terminated
- release the bus
- set the BERRN bit in the status word, and
- send an interrupt if the INTERRUPT ENABLE bit in CCR (3) was set.

The address counter reflects the address of the faulty bus cycle, while the transfer counter indicates the number of successful transfers.

If the CPU is the bus master, it will enter the bus error exception processing after the current bus cycle is terminated and BERRN has been released. Since the architecture of the SCC68070 differs from the 68000, it handles bus errors in a different manner. Unlike the 68000, the SCC68070 enables full recovery from bus errors.

The procedure follows the usual sequence of steps:

- the status register is copied internally
- the supervisor state is entered
- the trace state is turned off, and
- the vector number is generated to refer to the bus error vector.

To save more of the context, additional information is stored on the stack as follows:

- The program counter and a copy of the status register are saved.
- A format word containing a special bit configuration for the SCC68070 long stack format, and the vector number of the exception, in this case, the bus error vector, is stacked.
- Besides other internal information, the processor saves the address which was being accessed by the aborted bus cycle.
- Specific information about the access is either saved or is retrievable from stacked information.
- A special status word is saved to determine the state of the (internal) function codes, the source of the bus error (MMU or External), and whether the error occurred during a read or write cycle. A RERUN bit in this special status word has to be set to suppress a retry of the faulty bus cycle on Return from Exception (RTE).
- The instruction registers and temporary registers are saved.

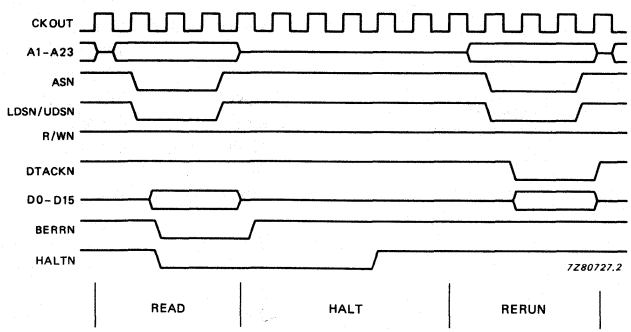


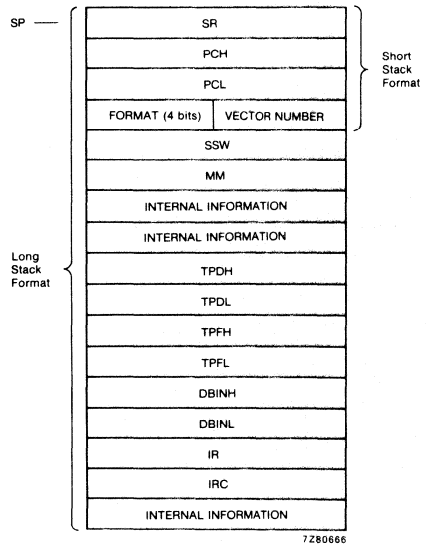
Fig.13 RERUN bus cycle timing.

SCC68070 stack format

The stacking operation for the exception processing is similar to the 68010 (rather than the 68000) however, the information stored is not the same due to the different architecture. To handle this, the following changes from the 68000 have been made:

- The stack format has changed.
- The minimum number of words put in or restored from the stack is 4 (short stack format) which is 68010 compatible; not 3 as for the 68000.
- The RTE instruction decides (with the aid of the 4 format bits) whether more information has to be restored. The SCC68070 long format is used for bus error and address error exceptions, all other exceptions use the short format.
- If another format code other than one of the two listed above is detected during the restore action, a FORMAT ERROR occurs.

If the user wants to finish the instruction in which the bus or address error occurred (modification of the stack), the SCC68070 format must be used on RTE. If no changes are required to the stack during exception processing, the stack format is transparent to the user.
The stack format is shown in Fig.14 and the special status word shown in Fig.15.



SR	Status Register.
PCH/PCL	Program Counter High/Low Word.
Format	Indicating either a short stack (only the first 4 words), or the long SCC68070 format for bus and address error exceptions.
Vector number	The vector number of the exception in the vector table; e.g. 2 for a bus error and 3 for an address error.
SSW	Special Status Word (see Fig.15).
MM	Current Move Multiple Mask.
TDPH/TDPL	In the event of a faulty write cycle, the data can be found here.
TPFH/TPFL	The address used during the faulty bus cycle.
DBINH/DBINL	Data that has been read prior to the faulty cycle can in some cases be found here.
IR	Holds the present instruction executed.
IRC	Holds either the present instruction executed or the prefetched instruction.

Fig.14 Stack format.

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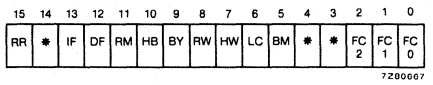


RR	Rerun. By default this bit is set to '0'. If set to '1' the CPU will not re-run the faulty bus cycle on return from exception (RTE).
*	Undefined (reserved).
iF	The faulty cycle was an instruction fetch.
DF	The faulty cycle was a data fetch.
RM	The error occurred during a readmodify-write cycle.
HB	High Byte.
BY	The faulty cycle was a byte transfer.
RW	Read/write cycle.
HW	High Word.
LC	The faulty cycle was during a longword access.
BM	The bus error was caused by the onchip MMU.
FC2,1,0	These bits hold the internal function code during the faulty bus cycle. The function codes are same as for the 68000 and affect the status of the CPU during the faulty bus cycle as follows.

FC2	FC1	FC0	
0	0	0	reserved
0	0	1	user data
0	1	0	user program
0	1	1	reserved
1	0	0	reserved
1	0	1	supervisor data
1	1	0	supervisor program
1	1	1	interrupt acknowledge

Fig.15 Special status word.

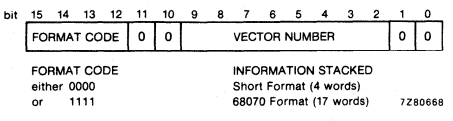


Fig.16 Vector number and format code.

Interrupt processing

The SCC68070 interrupt handling follows the same basic rules as the 68000. However, the following changes have been made to simplify system development:

- the IPL signals have been replaced by decoded interrupt signals IN2N, IN4N, IN5N and NMIN representing levels 2, 4, 5 and 7 respectively
- each of the interrupts has a separate acknowledge signal IACK2N, IACK4N, IACK5N and IACK7N
- two latched interrupt inputs (iNT1N and iNT2N) have programmable priority levels. They have no interrupt acknowledge signal and are always served by autovectoring with vectors located in the 'on-chip' entry in the vector table
- interrupt priority levels IPL1, IPL3 and IPL6 are not available externally, unless programmed into INT1N or INT2N
- if autovectoring is desired for IN2N, IN4N, IN5N or NMIN, the AUTOVECTOR request signal (AVN) must be asserted during the interrupt acknowledge routine.
- if more than one interrupt line is asserted at the same time, the one with the highest priority will be serviced first
- to ensure being recognized, an interrupt signal IN2N, IN4N, IN5N and NMIN must stay asserted until acknowledged by its IACK1N or IACK2N signal
- interrupts with a priority level equal to or less than the priority level actually running will not be accepted
- during the acknowledge cycle of an interrupt, the IPL bits of the status register are set to the priority level of the acknowledged interrupt.

If the priority of the interrupt pending is greater than the current processor priority then:

- the exception processing sequence is started
- a copy of the status register is saved
- the privilege level is set to supervisor state
- tracing is suppressed
- the priority level of the processor is set to that of the interrupt being acknowledged.

The processor then gets the vector number from the interrupting device, classifies it as an interrupt acknowledge, and displays the interrupt level number being acknowledged on the address bus.

During the interrupt acknowledge cycle ASN is asserted to indicate that the bus is occupied but LDSN is not asserted (note: the 68000 asserts both ASN and LDSN). This is done to simplify the address decoding circuitry of the memory. Acknowledge cycle decoding (by the interrupting device) is done using the IACK1N (or IACK2N) signal instead.

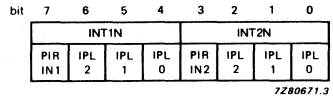
If autovectoring is requested by the internal logic, the processor generates a vector number internally that corresponds to the interrupt level number. Then, if a bus error is indicated by the external logic, the interrupt is treated as spurious and the vector number that was generated will refer to the spurious interrupt vector.

Priority level 7 is a special case and its interrupts cannot be inhibited by the interrupt priority mask thus providing a Non-Maskable Interrupt (NMIN) capability. An interrupt is generated each time the interrupt request level changes from a lower level to level 7.

If external and on-chip peripherals are programmed to the same interrupt priority level, an on-chip daisy-chain defines the priority as follows:

external interrupts	IN1N, IN2N	highest priority
	INT1N	
	INT2N	
	TIMER	
	UART RX	
	UART TX	
	I²C	
	DMA CH1	
	DMA CH2	lowest priority

The two latched interrupt inputs INT1N and INT2N have a common Latched Interrupt priority level register (LIR) as shown in Fig.17.



INT1N and INT2N refer to the external pins.

IPL — Interrupt priority level of interrupts connected externally to pins INT1N or INT2N. IPL2 is the MSB and IPL0 the LSB. All values are positive true; IPL = 111 represents priority level 7 and IPL = 000 will inhibit the interrupts.

PIR — Pending Interrupt Reset, when set to '1' any pending interrupts of the respective interrupt input will be reset and the inputs must be toggled again to create another interrupt. Note that this does not reset the interrupting status of a connected peripheral and further, if the IPL bits are changed without setting the PIR bit then spurious interrupts may occur. Reading the PIR bits will return zeros.

note: Initially and after RESET, all LIR bits are cleared to zero.

Fig.17 Latched Interrupt priority level Register (LIR).

On-chip addresses

All memory locations on the peripheral side of the on-chip interface can only be accessed in SUPERVISOR mode; i.e. the S-bit in the Processor Status Word (PSW) is set to '1'. If in USER mode (S = '0'), an external bus access is performed. All registers on the peripheral side of the interface are memory mapped separately from the 68070's external 16 Mbyte memory map. The on-chip address space is decoded by the two MSBs of the 32-bit internal address and the S-bit of the processor status word, as shown in Table 3. The address map of all the on-chip peripherals is given in Table 4.

Table 3 A31, A30 and S-bit decoding

S	A31	A30	
X	0	0	external
X	0	1	external
1	1	0	internal
0	1	0	external
X	1	1	external

Table 4 Address map of on-chip peripherals.

address range (HEX)			description
00000000	to	7FFFFFFF	off-chip
80000000	to	80001000	on-chip, reserved
80001001			LIR priority level
80001002	to	80002000	on-chip, reserved
80002001	to	80002009	I²C interface
8000200A	to	80002010	on-chip, reserved
80002011	to	8000201B	UART interface
8000201C	to	8000201F	on-chip, reserved
80002020	to	80002029	TIMER
8000202A	to	80002024	on-chip reserved
80002045			PICR1
80002046			on-chip, reserved
80002047			PICR2
80002048	to	80003FFF	on-chip, reserved
80004000	to	8000406D	DMA controller
8000406E	to	80007FFF	on-chip, reserved
80008000	to	8000807F	MMU
80008080	to	BFFFFFFF	on-chip, reserved
C0000000	to	FFFFFFFF	off-chip

Clock circuitry

The clock signals required by the SCC68070 are generated from one master oscillator. Dividing this frequency by two gives the clock signals for the CPU, MMU and DMA. Dividing the master oscillator frequency by four provides the clock frequency for the UART and I²C interface. Dividing the master oscillator frequency by 192 gives the clock for the Timer.

When the master oscillator frequency differs from 19.6608 MHz and standard baud rates are required from the UART, it is possible to clock the UART separately by supplying externally a 4.9152 or 9.8304 MHz signal on the XCKI pin (see Fig.18). The Timer will still have a period of 192 times that of the master oscillator period. The speed of the I²C interface is programmable and may need to be programmed with a different division factor.

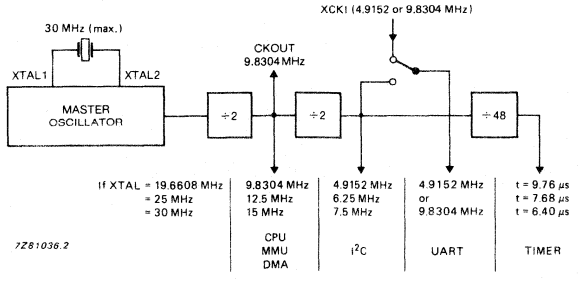


Fig.18 Clock circuitry.

INSTRUCTION SET AND ADDRESSING MODES

The SCC68070 is completely code compatible with the 68000 consequently programs developed for the 68000 will run on the SCC68070. This applies to both source and object code. The instruction set was designed to minimize the number of mnemonics that the programmer has to remember. Tables 5 and 6 give an overview of the instruction set and of the different addressing modes.

Table 5 Instruction set

mnemonic	description	operation	condition codes				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	(Destination)$_{10}$+(Source)$_{10}$→Destination	*	U	*	U	*
ADD	Add Binary	(Destination)+(Source)→Destination	*	*	*	*	*
ADDA	Add Address	(Destination)+(Source)→Destination	–	–	–	–	-
ADDI	Add Immediate	(Destination)+Immediate Data→Destination	*	*	*	*	*
ADDQ	Add Quick	(Destination)+Immediate Data→Destination	*	*	*	*	*
ADDX	Add Extended	(Destination)+(Source)+X→Destination	*	*	*	*	*
AND	AND Logical	(Destination) Λ (Source)→Destination	–	*	*	0	0
ANDI	AND Immediate	(Destination) Λ Immediate Data→Destination	–	*	*	0	0
ASL, ASR	Arithmetic Shift	(Destination) Shifted by <count>→Destination	*	*	*	*	*
Bcc	Branch Conditionally	If CC then PC+d→PC	–	–	–	–	-
BCHG	Test a Bit and Change	~(<bit number>) OF Destination→Z	–	–	*	–	-
		~(<bit number>) OF Destination→	–	–	*	–	-
		< bit number> OF Destination	–	–	*	–	-
BCLR	Test a Bit and Clear	~(<bit number>) OF Destination→Z	–	–	*	–	-
		0→<bit number>→ OF Destination	–	–	*	–	-
BRA	Branch Always	PC+d→PC	–	–	–	–	-
BSET	Test a Bit and Set	~(<bit number>) OF Destination→Z	–	–	*	–	-
		1→<bit number> OF Destination	–	–	*	–	-
BSR	Branch to Subroutine	PC→SP@-;PC+d→PC	–	–	–	–	-
BTST	Test a Bit	~(<bit number>) OF Destination→Z	–	–	–	–	-
CHK	Check Register against Bounds	If Dn<0 or Dn>(<ea>) then TRAP	–	*	U	U	U
CLR	Clear an Operand	0→Destination	–	0	1	0	0
CMP	Compare	(Destination)-(Source)	–	*	*	*	*
CMPA	Compare Address	(Destination)-(Source)	–	–	*	*	*
CMPI	Compare Immediate	(Destination)-Immediate Data	–	*	*	*	*
CMPM	Compare Memory	(Destination)-(Source)	–	*	*	*	*
DBcc	Test Condition, Decrement and Branch	If CC then Dn-1→Dn; if Dn -1 then PC+d→PC	–	–	–	–	-
DIVS	Signed Divide	(Destination)/(Source)→Destination	–	*	*	*	0
EOR	Exclusive OR Logical	(Destination)⊕(Source)→Destination	–	*	*	0	0
EORI	Exclusive OR Immediate	(Destination)⊕Immediate Data→Destination	–	*	*	0	0
EXG	Exchange Register	Rx↔Ry	–	–	–	–	-
EXT	Sign Extend	(Destination)Sign-extended→Destination	–	*	*	0	0
JMP	Jump	Destination→PC	–	–	–	–	-
JSR	Jump to Subroutine	PC→SP@-; Destination→PC	–	–	–	–	-
LEA	Load Effective Address	Destination→An	–	–	–	–	-
LINK	Link and Allocate	AN→SP@-; SP→An; SP+d→SP	–	–	–	–	-
LSL, LSR	Logical Shift	(Destination)Shifted by <count>→Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source)→Destination	–	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source)→CCR	*	*	*	*	*

mnemonic	description	operation	condition codes				
			X	N	Z	V	C
MOVE to SR	Move to the Status Register	(Source)→SR	*	*	*	*	*
MOVE from SR	Move from the Status Register	SR→Destination	–	–	–	–	-
MOVE USP	Move User Stack Pointer	USP→An; An→USP	–	–	–	–	-
MOVEA	Move Address	(Source)→(Destination)	–	–	–	–	-
MOVEM	Move Multiple Registers	Registers→Destination	–	–	–	–	-
		(Source)→Registers	–	–	–	–	-
MOVEP	Move Peripheral Data	(Source)→Destination	–	–	–	–	-
MOVEQ	Move Quick	Immediate Data→Destination	–	*	*	0	0
MULS	Signed Multiply	(Destination)*(Source)→Destination	–	*	*	0	0
MULU	Unsigned Multiply	(Destination)*(Source)→Destination	–	*	*	0	0
NBCD	Negate Decimal with Extend	$0-(Destination)_{10}-X→Destination$	*	U	*	U	*
NEG	Negate	0-(Destination)→Destination	*	*	*	*	*
NEGX	Negate with Extend	0-(Destination)-X→Destination	*	*	*	*	*
NOP	No Operation	–	–	–	–	–	-
NOT	Logical complement	~(Destination)→Destination	–	*	*	0	0
OR	Inclusive OR Logical	(Destination) v (Source)→Destination	–	*	*	0	0
ORI	Inclusive OR Immediate	(Destination) v Immediate Data→Destination	–	*	*	0	0
PEA	Push Effective Address	Destination→SP@-	–	–	–	–	-
RESET	Reset External Devices	–	–	–	–	–	-
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by <count>→Destination	–	*	*	0	*
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by <count>→Destination	*	*	*	0	*
RTE	Return from Exception	SP@+→SR; SP@+→PC	*	*	*	*	*
RTR	Return and Restore Condition Codes	SP@+→CC; SP@+→PC	*	*	*	*	*
RTS	Return from Subroutine	SP@+→PC	–	–	–	–	-
SBCD	Subtract Decimal with Extend	$(Destination)_{10}-(Source)_{10}-X→Destination$	*	U	*	U	*
Scc	Set According to Condition	If CC then 1's→Destination else 0's→Destination	–	–	–	–	-
STOP	Load Status Register and Stop	Immediate Data→SR; STOP	*	*	*	*	*
SUB	Subtract Binary	(Destination)-(Source)→Destination	*	*	*	*	*
SUBA	Subtract Address	(Destination)-(Source)→Destination	–	–	–	–	-
SUBI	Subtract Immediate	(Destination)-Immediate Data→Destination	*	*	*	*	*
SUBQ	Subtract Quick	(Destination)-Immediate Data→Destination	*	*	*	*	*
SUBX	Subtract with Extend	(Destination)-(Source)-X→Destination	*	*	*	*	*
SWAP	Swap Register Halves	Register [31:16]↔Register [15:0]	–	*	*	0	0
TAS	Test and Set Operand	(Destination) Tested→CC, 1→[7] OF Destination	–	*	*	0	0
TRAP	Trap	PC→SSP@-; SR→SSP@-; (Vector)→PC	–	–	–	–	-
TRAPV	Trap on overflow	If V then TRAP	–	–	–	–	-
TST	Test an Operand	(Destination) Tested→CC	–	*	*	0	0
UNLK	Unlink	An→SP; SP@+→An	–	–	–	–	-

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Notes to Table 5

1. [ ] = bit number
2. * affected
3. - unaffected
4. 0 cleared
5. 1 set
6. U defined
7. @ location addressed by

Notes to Tables 5 to 19

EA	=	Effective Address	PC	=	Program Counter
An	=	Address Register	()	=	Contents of
Dn	=	Data Register	d_8	=	8-bit offset (displacement)
Xn	=	Address or Data Register used as index register	d_{16}	=	16-bit offset (displacement)
N	=	1 for bytes, 2 for words and 4 for long words	SP	=	Stack Pointer
←	=	Replaces	SSP	=	System Stack Pointer
SR	=	Status Register	USP	=	User Stack Pointer

Table 6 Data addressing modes

mode	generation
Register Direct Addressing	
Data Register Direct	EA = Dn
Address Register Direct	EA = An
Absolute Data Addressing	
Absolute Short	EA = (Next Words)
Absolute Long	EA = (Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA = (PC)+d_{16}
Relative with Index and Offset	EA = (PC)+(Xn)+d_8
Register Indirect Addressing	
Register Indirect	EA = (An)
Postincrement Register Indirect	EA = (An), An←An+N
Predecrement Register Indirect	An←An–N, EA = (An)
Register Indirect with Offset	EA = (An)+d_{16}
Indexed Register Indirect with Offset	EA = (An)+(Xn)+d_8
Immediate Data Addressing	
Immediate	DATA = Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA = SR, USP, SSP, PC, SP

INSTRUCTION TIMING

Table 7 Effective address calculation times

	addressing Mode	.B	.W		.L
Rn	Data or Address Register Direct	0	(0/0)	0	(0/0)
(An)	Address Register Indirect	4	(1/0)	8	(2/0)
(An)+	Address Register Indirect postincrement	4	(1/0)	8	(2/0)
-(An)	Address Register Indirect predecrement	7	(1/0)	11	(2/0)
d(An)	Address Register Indirect Displacement	11	(2/0)	15	(3/0)
d(An,Xi)	Address Register Indirect with Index	14	(2/0)	18	(3/0)
xxx.S	Absolute Short	8	(2/0)	12	(3/0)
xxx.L	Absolute Long	12	(3/0)	16	(4/0)
d(PC)	Program Counter with Displacement	11	(2/0)	15	(3/0)
d(PC,Xi)	Program Counter with Index	14	(2/0)	18	(3/0)
#xxx	Immediate	4	(1/0)	8	(2/0)

The number of bus read and write cycles are shown in parenthesis.

Note. In Tables 8 to 19 clock period is twice the crystal oscillator period.

Table 8 MOVE Byte and MOVE Word instruction clock periods

	Rn	(An)	(An)+	-(An)	d(An)	d(An,iX)	xxx.S	xxx.L
Rn	7 (1/0)	11 (1/1)	11 (1/1)	14 (1/1)	18 (2/1)	21 (2/1)	15 (2/1)	19 (3/1)
(An)	11 (2/0)	15 (2/1)	15 (2/1)	18 (2/1)	22 (3/1)	25 (3/1)	19 (3/1)	23 (4/1)
(An)+	11 (2/0)	15 (2/1)	15 (2/1)	18 (2/1)	22 (3/1)	25 (3/1)	19 (3/1)	23 (4/1)
-(An)	14 (2/0)	18 (2/1)	18 (2/1)	21 (2/1)	25 (3/1)	28 (3/1)	22 (3/1)	26 (4/1)
d(An)	18 (3/0)	22 (3/1)	22 (3/1)	25 (3/1)	29 (4/1)	32 (4/1)	26 (4/1)	30 (5/1)
d(An,Xi)	21 (3/0)	25 (3/1)	25 (3/1)	28 (3/1)	32 (4/1)	35 (4/1)	29 (4/1)	33 (5/1)
xxx.S	15 (3/0)	19 (3/1)	19 (3/1)	22 (3/1)	26 (4/1)	29 (4/1)	23 (4/1)	27 (5/1)
xxx.L	19 (4/0)	23 (4/1)	23 (4/1)	26 (4/1)	30 (5/1)	33 (5/1)	27 (5/1)	31 (6/1)
d(PC)	18 (3/0)	22 (3/1)	22 (3/1)	25 (3/1)	29 (4/1)	32 (4/1)	26 (4/1)	30 (5/1)
d(PC,Xi)	21 (3/0)	25 (3/1)	25 (3/1)	28 (3/1)	32 (4/1)	35 (4/1)	29 (4/1)	33 (5/1)
#xxx	11 (2/0)	15 (2/1)	15 (2/1)	18 (2/1)	22 (3/1)	25 (3/1)	19 (3/1)	23 (4/1)

Table 9 MOVE long instruction clock periods

	Rn	(An)	(An)+	-(An)	d(An)	d(An,iX)	xxx.S	xxx.L
Rn	7 (1/0)	15 (1/2)	15 (1/2)	18 (1/2)	22 (2/2)	25 (2/2)	19 (2/2)	23 (3/2)
(An)	15 (3/0)	23 (3/2)	23 (3/2)	26 (3/2)	30 (4/2)	33 (4/2)	27 (4/2)	31 (5/2)
(An)+	15 (3/0)	23 (3/2)	23 (3/2)	26 (3/2)	30 (4/2)	33 (4/2)	27 (4/2)	31 (5/2)
-(An)	18 (3/0)	26 (3/2)	26 (3/2)	29 (3/2)	33 (4/2)	36 (4/2)	30 (4/2)	34 (5/2)
d(An)	22 (4/0)	30 (4/2)	30 (4/2)	33 (4/2)	37 (5/2)	40 (5/2)	34 (5/2)	38 (6/2)
d(An,Xi)	25 (4/0)	33 (4/2)	33 (4/2)	36 (4/2)	40 (5/2)	43 (5/2)	37 (5/2)	41 (6/2)
xxx.S	19 (4/0)	27 (4/2)	27 (4/2)	30 (4/2)	34 (5/2)	37 (5/2)	31 (5/2)	35 (6/2)
xxx.L	23 (5/0)	31 (5/2)	31 (5/2)	34 (5/2)	38 (6/2)	41 (6/2)	35 (6/2)	39 (7/2)
d(PC)	22 (4/0)	30 (4/2)	30 (4/2)	33 (4/2)	37 (5/2)	40 (5/2)	34 (5/2)	38 (6/2)
d(PC,Xi)	25 (4/0)	33 (4/2)	33 (4/2)	36 (4/2)	40 (5/2)	43 (5/2)	37 (5/2)	41 (6/2)
#xxx	15 (3/0)	23 (3/2)	23 (3/2)	26 (3/2)	30 (4/2)	33 (4/2)	27 (4/2)	31 (5/2)

Table 10 Standard instruction clock periods

	size	op <ea>,An	op <ea>,Dn	op Dn,<M>
ADD/ADDA	.B .W	7+(1/0)	7+(1/0)	11+(1/1)
	.L	7+(1/0)	7+(1/0)	15+(1/2)
ADD	.B .W	–	7+(1/0)	11+(1/1)
	.L	–	7+(1/0)	15+(1/2)
CMP/CMPA	.B .W	7+(1/0)	7+(1/0)	-
	.L	7+(1/0)	7+(1/0)	-
DIVS	–	–	169+**(1/0)	-
DIVU	–	–	130+*(1/0)	-
EOR	.B .W	–	7+(1/0)***	11+(1/1)
	.L	–	7+(1/0)***	15+(1/2)
MULS	–	–	76+*(1/0)	-
MULU	–	–	76+*(1/0)	-
OR	.B .W	–	7+(1/0)	11+(1/1)
	.L	–	7+(1/0)	15+(1/2)
SUB	.B .W	7+(1/0)	7+(1/0)	11+(1/1)
	.L	7+(1/0)	7+(1/0)	15+(1/2)

\+ add effective address calculation time
* the duration of the instruction is constant
** indicates maximum value
*** only effective address mode is data register direct

Table 11 Immediate instruction clock periods

	size	op <#>,Dn	op <#>,An	op <#>,<M>
ADDI	.B .W	14 (2/0)	–	18+(2/1)
	.L	18 (3/0)	–	26+(3/2)
ADDQ	.B .W	7 (1/0)	7 (1/0)	11+(1/1)
	.L	7 (1/0)	7 (1/0)	15+(1/2)
ANDI	.B .W	14 (2/0)	–	18+(2/1)
	.L	18 (3/0)	–	26+(3/2)
CMPI	.B .W	14 (2/0)	–	14+(2/0)
	.L	18 (3/0)	–	18+(3/0)
EORI	.B .W	14 (2/0)	–	18+(2/1)
	.L	18 (3/0)	–	26+(3/2)
MOVEQ	.L	7 (1/0)	–	-
ORI	.B .W	14 (2/0)	–	18+(2/1)
	.L	18 (3/0)	–	26+(3/2)
SUBI	.B .W	14 (2/0)	–	18+(2/1)
	.L	18 (3/0)	–	26+(3/2)
SUBQ	.B .W	7 (1/0)	7 (1/0)	11+(1/1)
	.L	7 (1/0)	7 (1/0)	15+(1/2)

\+ add effective address calculation time

Table 12 Single operands instruction clock periods

instruction	size	register	memory
CLR	Byte, Word	7 (1/0)	11 (1/1)+*
	Long	7 (1/0)	15 (1/2)+**
NBCD	Byte	10 (1/0)	14 (1/1)+
NEG	Byte, Word	7 (1/0)	11 (1/1)+
	Long	7 (1/0)	15 (1/2)+
NEGX	Byte, Word	7 (1/0)	11 (1/2)+
	Long	7 (1/0)	15 (1/2)+
NOT	Byte, Word	7 (1/0)	11 (1/1)+
	Long	7 (1/0)	15 (1/2)+
Scc	Byte, Word	13 (1/0)	17 (1/1)+
	Long	13 (1/0)	14 (1/1)+
TAS	Byte	10 (1/0)	15 (1/1)+*
TST	Byte, Word	7 (1/0)	7 (1/0)+
	Long	7 (1/0)	7 (1/0)+

+ add effective address calculation time

* subtract one read cycle (-4(1/0)) from effective address calculation

** Subtract two read cycles (-8(2/0)) from effective address calculation

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Table 13 Shift/rotate instruction clock periods

instruction	size	register	memory
ASR, ASL	Byte, Word	13 + 3n (1/0)	14 (1/1)+
	Long	13 + 3n (1/0)	-
LSR, LRL	Byte, Word	13 + 3n (1/0)	14 (1/1)+
	Long	13 + 3n (1/0)	-
ROR, ROL	Byte, Word	13 + 3n (1/0)	14 (1/1)+
	Long	13 + 3n (1/0)	-
ROXR, ROXL	Byte, Word	13 + 3n (1/0)	14 (1/1)+
	Long	13 + 3n (1/0)	-

+ add effective address calculation time

Table 14 Bit manipulation instruction clock periods

instruction	size	dynamic		static	
		register	memory	register	memory
BCHG	Byte	-	14 (1/1)+	–	21 (2/1)+
	Long	10 (1/0)	–	17 (2/0)	-
BCLR	Byte	–	14 (1/1)+	–	21 (2/1)+
	Long	10 (1/0)	–	17 (2/0)	-
BSET	Byte	–	14 (1/1)+	–	21 (2/1)+
	Long	10 (1/0)	–	17 (2/0)	-
BTST	Byte	–	7 (1/0)+	–	14 (2/0)+
	Long	7 (1/0)	–	14 (2/0)	-

+ add effective address calculation time

Table 15 Conditional instruction clock periods.

instruction	displ.	trap/branch taken	trap/branch not taken
Bcc	.B	13 (1/0)	13 (1/0)
	.W	14 (2/0)	14 (2/0)
BRA	.B	13 (1/0)	-
	.W	14 (2/0)	-
BSR	.B	17 (1/2)	-
	.W	22 (2/2)	-
DBcc	ccTrue	–	14 (2/0)
	ccFalse	17 (2/0)	17 (2/0)
CHK	–	64 (3/5)+	19 (1/0)+
TRAPV	–	55 (3/4)	10 (1/0)

+ add effective address calculation time

Table 16 JMP, JSR, LEA, PEA, MOVEM instruction clock periods.

	size	(An)	(An)+	-(An)	d(An)	d(An,Xi)	xxx.S	xxx.L	d(PC)	d(PC,Xi)
JMP	–	7	–	–	14	17	14	18	14	17
	–	(1/0)	–	–	(2/0)	(2/0)	(2/0)	(3/0)	(2/0)	(2/0)
JSR	–	18	–	–	25	28	25	29	25	28
	–	(1/2)	–	–	(2/2)	(2/2)	(2/2)	(3/2)	(2/2)	(2/2)
LEA	–	7	–	–	14	17	14	18	14	17
	–	(1/0)	–	–	(2/0)	(2/0)	(2/0)	(3/0)	(2/0)	(2/0)
PEA	–	18	–	–	25	28	25	29	25	28
	–	(1/2)	–	–	(2/2)	(2/2)	(2/2)	(3/2)	(2/2)	(2/2)
MOVEM M→R	.W	26+7n	26+7n	–	30+7n	33+7n	30+7n	34+7n	30+7n	33+7n
		(2+n/0)	(2+n/0)	–	(3+n/0)	(3+n/0)	(3+n/0)	(4+n/0)	(3+n/0)	(3+n/0)
	.L	26+11n	26+11n	–	30+11n	33+11n	30+11n	34+11n	30+11n	33+11n
		(2+2n/0)	(2+2n/0)	–	(3+2n/0)	(3+2n/0)	(3+2n/0)	(4+2n/0)	(3+2n/0)	(3+2n/0)
MOVEM R→M	.W	23+7n	–	23+7n	27+7n	30+7n	27+7n	31+7n	–	-
		(2/n)	–	(2/n)	(3/n)	(3/n)	(3/n)	(4/n)	–	-
	.L	23+11n	–	23+11n	27+11n	30+11n	27+11n	31+11n	–	-
		(2/2n)	–	(2/2n)	(3/2n)	(3/2n)	(3/2n)	(4/2n)	–	-

n = number of registers to move

Table 17 Multi-precision instruction clock periods

instruction	size	op Dn, Dn	op M, M
ADDX	Byte, Word	7 (1/0)	28 (3/1)
	Long	7 (1/0)	40 (5/2)
CMPM	Byte, Word	-	18 (3/0)
	Long	-	26 (5/0)
SUBX	Byte, Word	7 (1/0)	28 (3/1)
	Long	7 (1/0)	40 (5/2)
ABCD	Byte	10 (1/0)	31 (3/1)
SBCD	Byte	10 (1/0)	31 (3/1)

Table 18 Miscellaneous clock periods

instruction	size	register	memory	register to memory	memory to register
ANDI to CCR	–	14 (2/0)	–	–	-
ANDI to SR	–	14 (2/0)	–	–	-
EORI to CCR	–	14 (2/0)	–	–	-
EORI to SR	–	14 (2/0)	–	–	-
EXG	–	13 (1/0)	–	–	-
EXT	Word	7 (1/0)	–	–	-
	Long	7 (1/0)	–	–	-
LINK	–	25 (2/2)	–	–	-
MOVE from SR	–	7 (1/0)	11/11+	–	-
MOVE to CCR	–	10 (2/0)	10 (2/0)+	–	-
MOVE to SR	–	10 (2/0)	10 (2/0)+	–	-
MOVE from USP	–	7 (1/0)	–	–	-
MOVE to USP	–	7 (1/0)	–	–	-
MOVEP	Word	–	–	25 (2/2)	22 (4/0)
	Long	–	–	39 (2/4)	36 (6/0)
NOP	–	7 (1/0)	–	–	-
ORI to CCR	–	14 (2/0)	–	–	-
ORI to SR	–	14 (2/0)	–	–	-
RESET	–	154 (2/0)	–	–	-
RTE					
short format		39 (5/0)			
long format:					
no rerun		140 (18/0)			
with rerun		146 (18/0)			
rerun of TAS		151 (19/1)			
RTR	–	22 (4/0)	–	–	-
RTS	–	15 (3/0)	–	–	-
STOP	–	13 (0/0)	–	–	-
SWAP	–	7 (1/0)	–	–	-
UNLK	–	15 (3/0)	–	–	-

+ add effective address calculation time

Table 19 Exception processing clock periods

exception	No. of clock periods
Address error	158 (3/17)
Bus error	158 (3/17)
Interrupt	65 (4/4)*
Illegal instruction	55 (3/4)
Privilege violation	55 (3/4)
Trace	55 (3/4)
Trap	52 (3/4)
Divide by Zero	64 (3/4)+
RESET**	43 (4/0)

* The interrupt acknowledge bus cycle is assumed to take four external clock periods.

** Indicates the maximum time from when RESETN and HALTN are first sampled as negated to first instruction fetch.

DEVELOPMENT DATA

68070 ON-CHIP MMU

The SCC68070 has an on-chip Memory Management Unit (MMU) that if enabled, supports virtual memory, multitasking, task protection and dynamic stack allocation.

Segmentation

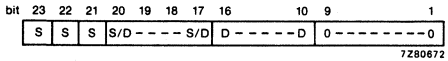
The MMU divides the memory into segments of multiples of 1 Kbyte (blocks). Two modes are possible:

mode	no. of segments	max. segment length
1	8	2048 blocks = 2 Mbytes
2	128	128 blocks = 128 Kbytes

Memory protection is assigned on a segment to segment basis.

For address translation, the logical address can be split into three parts (see Fig.19).

- segment number
- displacement
- offset

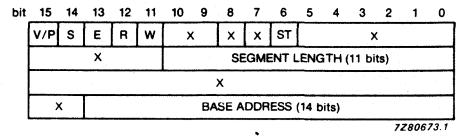


S = the segment number
S/D = either the segment number or a displacement, as defined by the MMU Control Register (MCR)
D = displacement
O = offset

Fig.19 Logical address format.

Segment descriptors

Every segment is described by a segment descriptor stored in the segment descriptor table in main memory. Each descriptor contains a segment address field, a segment protection field (with protection attributes) and the segment length. However, for ease of access up to 8 descriptors can be stored in the on-chip descriptor RAM. The format of the descriptors in main memory is shown in Fig.20.



X = undefined, reserved

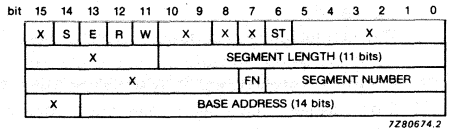
- Base Address: the 14 MSBs of the start address of this segment.
- V/P (Valid/Present) – may be used by the loading software to determine whether the segment is valid and present.
- S (Supervisor) – supervisor permission is required to access this segment.
- E (Execute) – instruction fetches may be performed with this segment.
- R (Read) – read operations may be performed with this segment.
- W (Write) – write operations may be performed with this segment.
- ST (Stack) – stack segments grow from high to low addresses.

Segment length: the 11 bits define the length of a segment by the number of 1 Kbyte blocks. (If the SN bit of the MMU Control Register (MCR) is set, placing the MMU in Mode 2, only 7 MSBs define the length of the segment.)

Note:
All bits indicated as 'undefined, reserved' must be programmed to zeros, except bit 8 of the first word which must be set to '1' to be compatible with the Memory Access Controllers of the 68000 family.

Fig.20 Format of descriptors in main memory

The format of the descriptor in the on-chip descriptor RAM is shown in Fig.21.
The low-order byte of the third word contains the segment number that is loaded into the fully associative CAM. The MSB of the segment number is in Bit 6 of this word, i.e. it is left justified for either mode of the segment number.



FN = FLUSH If this bit is equal to zero it invalidates the descriptor. Therefore, it must be reset to zero when writing a new valid segment number. The FN bit should be set to one after the remainder of the segment descriptor has been loaded into the MMU.

X = Undefined, reserved; will return zeros when ready by the CPU.

Fig.21 Descriptor format in MMU.

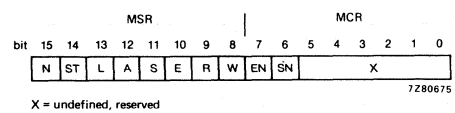


Fig.22 MMU Status and Control Registers (MSR and MCR).

MMU Control and Status Registers

The formats of the Control Register (MCR) and the Status Register (MSR) are shown in Fig.22.
The registers can be accessed as either one word or two separate bytes. MCR may be written to, or read from, but MSR is a read only register. Writing to MSR will result in a normal bus cycle with no effect.

Control Register (MCR)

Enable (MCR 7)

If the Enable bit EN is set the MMU is enabled (address translation and protection).
The default reset value is zero, inhibiting the MMU.

Number of segments (MCR 6)

The state of the SN bit determines the maximum number of segments the MMU is to handle.
When SN is '0', the maximum number of segments is 8 (Mode 1). When SN is '1', the maximum number of segments is 128 (Mode 2).
The default reset value is zero.

Status Register (MSR)

Not-present (MSR 15)

The Not-present bit N, is set by the MMU if the addressed segment has no descriptor in the MMU or when the FN bit in the descriptor is zero.

Stack Segment (MSR 14)

The Stack segment bit ST, indicates that the segment in which the error occurred was defined as a stack segment. If ST is set, the segment grows from the highest to lowest address.

Length violation (MSR 13)

The Length violation bit L, is set if the displacement given by the logical address exceeds the segment length given by the segment descriptor.

Access error (MSR 12)

The Access error bit A, is set by the MMU if an attribute violation occurred during the last bus access.

Descriptor attributes (MSR 11:8)

The Supervisor bit S (MSR 11), Execute bit E (MSR 10), Read bit R (MSR 9) and Write bit W (MSR 8) are permission bits and reflect the descriptor attributes when an access error has occurred.

DEVELOPMENT DATA

Address map of the MMU

The internal addresses of the MMU's registers and Descriptor RAM are given below:

Base address 8000 8000 (HEX)

A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	MSR
0	0	0	0	0	0	1	MCR
1	C	C	C	0	0	0/1	ATTR
1	C	C	C	0	1	0/1	SEG LENGTH
1	C	C	C	1	0	0	Undefined, reserved
1	C	C	C	1	0	1	SEG NUMBER
1	C	C	C	1	1	0/1	BASE ADDRESS

Notes

MSR = MMU Status Register
MCR = MMU Control Register
SEG = Segment
ATTR = Attributes
CCC = 000 to 111 (see Segment Descriptors 0 to 7).

All internal MMU addresses are mapped in the SCC68070's on-chip address space and are only accessible in Supervisor mode (see Tables 1 and 2). On-chip addresses are not processed by the MMU.

Operation

The MMU provides protection and virtual memory support. When the MMU is enabled it only influences addresses sent by the CPU and adds two SM states (or one clock cycle) at the beginning of each external bus cycle of the CPU. However, during the vector acquisition of an interrupt acknowledge cycle, the MMU does not process the address coming from the CPU; i.e. logical address equals physical address and the SM states are not added. The address translation is processed as follows:

1. The segment number S, of the logical address is used to address the segment descriptor stored in the MMU on-chip descriptor RAM. If this segment descriptor is not valid or not present, BERRN will be generated and corrective action must be taken to load the indicated segment descriptor and continue the interrupted instruction.
2. The displacement D, of the logical address is compared to the length attribute in the segment descriptor. If the displacement is outside the indicated length then BERRN is generated.
3. The internal function codes are used to check for access violations, using the attributes of the segment descriptor. In the event of a violation BERRN will be generated.
4. If no violations have been detected, a physical address will be generated. This address is constructed by adding the segment base address, the displacement D and the offset '0' bits. This is illustrated in Fig.23.

Error handling.

If an error occurs within the enabled MMU, the MMU inhibits data strobes (UDSN, LDSN) and asserts a bus error signal (BERRN) to both the CPU and the external world. The address strobe (ASN) will be asserted to indicate bus occupation to other possible bus masters. Then, the CPU will start bus error processing with the stack operation.

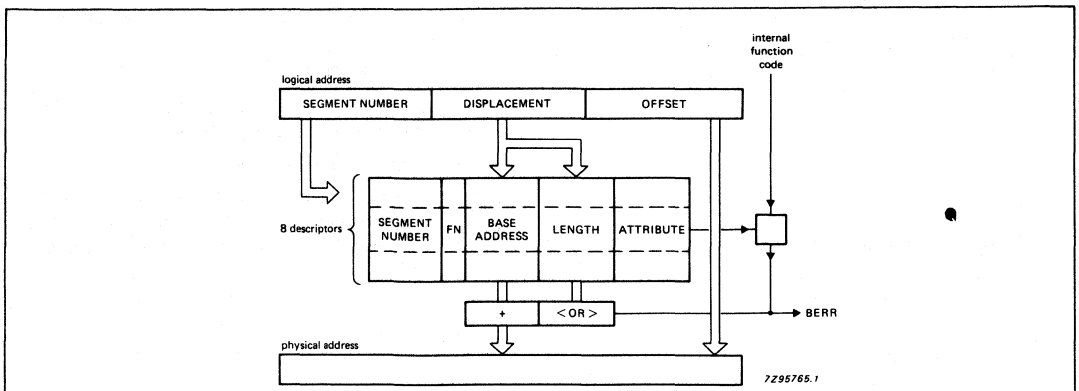


Fig.23 Principle of the MMU.

DMA CONTROLLER

General

The SCC68070 has on-chip, a two-channel DMA controller that handles byte or word operands, and devices with port sizes of 8 or 16-bits. The channels can be programmed to transfer data in cycle steal (single cycle) or burst (a block of successive cycles) mode. Channel 1 always uses single addressing, while Channel 2 can operate with single or dual addresses (memory to memory).
Typical system latency times are less than 1.7 µs and the maximum transfer rate (using single addressing) is 2.5 million transfers per second (crystal frequency 30 MHz).
The SCC68070's DMA controller is a subset of the existing DMA controllers in the 68000 family (68430, 68440 and 68450) and is therefore programmed similar to these devices.

Device/DMA controller communication

The following five signal lines enable peripheral devices and the DMA controller to communicate with each other. See pin description for further details.

- Request (REQ1N and REQ2N). The device makes a request for service by asserting the REQ1N (or REQ2N) line. Either burst or cycle steal mode can be used.
- ACKNOWLEDGE (ACK1N and ACK2N). The channel asserts the acknowledge line (which implicitly addresses the device making the request) during transfers to and from the device.
- READY (RDYN). RDYN is an active-LOW input which is asserted by the requesting device in single-address mode.
- Device Transfer Complete (DTCN). DTCN is an active LOW output asserted by the DMA controller during device bus cycles to indicate that the cycle has been completed successfully.
- Done (DONEN). DONEN is a bidirectional active-LOW signal. As an output it indicates to the device that the memory transfer count is exhausted. As an input, it indicates that the operation will terminate after current operand has been transferred. (See Termination phase).

Bus arbitration and priority resolution

The SCC68070 contains three possible bus masters, the DMA Channels 1 and 2 and the CPU, where Channel 1 has the highest priority and the CPU the lowest. There can also be external bus masters which have a priority lower than Channel 2 but higher than the CPU (which has the lowest priority in the system).

When a valid bus transfer request is received from a device, the DMA controller will arbitrate for and acquire the bus. The DMA controller indicates to the CPU that it wants to become bus master by generating an internal bus request signal, and the CPU responds by sending an internal bus grant signal, daisy-chained through the DMA controller. It is not offered to the external devices because the DMA controller has a request pending. If BGN has already been offered to the external devices when a DMA request arrives, the DMA controller waits for BGACKN to become inactive.
If the CPU is the current bus master, it will finish its current cycle and then give the bus to the DMA controller. When the DMA controller has received the internal bus grant signal, it waits for the external signals, Address Strobe (ASN) and Data Transfer Acknowledge (DACKN) to become inactive, it then assumes bus ownership.
If the BRN signal is asserted by an external device when the CPU is not the bus master (i.e. BGACKN is asserted) no BGN signal will be sent until the CPU has regained the bus (i.e. BGACKN is inactive.)

Registers and counters

The internal organization of the DMA controllers accessible registers is shown in Table 20. The following rules apply to all registers:

- A read from a reserved location in the map results in a read from the 'null register'. The null register register returns all ones for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle but no write occurs.
- Unused bits of a defined register are read as indicated in the register description.
- All registers are addressable as 8-bit quantities. Addresses are arranged so that certain sets of registers may also be accessed as either words or long words.

Compatibility with other 68000 family DMA controllers is provided by mapping control and status bits into bit positions which are equivalent to the register map of the other devices. Bits which are used in other devices but not in the DMA controller are assigned default values. If upward compatibility with the other devices is required, the programmer should use these default values when writing the control words to the registers; although they have no effect in the DMA controller. When a register is read, the default value is returned regardless of the value used when the register was programmed. The default value is indicated by '(x)' in unused bit positions in the register descriptions that follow.

Table 20 DMA controller address map

Base address 8000 4000 (HEX)

address bits[1], [2] 7	6	5	4	3	2	1	0	acronym	register name	mode	affected by RESET
c	c	0	0	0	0	0	0	CSR	Channel Status Register	R/W[3]	Yes
c	c	0	0	0	0	0	1	CER	Channel Error Register	R	Yes
c	c	0	0	0	0	1	0		Reserved		
c	c	0	0	0	0	1	1		Reserved		
c	c	0	0	0	1	0	0	DCR	Device Control Register	R/W	Yes
c	c	0	0	0	1	0	1	OCR	Operation Control Register	R/W	Yes
c	c	0	0	0	1	1	0	SCR	Sequence Control Register	R/W[4]	Yes
c	c	0	0	0	1	1	1	CCR	Channel Control Register	R/W	Yes
c	c	0	0	1	0	0	0		Reserved		
c	c	0	0	1	0	0	1		Reserved		
c	c	0	0	1	0	1	0	MTCH	Memory Transfer Counter High	R/W	No
c	c	0	0	1	0	1	1	MTCL	Memory Transfer Counter Low	R/W	No
c	c	0	0	1	1	0	0	MACH	Memory Address Counter High	R/W[4]	No
c	c	0	0	1	1	0	1	MACMH	Memory Address Counter Middle High	R/W	No
c	c	0	0	1	1	1	0	MACML	Memory Address Counter Middle Low	R/W	No
c	c	0	0	1	1	1	1	MACL	Memory Address Counter Low	R/W	No
c	c	0	1	0	0	d	d		Reserved		
c	c	0	1	0	1	0	0	DACH	Device Address Counter High	R/W[4], [5]	No
c	c	0	1	0	1	0	1	DACHMH	Device Address Counter Middle High	R/W[5]	No
c	c	0	1	0	1	1	0	DACML	Device Address Counter Middle Low	R/W[5]	No
c	c	0	1	0	1	1	1	DACL	Device Address Counter Low	R/W[5]	No
c	c	0	1	1	d	d	d		Reserved		
c	c	1	0	0	d	d	d		Reserved		
c	c	1	0	1	0	d	d		Reserved		
c	c	1	0	1	1	0	0		Reserved		
c	c	1	0	1	1	0	1	CPR	Channel Priority Register	R/W[4]	No
c	c	1	0	1	1	1	0		Reserved		
c	c	1	0	1	1	1	1		Reserved		
c	c	1	1	d	d	d	d		Reserved		

Notes to Table 20

1. 'cc' = 00 for channel 1, 'cc' = 01 for channel 2, 'cc' = 10 or 11 reserved.
2. 'd' designates don't care states.
3. A write to this register may perform a status reset operation.
4. This is a dummy register present only to provide compatibility with other 68000 family DMA controllers. A write to this register has no effect on the DMA controller.
5. Channel 2 only.

Device Control Register (DCR)

External Request Mode (DCR 15)

This bit selects whether the channel operates in either burst or cycle steal mode, as follows:

0 Burst Mode: This mode allows a device to request the transfer of multiple operands over consecutive bus cycles.

1 Cycle steal mode: This mode allows a device to transfer operands on a per cycle basis.

Device Type (DCR13:12) - Channel 1

These bits determine how a device is addressed, as follows:

11 The device connected is implicitly addressed by the 5 device control signals with handshake using ACK1N (or ACK2N) and RDYN.

Device Type (DCR13:12) - Channel 2.

These bits determine how a device is addressed, as follows:

00 The device is explicitly addressed by the Device Address Counter (DAC) via the SCC68070 bus interface. Transfers are made in two bus cycles; the data being stored in the CPU between cycles.

11 The device connected is implicitly addressed by the 5 device control signals with handshake using ACK1N (or ACK2N) and RDYN.

Device Size (DCR 11) - Channel 2 only

This bit functions only with explicitly addressed devices, DCR13:12 = 00

0 The device port size is 8-bit. The device reads/writes using only the low-order half of the bus (D0 to D7) or the high-order half (D8 to D15) depending on bit A0 of the Device Address Counter (DAC). Depending on which part of the bus is used either LDSN for the low-order part or UDSN for the high-order part is asserted. During byte size transfers (OCR 5:4 = 00) the half of the data bus used for read/write to the memory depends on the state of A0 of the Memory Address Counter (MAC). During word size transfers (OCR 5:4 = 01), read/write operations take place in two successive bytes; the DAC will either be unchanged or incremented by two per byte, depending on SCR 9:8 (see Fig.26)

1 The device port size is 16-bits and the device is accessed as a normal memory location.

Operation Control Register (OCR)

Direction (OCR 7)

0 Transfer is from memory to device.

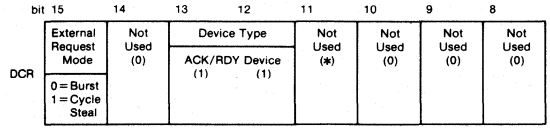
1 Transfer is from device to memory.

Operand size (OCR 5:4)

These bits determine whether UDSN, LDSN or both are generated during the transfer cycle and also to what value the address counters MAC and DAC (AC) are incremented by each transfer cycle.

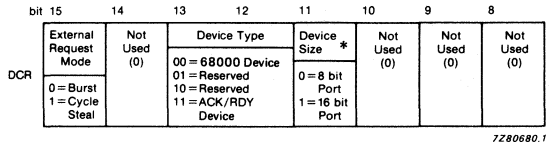
DEVELOPMENT DATA

Channel 1



* Must be 0 if OCR 5:4 = 00 (SIZE), otherwise 1. When read, the value of this bit is (OCR 5 or OCR 4).

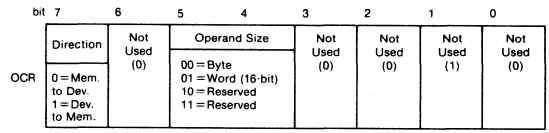
Channel 2



* This bit is programmable only when DCR 13:12 = 00 (68000 device). For DCR 13:12 = 11 (ACKx/RDY Device) the function is identical to Channel 1.

Fig.24 Device Control Registers (DCR).

Channel 1



Channel 2

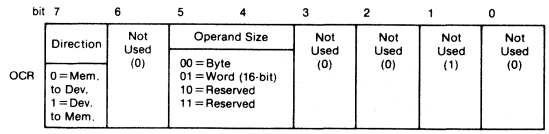


Fig.25 Operation Control Registers (OCR).

Sequence Control Register

MAC (SCR 11:10) - Channel 1

01 These bits are not programmable, the Memory Address Counter always counts upwards.

MAC (SCR 11:10) - Channel 2

00 The Memory Address Counter is not changed during transfers.

01 The Memory Address Counter is incremented by 1 or 2 during the transfer, depending on the operand size; OCR 5:4 (byte or word transfer).

DAC (SCR 9:8) - Channel 2 only

00 The Device Address Counter is not changed between transfers.

01 The Device Address Counter is incremented by 1 or 2 during the transfer, depending on the operand size; OCR 5:4 (byte or word transfer).

Channel Control Register (CCR)

Start Operation (CCR 7)

0 No Start pending

1 Start Operation. The start bit is set to initiate operation of the channel.

Software Abort (CCR 4)

0 Do not abort.

1 Abort Operation. Setting this bit terminates the current operation and puts it into the Idle state, then:

- The COC bit (CSR 15) and ERR bit (CSR 12) are set
- The Channel Active bit (CSR 11) is reset
- An Abort Error condition is signalled in the Channel Error Register (CER).

Setting this bit causes a pending start to be reset. When reading CCR this bit is always zero.

Interrupt Enable (CCR 3)

0 Interrupts not enabled.

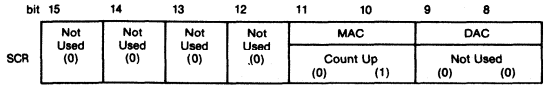
1 Interrupts enabled.

Interrupt Priority Level (CCR 2:0)

These three bits define the priority level of the interrupt given by the channel. 000 will cause no interrupt, 001 is the lowest and 111 is the highest interrupt priority.

DEVELOPMENT DATA

Channel 1



Channel 2

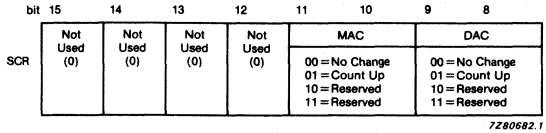
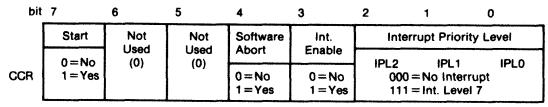


Fig.26 Sequence Control Registers (SCR).

Channel 1



Channel 2

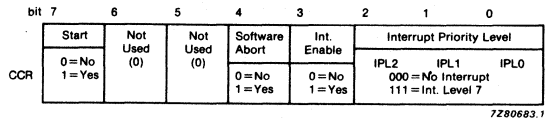


Fig.27 Channel Control Registers (CCR).

Channel Status Register (CSR)

This register is read to obtain the status of the channel.

COC bit (CSR 15)

This bit is set after the termination (whether successful or not) of any channel operation and indicates that the DMA transfer has been completed. It must be cleared before starting another channel operation.

NDT (CSR 13)

This bit is set when the device terminates channel operation by asserting DONEN while the device was being acknowledged. This bit must be cleared before another channel operation can start.

ERR (CSR 12)

This bit is used to report that channel operation has been terminated because of an error. By reading the Channel Error Register the cause of the error can be determined. This bit must be cleared before another channel operation can start. Clearing CSR 12 also clears the Channel Error Register.

Channel Active (CSR 11)

This bit is set automatically after channel operation has been started and remains set until channel operation terminates, whereupon it is automatically reset by the channel. This bit is not effected by write operations.

Bits CSR 15, CSR 13 and CSR 12 can be cleared by writing a '1' to the appropriate bit positions of the register. Writing a '0' to these bit positions has no effect.

Channel Error Register (CER)

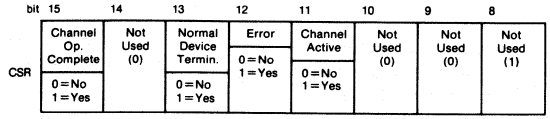
Error Code (CER 4:0)

This field indicates the source of the error when the ERR bit (CSR 12) is set. Clearing CSR 12 in the Channel Status Register also clears the Channel Error Register.

00000	No Error.
00010	Timing Error. An attempt has been made to start the channel before all the bits of the Channel Status Register have been cleared.
01001	Bus Error memory side. A bus error (BERRN asserted without HALTN) has occurred during the cycle with MAC presenting the address.
01010	Bus Error device side. A bus error (BERRN asserted without HALTN) occurred during the cycle with DAC presenting the address (Channel 2 only).
10001	Software Abort. The channel operation was aborted by a Software Abort command (CCR 4).

DEVELOPMENT DATA

Channel 1



Channel 2

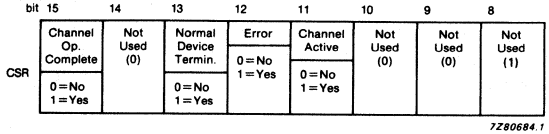
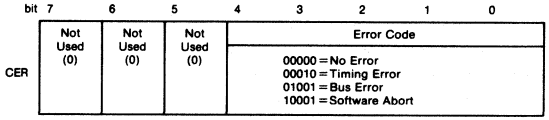


Fig.28 Channel Status Registers (CSR).

Channel 1



Channel 2

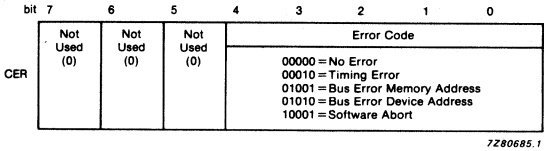


Fig.29 Channel Error Registers (CER).

Channel Priority Register (CPR)

CPR serves no function in the channel but is included only for programming compatibility with the other 68000 family DMA controllers. It contains the value '0' for Channel 1 and the value '1' for Channel 2.

Memory Address Counter (MACH, MACMH, MACML, MACL)

The 32-bit memory address counter defines a memory location as the source or destination of the operand to be transferred, depending on the direction of the transfer.
Only the least significant 24-bits of the counter (MACMH, MACML, and MACL) are implemented in the DMA controller.

Device Address Counter (DACH, DACMH, DACML, DACL) - Channel 2 only

The 32-bit device address counter defines a device location as the source or destination of the operand to be transferred, depending on the direction of the transfer.
Only the least significant 24-bits of the counter (DACMH, DACML, and DACL) are implemented in the DMA controller.

Memory Transfer Counter (MTCH, MTCL)

The 16-bit memory transfer counter defines the number of operands to be transferred by the channel.

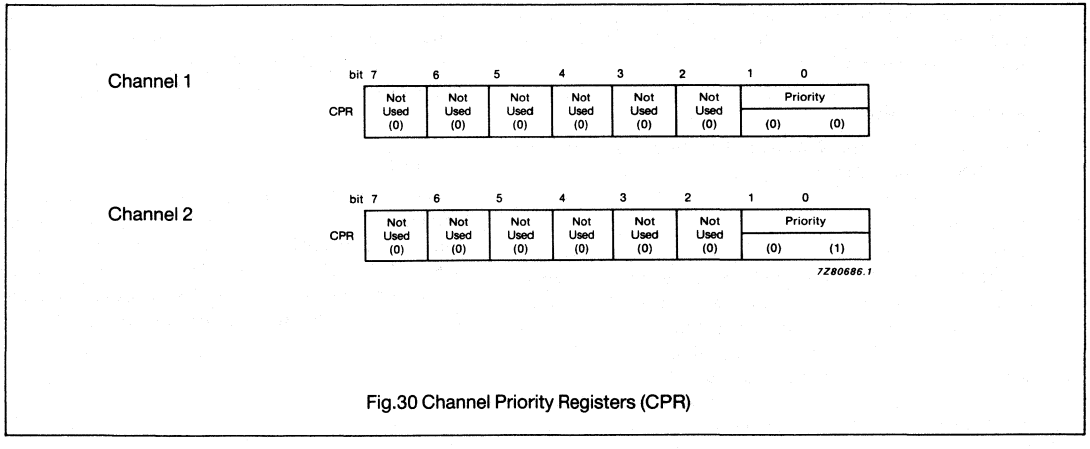


Fig.30 Channel Priority Registers (CPR)

Operation

The DMA controller operation has three principle phases:

- The initialization phase, during which the CPU configures the Channel Control Registers, loads the initial memory address and transfer count, and then starts the channel operation.
- The transfer phase, during which the channel accepts requests for transfers from the device, arbitrates for and acquires the bus, and provides the addressing and bus control for the transfers.
- The termination phase, which occurs after the operation has been completed when the channel reports the status of the operation.

Initialization phase

After programming the Channel Control Registers (CCR), the Memory and Device Address Counters and the Memory Transfer Counter, the CPU sets the START bit (CCR 7). The channel initializes the operation by clearing any pending requests, clearing the START bit and setting the Channel Active bit in the Channel Status Register. The channel is then ready to receive valid requests for an operation via the external REQ1N (or REQ2N) pin.

Transfer phase

Data movement between the device and memory takes place during the transfer phase in one of two ways. In single-address mode, transfers occur during a single bus cycle; in double-address mode, each transfer is performed with a read and write bus cycle.

Termination phase

The termination phase of the block transfer occurs under the conditions detailed below:

Count termination

During operand transfer, the channel decrements the Memory Transfer Counter (MTC). Completion of a channel transfer occurs when this counter reaches zero and the last byte or word has been moved from source to destination. The channel then notifies the device of completion by asserting the DONEN output during the last operand transfer cycle. On completion of the transfer, the Channel Active bit (CSR 11) in the Channel Status Register is cleared and the COC bit (CSR 15) is set.

Device termination

The channel monitors the state of the DONEN line while acknowledging a device transfer request. If the device asserts DONEN, the channel will terminate the operation after transferring the current operand. The channel then clears bit CSR 11, and sets bits CSR 15 and CSR 13 (all these bits reside in the Channel Status Register)

Software Abort

The Software Abort bit (CCR 4) allows the CPU to abort the current channel operation. (See description of Channel Control Register).

Bus error treatment

If both the BERRN and HALTN signals are asserted during a DMA controller cycle, the DMA controller will enter the RERUN state. If only the BERRN signal is asserted during a DMA controller cycle, the channel stops the controller operation, releases the bus, sets the ERR (CSR 12) and COC (CSR 15) bits and clears the Channel Active bit (CSR 11); all of these reside in the Channel Status Register. The channel also sets the error code in the Channel Error Register to indicate a bus error.

Reset

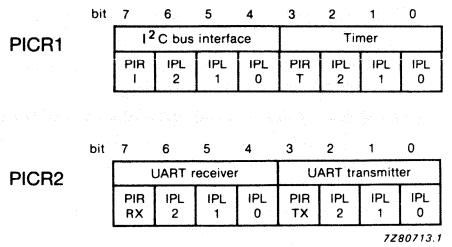
Via RESETN, external sources and CPU programs can reset and
initialize the DMA controller. If the DMA controller is the bus master when reset is detected, it releases the bus and resets all the bits of the Channel Status Register (except CSR 8) to zero.

Interrupts

If the Interrupt Enable bit (CCR 3) is set, the channel will send an interrupt when it terminates an operation (COC bit set - CSR 15). The priority level of the interrupt is given by the IPL bits in the Channel Control Register. During the interrupt acknowledge cycle, the channel requests an autovector and thus the IPL bits correspond directly to the vector used.

PERIPHERAL INTERRUPT CONTROL

The I²C and UART serial interfaces and the Timer, use a common set of Peripheral Interrupt Control Registers (PICR). These registers are memory mapped on the on-chip bus and communicate with the CPU of SCC68070.



I²C	I²C serial bus interface.
UART	UART serial interface.
Rx	UART receiver.
Tx	UART transmitter.
TIMER	Timer functions.
IPL	Interrupt priority level of interrupts requested by the IC, UART or Timer. IPL2 is the MSB and IPL0 the LSB. All values are positive true; IPL = 111 represents priority level 7 and IPL = 000 will inhibit the interrupts.
PIR	Pending Interrupt Reset, when set to '1' any pending interrupts of the respective peripheral will be reset. Note that this does not reset the interrupting status of a peripheral and further, if the IPL bits are changed without setting the PIR bit then spurious interrupts may occur. Reading the PIR bits will return a '0'.
note	Initially and after RESET, all PICR bits are cleared to zero.

Fig.31 Peripheral Interrupt Control Registers (PICR).

THE I²C SERIAL BUS INTERFACE

The SCC68070 has a serial I/O interface so that it can communicate with other devices via the I²C-bus. The I²C-bus can be used in master or slave mode, and can be connected to a maximum of 128 different peripheral ICs, each with a unique device address. Maximum transmission speed is 100 kbits/s. Communication with the bus is via two dedicated pins, SCL the serial clock pin and SDA the serial data pin. The interface can generate interrupts with priorities programmed to one of seven levels. A complete data transfer is shown in Fig.32.

Operating modes

The CPU can operate in the following modes with the serial I²C-bus.

- master transmitter (MTX)
- master receiver (MRX)
- slave transmitter (STX)
- slave receiver (SRX)

The I²C-bus I/O registers

The communication between the CPU and the I²C-bus interface is via a set of registers and an interrupt request facility. All I²C registers are accessible by read or write operations. The data and information controlling the operation of the interface is stored in the following registers (these are fully transparent and memory mapped to the CPU):

Table 21 Register memory map

Base address 8000 2000 (HEX)

A3	A2	A1	A0	I²C Register
0	0	0	0	reserved
0	0	0	1	Data Register (IDR)
0	0	1	0	reserved
0	0	1	1	Address Register (IAR)
0	1	0	0	reserved
0	1	0	1	Status Register (ISR)
0	1	1	0	reserved
0	1	1	1	Control Register (ICR)
1	0	0	0	reserved
1	0	0	1	Clock Control Register (ICCR)

Data Register (IDR)

The data register IDR performs the conversion between the serial and parallel data formats. Data to be transmitted is loaded into IDR by the CPU and then shifted out serially (MSB first), and data received on the serial bus is shifted into IDR (MSB first)

Address Register (IAR)

The address register holds the slave address allocated to the device in its 7 MSB's. It is only written to by the CPU and remains unchanged until rewritten. The LSB is the Always Selected bit (ALS) and when set to '1' will disable the address recognition and the interpretation of the R/W bit of the first byte. Thus, the I²C-bus interface will transfer in the Free Data Format and will respond to each data transfer.

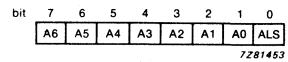


Fig.33 I²C Address Register (IAR).

Status Register (ISR)

The Status Register contains all the information concerning the status of the I²C-bus interface. All bits can be written to or read, by the CPU. The functions of the status bits, illustrated in Fig.34, follow:

MST = Master

If MST is '1', the I²C-bus interface is in the master mode and it generates clock pulses on SCL for transmission/reception timing of serial data.
If MST is '0', the I²C-bus is in the slave mode and clock pulses are received from the master on SCL.

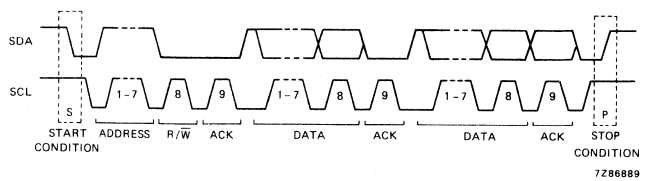


Fig.32 A complete data transfer on the I²C-bus.

TRX = Transmitter

If TRX is '1', the I²C-bus interface is in the transmitter mode and data in the IDR is shifted out onto the data line SDA, synchronized with the clock pulses on SCL.
If TRX is '0', the I²C-bus interface is in the receiver mode and data on the data line SDA is shifted into the IDR synchronized with the clock pulses on SCL.

BB = Busy

This bit indicates the state of the serial bus.

If BB is '0', the bus is free.
If BB is '1', the bus is busy.

PIN = Pending Interrupt Not

The PIN bit is set to '0' every time an I²C-bus interrupt is requested.
Any access to IDR will set the PIN bit to '1'.

AL = Arbitration Lost

The AL bit generally indicates the detection of an error. It is set to '1' when:

- a data error occurs in the transmitter mode
- the CPU tries to write to the ISR from the slave mode when it is not selected and the bus-busy flag is already set to '1'

The AL bit is reset to '0' by any access to IDR.

AAS = Addressed As Slave

AAS is set to '1' when the address comparator recognizes either its own slave address, the general call address (8 zeros) or the first byte in the free data format that has been received.
AAS is reset to zero by any access to IDR.

AD0 = Address Zero

AD0 is set to '1' if the address comparator detects the general call address (8 zeros). It is reset to '0' when either a START or STOP condition is detected.

LRB = Last Received Bit

When the interface is in the transmitter mode the LRB bit contains the receiver acknowledge bit. LRB is '0' when the reception of the transmission has been acknowledged.

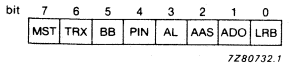


Fig.34 I²C Status Register (ISR).

Control Register (ICR)

Some additional functions of the interface are provided by the Control Register (ICR) as shown in Fig.35.

SEL = Selected

The SEL bit is a flag set (together with the AAS bit in the Status Register) by the interface logic when in the slave mode, and remains set during the whole transfer. It is reset when a STOP, START or repeated Start condition is detected.

ESO = Enable I²C-bus

When the ESO bit is set the I²C-bus is enabled and when reset the I²C-bus is disabled. Only the CPU can alter the ESO bit.

ACK = Acknowledge

This bit determines the polarity of the acknowledge that a receiver sends after correct reception of a byte.

If ACK = '1', reception will be acknowledged by a '0' bit.
If ACK = '0', reception will not be acknowledged, a '1' bit is sent.

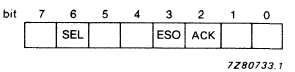
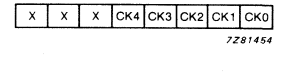


Fig.35 I²C Control Register.

Clock Control Register (ICCR)

By programming the 5 LSBs of the Clock Control Register, the frequency of SCL and SDA can be adapted to the needs of the I²C-bus or the SCC68070's system clock. After initialization or RESET, bits CK4 to CK0 are cleared to zero and must be programmed to a non-zero value before the I²C-bus is enabled.



X = undefined, reserved. Reading these bits will return a '1'.

Fig.36 I²C Clock Control Register (ICCR).

Table 22 I²C-bus interface divisors

CK4-CK0 (HEX)	divisor	≃ SCL freq. (kHz) (1)	≃ SCL freq. (kHz) (2)
0	illegal	–	-
1	78	126,025(3)	192,308(3)
2	90	109,222(3)	166,667(3)
3	102	96,372	147,059(3)
4	126	78,015	119,048(3)
5	150	65,533	100,000
6	174	56,494	86,207
7	198	49,464	75,758
8	246	39,959	60,976
9	294	33,435	51,020
A	342	28,742	43,860
B	390	25,205	38,462
C	486	20,266	30,864
D	582	16,890	25,773
E	678	14,498	22,124
F	774	12,700	19,380
10	996	10,175	15,060
11	1158	8,488	12,953
12	1350	7,281	11,111
13	1542	6,374	9,728
14	1926	5,103	7,788
15	2310	4,255	6,494
16	2694	3,648	5,568
17	3078	3,193	4,873
18	3846	2,555	3,900
19	4614	2,130	3,251
1A	5382	1,826	2,787
1B	6150	1,598	2,439
1C	7686	1,278	1,952
1D	9222	1,065	1,627
1E	10758	0,913	1,394
1F	12294	0,799	1,220

Notes to Table 22

1. The crystal or clock input frequency = 19.6608 MHz.
2. The crystal or clock input frequency = 30 MHz.
3. The maximum bus clock frequency in an I²C system is specified as 100 kHz.

DEVELOPMENT DATA

UART SERIAL INTERFACE

A UART (Universal Asynchronous Receiver/Transmitter) interface is included on-chip and functions like a subset of the UART's 2642, 2661 and 2691.

The UART interfaces directly with the CPU and can be used in either polled or interrupt driven modes. It accepts programmed instruct..ions from the CPU whilst supporting asynchronous serial data communication in either full or half-duplex mode. The interface then converts data received from the CPU into a serial form for transmission, and simultaneously it can receive serial data and convert it into parallel data as input to the CPU. Two bit rate generators can be programmed to generate transmit/receive bit rates by either using the SCC68070's system clock, or accepting an external clock via the XCKI input.

Table 23 UART register addressing

Base address 8000 2011 (HEX)

A3	A2	A1	A0*	register
0	0	0	1	Mode Register (UMR)
0	0	1	1	Status Register (UMR)
0	1	0	1	Clock Select Register(UCSR)
0	1	1	1	Command Register (UCR)
1	0	0	1	Transmit Holding Register (UTH)
1	0	1	1	Receive Holding Register (URH)
1	1	0	1	undefined, reserved
1	1	1	1	undefined, reserved

* All allocations with A0 = 0 are undefined, reserved.

Programming

Before initiating data communication, the UART operation mode must be programmed by writing to the mode, Clock Select and Command Registers. The UART interface can be re-configured at any time during program execution but when writing to the Mode and Clock Select Registers the transmitter and receiver should be disabled.

The Mode Register defines the general operational characteristics of the interface, while the Command Register controls the operation within the basic framework. Using the Clock Select Register, the bit rates for transmitter and receiver can be set and the result of the operation displayed in the Status Register. Certain bits of these registers are cleared when either a RESET input is applied, when a RESET instruction is performed by the CPU, or when special reset commands are programmed into the UART interface.

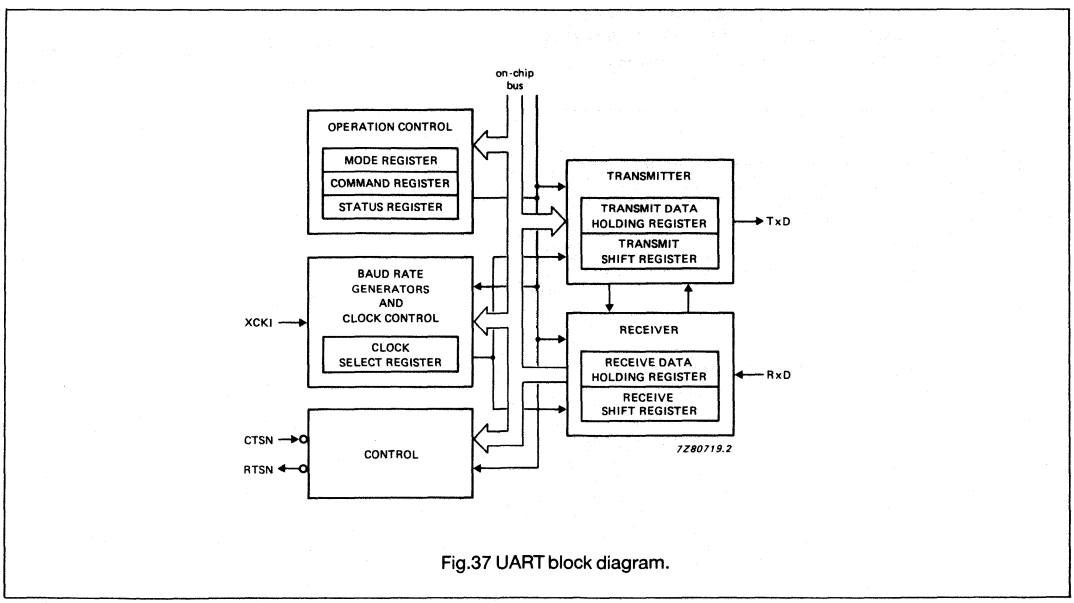


Fig.37 UART block diagram.

Mode Register (UMR)

UMR 0 selects the character length (7 or 8 bits). This does not include the parity bit (if programmed) or the START/STOP bits.

UMR 1 selects the number of STOP bits, either 1 or 2.

UMR 2 selects either odd or even parity when parity has been enabled by UMR 3.

UMR 3 controls the parity generation and when enabled a parity bit is added to the transmitted character and the receiver performs a parity check on the incoming data.

UMR 4 determines if the CTSN input controls the operation of the transmitter. If set to '0', CTSN has no influence on the transmitter. If set to '1', the transmitter monitors the state of CTSN every time it is ready to send a character and delays transmission until CTSN has been asserted

UMR 5 not used.

UMR 7:6 these bits determine the operation mode of the UART interface.

UMR 7:6 = 00 is the normal mode, with the transmitter and receiver operating independently.

UMR 7:6 = 01 places the channel in the auto echo mode which automatically retransmits the received data.

UMR 7:6 = 10 selects local loopback mode.

UMR 7:6 = 11 selects the remote loopback mode.

All bits of this register are cleared by a RESETN signal or a RESET instruction issued by the CPU, with the exception of bit 5 which is not used but returns a '1' when read.

bit 7	6	5	4	3	2	1	0
Channel mode		Not used	CTSN enable TxD	Parity control	Parity type	Stop bit length	Character length
00 = normal 01 = auto echo 10 = local loopback 11 = remote loopback		(1)	0 = no CSTN control 1 = CSTN control TxD	0 = inhibited 1 = enabled	0 = odd 1 = even	0 = one stop bit 1 = two stop bits	0 = seven bits 1 = eight bits

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Fig.38 UART Mode Register (UMR).

Clock Select Register (UCSR)

The UCSR allows selection of the clock source and baud rate for receiver and transmitter; as shown in Fig.39. The baud rates given are generated when either a 19.6608 MHz clock is used as the SCC68070's system clock (source = internal) or a 4.9152 MHz clock is applied to XCKI (source = external). Other frequencies will give a different set of baud rates. Note that when using the SCC68070's internal clock, it is pre-divided by 4.

UCSR 7 selects the clock source for the receiver and transmitter baud rates. After RESET, the clock source is the on-chip clock and with a 19.6608 MHz crystal, the listed baud rates are possible.
An external clock source (XCKI) is selected if UCSR 7 is '1'. The maximum frequency that can be applied to XCKI is 10 MHz.
All bits of this register are cleared by a RESETN signal or by a RESET instruction issued by the CPU, with the exception of Bit 3 which is not used but returns a '1' when read.

bit 7	6 5 4	3	2 1 0
Clock source	Receiver clock select	Not used	Transmitter clock select
	bit rate / divisor		bit rate / divisor
0 = internal (default after RESETN)	000 = 75 baud 65536 001 = 150 32768 010 = 300 16384 011 = 1200 4096 100 = 2400 2048 101 = 4800 1024 110 = 9600 512 111 = 19200 256	(1)	000 = 75 baud 65536 001 = 150 32768 010 = 300 16384 011 = 1200 4096 100 = 2400 2048 101 = 4800 1024 110 = 9600 512 111 = 19200 256
1 = external			

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Fig.39 UART Clock Select Register (UCSR).

Command Register (UCR)

The UCR is used to write commands to the UART.

UCR 6:4 = Miscellaneous commands.The encoded value of this field may be used to specify a single command as follows.

000 No command
001 No command
010 Reset receiver. Resets the receiver as if a hardware reset has been applied.
011 Reset transmitter. Resets the transmitter as if a hardware reset has been applied.
100 Reset error status. Clears the received break, parity error, framing error and overrun error bits in the Status Register USR 7:4.
101 No command.
110 Start break. Forces the TxD output LOW (spacing).
111 Stop break. The TxD line will go HIGH (marking) within two bit times. TxD will remain HIGH for one bit time before the next character, if any, is transmitted.

All bits of this register are cleared by a RESETN signal or by a RESET instruction issued by the CPU, with the exception of Bit 7 which is not used but returns a 1 when read.

DEVELOPMENT DATA

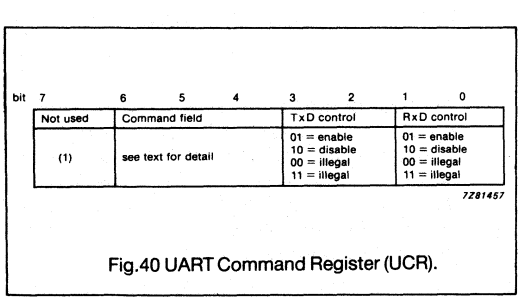
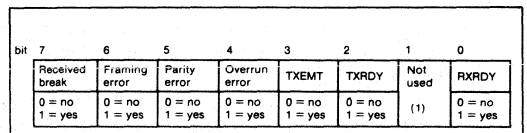


Fig.40 UART Command Register (UCR).

Status Register (USR).

The Status Register can be read by the CPU to determine the condition of an enabled receiver or transmitter.

All bits of this register are cleared by a RESETN or by a RESET instruction issued by the CPU, except bit 1 which is not used and returns a '1' when read.



TxEMT = Transmitter Empty
TxRDY = Transmitter Ready
RxRDY = Receiver Ready

Fig.41 UART Status Register (USR).

TIMER

The Timer comprises a 16-bit reference timer with an auto-reload register and two identical (independently function-programmable) 16-bit registers. The clock period of the reference timer and hence the maximum resolution is 96/CLKOUT(MHz) µs. Two programmable I/O lines provide the necessary connection to external circuitry. Three modes can be selected:

- match or pulse output mode which changes the output state when there is a match between the reference and register values
- count mode which counts external events that occur at the T1 (T2) input
- capture mode which stores the reference timer value in a capture register when an external event occurs at the T1 (T2) input

Any transition on the inputs to T1 or T2 can be programmed as an external event.

Timer programming

The CPU can read from or write to all the timer registers and they can also be accessed 'on the fly'. The address map of the timer registers is shown in Table 24.

Table 24 Timer registers address map.

Base address 8000 2020 (HEX)

A3	A2	A1	A0	register
0	0	0	0	Timer Status Register (TSR)
0	0	0	1	Timer Control Register (TCR)
0	0	1	0	Reload Register High (RRH)
0	0	1	1	Reload Register Low (RRL)
0	1	0	0	Timer 0 High (T0H)
0	1	0	1	Timer 0 Low (T0L)
0	1	1	0	Timer 1 High (T1H)
0	1	1	1	Timer 1 Low (T1L)
1	0	0	0	Timer 2 High (T2H)
1	0	0	1	Timer 2 Low (T2L)

Timer Control Register (TCR)

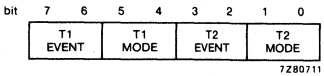


Fig. 42 Timer Control Register (TCR).

EVENT Control for external events monitored to trigger a function in Timer registers T1 or T2.

00 Input inhibited.

01 LOW-to-HIGH transitions will be monitored.

10 HIGH-to-LOW transitions will be monitored.

11 Any transition will be monitored.

MODE Control for the function of Timer registers T1 or T2.

00 Timer inhibited.

01 Match Mode. A match between the reference timer T0 with the respective Timer register will reset output T1 or T2. Each overflow of T0 will set output T1 or T2. The I/O port of the Timer is automatically switched to output mode.

10 Capture Mode. When an external event occurs (as described above), the contents of the reference timer T0 will be stored in the Timer register T1 or T2.

11 Event Counter Mode. When an external event occurs the timer register T1 or T2 will be incremented.

Timer Status Register (TSR)

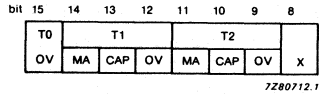


Fig.43 Timer Status Register (TSR).

The Timer Status Register indicates which timer and what specific event occurred that caused an interrupt (if enabled) and can be read by the CPU. After being read, each bit of this register should be reset by software as an acknowledge of the read because the status bits are automatically set but are not reset by the Timer. To reset each bit a '1' must be written to the appropriate bit position of the register.

OV Overflow. The Timer counts from FFFF(HEX) to 0000(HEX). This bit will be reset by timers T1 and T2 in event-counter mode only.

MA Match. A match between the value stored in Timer registers T1 or T2 and the value of the continuous timer T0 has occurred (in match mode).

CAP Capture. When an external event occurs the current value of the continuous timer T0 is stored in Timer T1 or T2 (in capture mode).

X Undefined, reserved.

Reference timer

The reference timer T0 will increment by 1 (starting from the value initially loaded into T0H and T0L). Using a crystal frequency of 19.6608 MHz the SCC68070 will increment every 9.766 µs (or 96 CKOUT cycles). When T0 reaches FFFF, the OV flag in the status register is set, and the reload register (RR) is loaded into T0. T0 will then start incrementing again until the next overflow occurs. A 30 MHz XTAL frequency will increment the timer every 6.4 µs, independently of the XCLI frequency.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Input voltage on any pin with respect to ground (V_{SS})	V_I	−0.3	+7.0	V
Input, output current	I_I, I_O	–	± 10	mA
Total power dissipation	P_{tot}	–	2	W
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range*	T_{amb}	0	+70	°C
	T_{amb}	−40	+85	°C

* Devices are available in two temperature ranges; see Ordering information.

Notes to Ratings and Electrical characteristics

1. Stresses above those listed in the Absolute Maximum System may cause permanent damage to the device. These are stress ratings only and do not mean that the device will operate at these or other conditions above those given in the operation section.
2. For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature.
3. This product contains circuitry specifically designed to protect its internal devices from excessive static charge. Nevertheless it is recommended that conventional precautions be taken to avoid applying any voltage above the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltages are measured with ground as reference (GRD). For testing, all input signals swing between 0.4 and 2.4 V with a transmission time of 5 ns maximum. All time measurements are made with input and output voltages of 0.8 and 2.0 V as appropriate.
6. On clock input XTAL1 when an external clock is used.
7. All timing measurements have CKOUT as a reference for both internal oscillator and external clock input modes. The device has been designed to be used with a 30 MHz crystal but the minimum crystal frequency specified is 8 MHz. All timing measurements except number 1 are specified at 19.6608, 25 and 30 MHz.
8. Actual value depends on clock period.
9. After V_{DD} has been applied for 100 ms.
10. If the asynchronous setup time (# 41A) requirements are met, the DTACKN LOW-to-data setup time (# 31) requirements can be ignored. The data must only satisfy the data-in to clock-LOW setup time (# 27) for the following cycle.
11. If the asynchronous setup time (# 41A) requirements are met, for both DTACKN and BERRN, then # 42 may be 0 ns.
12. All timing diagrams should only be referred to in regard to edge-to-edge measurements of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to the functional description and related diagrams for device operation.

DEVELOPMENT DATA

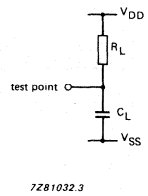
DC CHARACTERISTICS

V_{DD} = 5.0 V ±10%; V_{SS} = 0 V; T_{amb} = 0 to + 70 °C or − 40 to + 85 °C, dependent on type number. (See Figs.44 to 47 and notes 4 and 5)

parameter	test conditions	symbol	min.	max.	unit
Input voltage HIGH, all inputs					
except XTAL1, XTAL2, SDA, SCL		V_{IH}	2.0	V_{DD}	V
XTAL1	5.5 V_{DD}	V_{IH1}	0.8V_{DD}	V_{DD}	V
SDA, SCL	–	V_{IH2}	3.0*	V_{DD}	V
Input voltage LOW, all inputs					
except SDA, SCL	–	V_{IL}	V_{SS}-0.3	0.8	V
SDA, SCL	4.5 V_{DD}	V_{IL2}	V_{SS}-0.3	1.5	V
Input leakage current					
RTSN, CTSN, XCKI, DTACKN, INT1N, INT2N, REQ1N, REQ2N, RDYN, IN2N, IN4N, IN5N, NMIN, AVN, XTAL1	V_{DD} = 5.25 V V_{IN} = 5.25 V**	I_{LI}	–	20	µA
3-state (off-state) input current					
A1-A23, D0-D15, ASN, LDSN, R/WN, UDSN, T1, T2	V_i = 2.4/0.4 V	I_{TSI}	–	20	µA
Open-drain (off-state) input current					
BGACKN, RESETN, HALTN, BERRN, DTCN, DONEN, SCL, SDA	5.25 V_{DD}	I_{ODI}	–	20	µA
Output voltage HIGH					
A1-A23, DO-D15, ASN, BGN, LDSN, R/WN, UDSN, T1, T2, TXD, RTSN, ACKN1N, ACKN2N, IACKN2,4,5,7N	I_{OH} = 400 µA	V_{OH}	2.4	–	V
CKOUT	I_{OH} = 400 µA	V_{OH}	0.8V_{DD}	–	V
Output voltage LOW					
HALTN, BERRN, IACKN2,4,5,7, A1-A23, BGN, BGACKN, ACKN1N, ACKN2N, RESETN, T1, T2, RTSN, ASN, D0-D15, LDSN, R/WN, UDSN, DTCN, DONEN	I_{OL} = 3.2 mA	V_{OL}	–	0.5	V
CKOUT	I_{OL} = 3.2 mA	V_{OL}	–	0.45	V
SDA, SCL	I_{OL} = 3.0 mA	V_{OL}	–	0.45	V
Current consumption	CKOUT = 10 MHz	I_{DD}	–	95	mA
	CKOUT = 15 MHz	I_{DD}	–	142.5	mA
Input capacitance	V_i = 0V, T_{amb} = 25 °C frequency = 1 MHz	C_i		20	pF

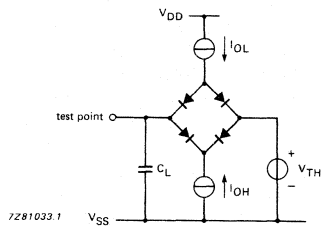
* Not tested, applied by external pullups.

** V_{IN} = enforced voltage.



test point	R_L (kΩ)	C_L (pF)
RESETN	1.2	130
HALTN	1.2	130
SDA	1.4	400
SCL	1.4	400
BGACKN	1.2	130
DONEN	1.2	130
BERRN	1.2	130
DTCN	1.2	130

Fig. 44 Open drain, bidirectional test loads.



C_L = 130 pF (including all parasitics) exept CKOUT for which C_L = 50 pF

V_{TH} = 1,6 V system load threshold voltage at which dynamic loads (I_{OL} and I_{OH}) switch; see d.c. characteristics

Fig. 45 Remaining test loads.

DEVELOPMENT DATA

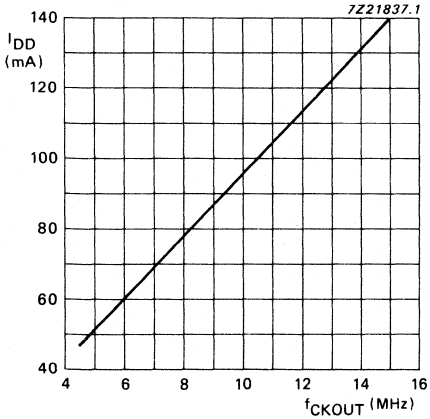
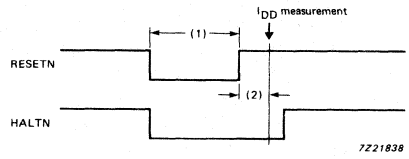


Fig. 46 I_{DD} (max.) verses frequency.



1. ≥400 t_{CYC}.
2. ≥10 ms.

Fig.47 I_{DD} measurement.

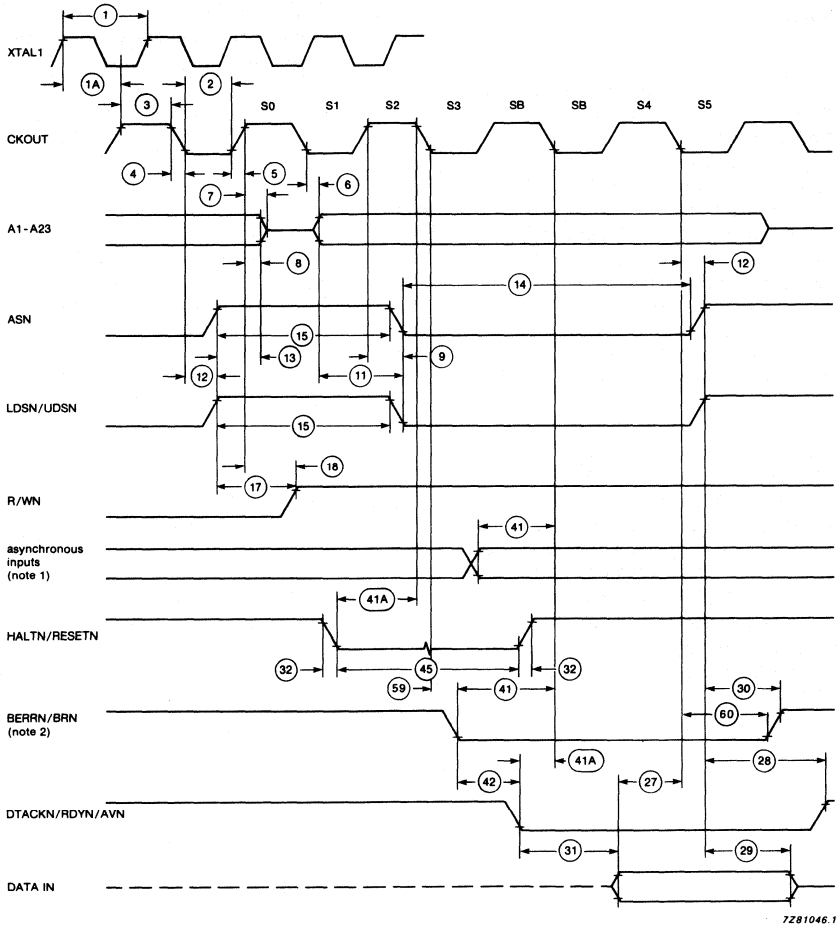
AC CHARACTERISTICS

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_{amb} = 0 to + 70 °C or − 40 to + 85 °C (dependent on type number), C_{load} on CKOUT = 50 pF (see Figures 48 to 51).

No.	parameter	symbol	f_{XTAL1} = 19.6 MHz		f_{XTAL1} = 25 MHz		f_{XTAL1} = 30 MHz		
			min.	max.	min.	max.	min.	max.	unit
1	Crystal or input clock period	t_{CYC}	50	125	40	125	33	125	ns
1A	XTAL HIGH to CKOUT HIGH or LOW	t_{XHCV}	8	96	5	45	5	40	ns
2	CKOUT, LOW level	t_{COL}	33	–	25	–	20	–	ns
3	CKOUT, HIGH level	t_{COH}	33	–	25	–	20	–	ns
4	CKOUT fall-time	t_{COf}	–	10	–	10	–	10	ns
5	CKOUT rise-time	t_{COr}	–	12	–	10	–	10	ns
6	CKOUT LOW to address valid	t_{CLAV}	–	55	–	50	–	50	ns
7	CKOUT HIGH to address/data, high-impedance (max.)	t_{CHAZx}	–	55	–	55	–	55	ns
8	CKOUT HIGH to address invalid (min.)	t_{CHAZn}	0	–	0	–	0	–	ns
9	CKOUT HIGH to ASN, DSN LOW	t_{CHSL}	0	45	0	45	0	45	ns
11[8]	Address to ASN/DSN (read), ASN (write) LOW	t_{AVSL}	20	–	10	–	10	–	ns
12	CKOUT LOW to ASN, DSN HIGH	t_{SLSH}	0	55	0	45	0	45	ns
13[8]	ASN, DSN HIGH to address invalid	t_{SHAZ}	20	–	10	–	10	–	ns
14[8]	ASN/DSN (read), ASN (write) LOW level	t_{SL}	200	–	160	–	130	–	ns
14A[8]	DSN LOW level (write)	t_{DSL}	100	–	80	–	65	–	ns
15	ASN, DSN HIGH level	t_{SH}	100	–	80	–	70	–	ns
16	CKOUT HIGH to ASN, DSN high impedance	t_{CHSZ}	–	55	–	55	–	50	ns
17[8]	ASN, DSN HIGH to R/WN HIGH (read)	t_{SHRH}	20	–	10	–	10	–	ns
18	CKOUT HIGH to R/WN HIGH	t_{CHRH}	0	55	0	45	0	45	ns
20	CKOUT HIGH to R/WN LOW (write)	t_{CHRL}	–	55	–	45	–	45	ns
21[8]	Address valid to R/WN LOW (write)	t_{AVRL}	0	–	0	–	0	–	ns
22[8]	R/WN LOW to DSN LOW (write)	t_{CLSL}	55	–	30	–	25	–	ns
23	CKOUT LOW to data out valid (write)	t_{CLDO}	–	50	–	45	–	45	ns
25[8]	ASN, DSN HIGH to data out invalid (write)	t_{SHDO}	20	–	15	–	15	–	ns
26[8]	Data out valid to DSN LOW (write)	t_{DOSL}	20	–	15	–	15	–	ns
27[10]	Data in to clock LOW (set-up time, read)	t_{DICL}	10	–	10	–	5	–	ns
28[8]	ASN, DSN HIGH to DTACKN, RDYN, AVN HIGH	t_{SHDAH}	0	190	0	150	0	120	ns
29	ASN, DSN HIGH to data invalid (hold time, read)	t_{SHDI}	0	–	0	–	0	–	ns
30	ASN, DSN HIGH to BERRN HIGH	t_{SHBEH}	0	–	0	–	0	–	ns
31[8/10]	DTACKN LOW to data in (set-up time, read)	t_{DCLDI}	–	65	–	50	–	45	ns
32[9]	HALTN and RESETN input transition time	t_{RHrf}	0	200	0	200	0	200	ns
33	CKOUT HIGH to BGN LOW	t_{CHGL}	–	55	–	50	–	50	ns
34	CKOUT HIGH to BGN HIGH	t_{CHGH}	–	55	–	50	–	50	ns
35	BRN LOW to BGN LOW	t_{BRLGL}	1.5	3.5 + 80	1.5	3.5 + 70	1.5	3.5 + 70	cp ns
36	BRN HIGH to BGN HIGH	t_{BRHGH}	1.5	2.5 + 80	1.5	2.5 + 70	1.5	2.5 + 70	cp ns
37	BGACKN LOW to BGN HIGH	t_{GALGH}	1.5	2.5 + 80	1.5	2.5 + 70	1.5	2.5 + 70	cp ns

No.	parameter	symbol	f_{XTAL1} = 19.6 MHz		f_{XTAL1} = 25 MHz		f_{XTAL1} = 30 MHz		unit
			min.	max.	min.	max.	min.	max.	
38	BGN LOW to bus high impedance (ASN HIGH)	t_{GLZ}	–	55	–	50	–	50	ns
39	BGN HIGH level	t_{GH}	1.5	–	1.5	–	1.5	–	cp
40	BGACKN width	t_{BGL}	1.5	–	1.5	–	1.5	–	cp
41	Asynchronous set-up time	t_{ASI}	25	–	25	–	25	–	ns
41A[10]	Asynchronous set-up time for DTACKN, AVN, BERRN, HALTN, RDYN	t_{ASDT}	25	–	10	–	10	–	ns
42[11]	BERRN (input) LOW to DTACKN LOW	t_{BELDAL}	20	–	15	–	15	–	ns
43	CKOUT HIGH to Data OUT invalid (write)	t_{CHDO}	0	–	0	–	0	–	ns
44	R/WN LOW to data bus driven	t_{RLDL}	20	–	10	–	10	–	ns
45	HALTN/RESETN pulse width	t_{HRPW}	10	–	10	–	10	–	cp
46	REQx set-up before CKOUT LOW		25	–	10	–	10	–	ns
47	ACKxN LOW from CKOUT HIGH		0	50	0	50	0	50	ns
48	REQxN hold after CKOUT LOW		10	–	10	–	10	–	ns
49	DTCN LOW from CKOUT HIGH		–	50	–	50	–	50	ns
50	ASN, LDSN, UDSN HIGH from DTCN LOW		0	–	0	–	10	–	ns
51	ACKxN HIGH from CKOUT HIGH		–	55	–	50	–	50	ns
52	DTCN non-active to CKOUT HIGH		–	45	–	40	–	40	ns
53	DONEN (output) LOW from CKOUT HIGH		–	45	–	40	–	40	ns
54	DONEN (output) non-active from CKOUT HIGH		–	55	–	55	–	55	ns
56	DONEN (input) set-up LOW before CKOUT LOW		25	–	10	–	10	–	ns
57	DONEN (input) hold LOW after CKOUT HIGH		10	–	10	–	10	–	ns
58	REQ LOW to BGACKN (output) LOW		3.5	–	3.5	–	3.5	–	cp
59	CKOUT LOW to BERRN (output) LOW		–	50	–	40	–	40	ns
60	CKOUT LOW to BERRN (output) non-active		–	45	–	45	–	45	ns
61	CKOUT HIGH to BGACKN (output) LOW		–	60	–	60	–	60	ns

DEVELOPMENT DATA



Notes to Fig.48

1. Setup time for the asynchronous inputs and AVN guarantees their recognition at the next falling edge of the clock.

2. BRN need fall at this time only to ensure being recognized at the end of this bus cycle. When BERRN is driven during a faulty MMU cycle, an additional error cycle (SE) is inserted in between SB and S4.

Fig.48 Read cycle timing.

DEVELOPMENT DATA

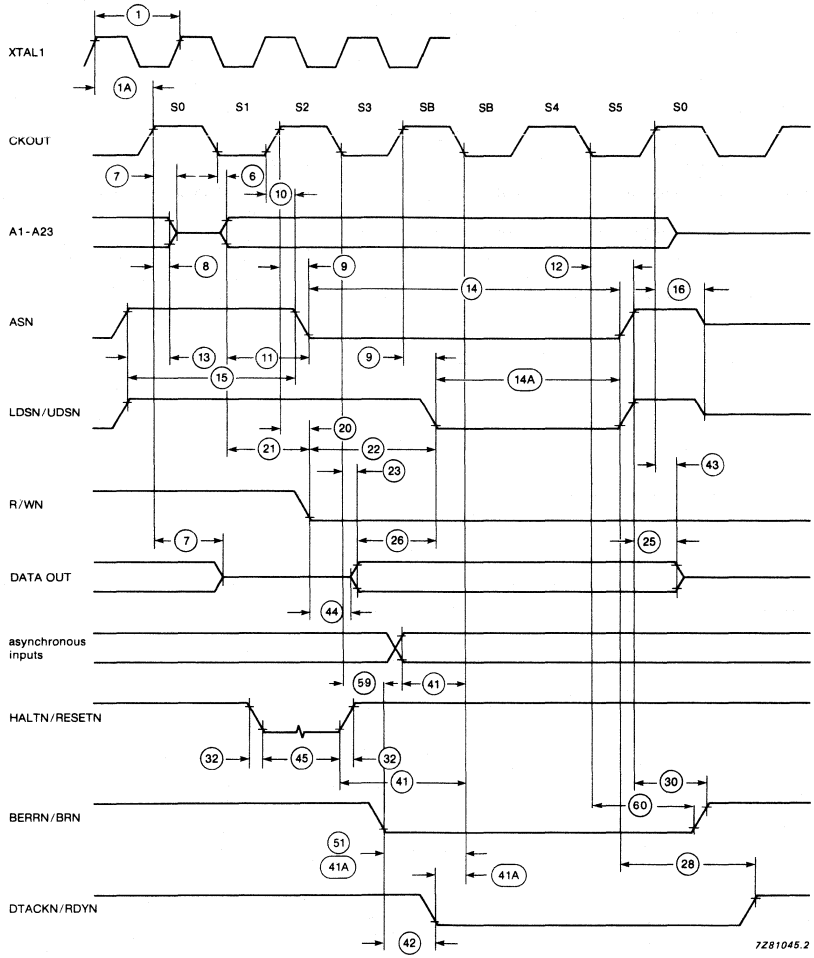


Fig.49 Write cycle timing.

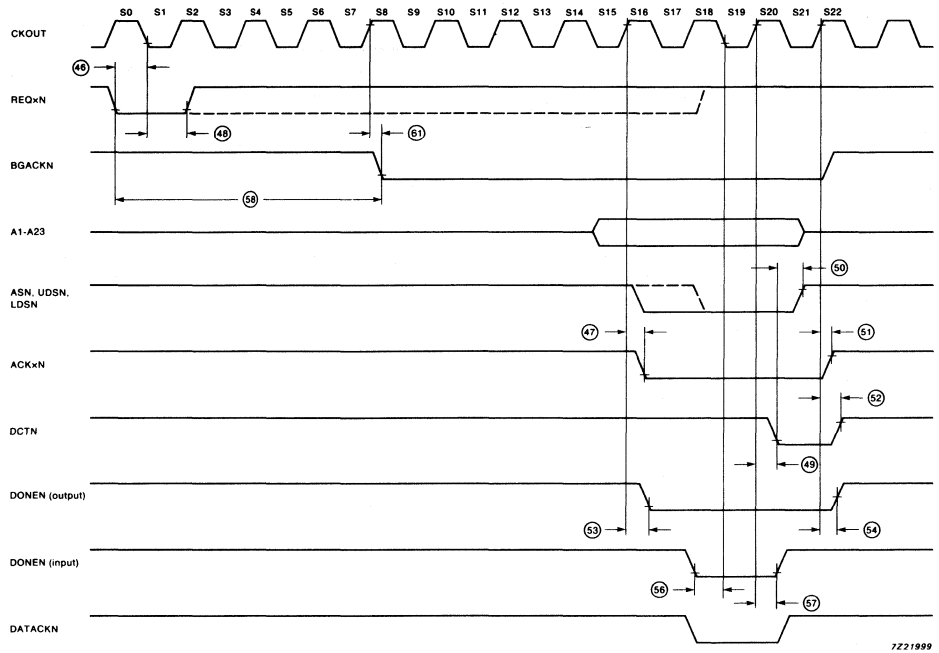
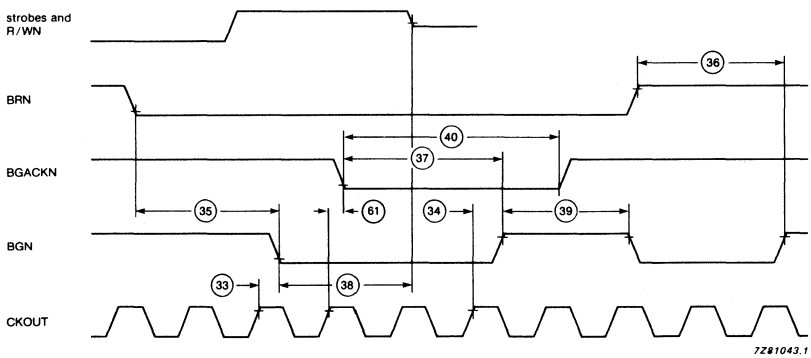


Fig.50 DMA timing.



Note to Fig.51

1. Setup for the asynchronous inputs BERRN, BRN, BGACKN, DTACKN, IN2N, IN4N, IN5N, NMIN, INT1N, INT2N, AVN, REQ1N, REQ2N, DONEN, RDYN and DATA guarantees their recognition.

Fig.51 AC electrical timing - bus arbitration.

DEVELOPMENT DATA

POWER CONSIDERATIONS

The average chip-junction temperature T_j, in °C can be obtained from:

$$T_j = T_{amb} + (P_d \times R_{th\ ja}) \quad (1)$$

where :

T_{amb} = ambient temperature (°C)
$R_{th\ ja}$ = package thermal resistance, junction-to-ambient, (K/W)
P_d = $P_{INT} + P_{I/O}$ (2)
P_{INT} = $I_{DD} \times V_{DD}$ = chip internal power (W)
$P_{I/O}$ = power dissipation on input and output pins (determined by the user)

For most applications $P_{I/O} < P_{INT}$. The approximate relationship between P_d and T_j (if $P_{I/O}$ is neglected) is:

$$P_d = K/(T_j + 273)$$

Solving equations (1) and (2) for K gives:

$$K = P_O(T_{amb} + 273) + R_{th\ ja}P_d^2 \quad (3)$$

Where K is a constant pertaining to a particular part. K can be determined from equation (3) by measuring P_d (at equilibrium) for a known T_{amb}. Using this value of K, the values of P_d and T_j can be obtained by solving equations (1) and (2) for any value of T_{amb}.

CLOCK TIMING (see figs.52 and 53)

Table 25 Clock timing

parameter	symbol	min.	max.	unit
Crystal or input frequency	f	8	30	MHz
Cycle time	t_{cyc}	33	125	ns
Clock pulse width	t_{CL}	10	–	ns
	t_{CH}	10	–	ns
Rise and fall times	t_{Cr}	–	10	ns
	t_{Cf}	–	10	ns
XTAL1 HIGH to XTAL2 LOW	t_{C12}	–	10	ns
XTAL1 LOW to XTAL2 HIGH	t_{C21}	–	10	ns

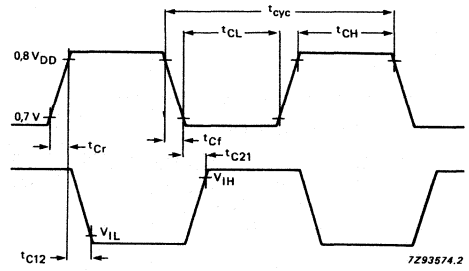
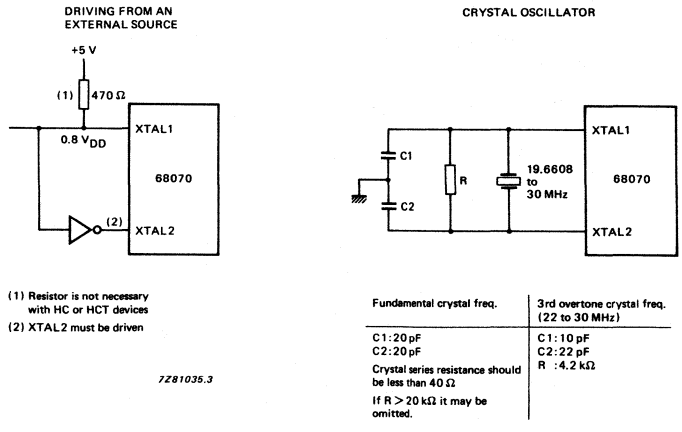


Fig.52 Input clock timing when external clock used.



(1) Resistor is not necessary with HC or HCT devices
(2) XTAL2 must be driven

Fundamental crystal freq.	3rd overtone crystal freq. (22 to 30 MHz)
C1: 20 pF C2: 20 pF Crystal series resistance should be less than 40 Ω If R > 20 kΩ it may be omitted.	C1: 10 pF C2: 22 pF R : 4.2 kΩ

Fig.53 Clock circuitry.

I²C INTERFACE TIMING

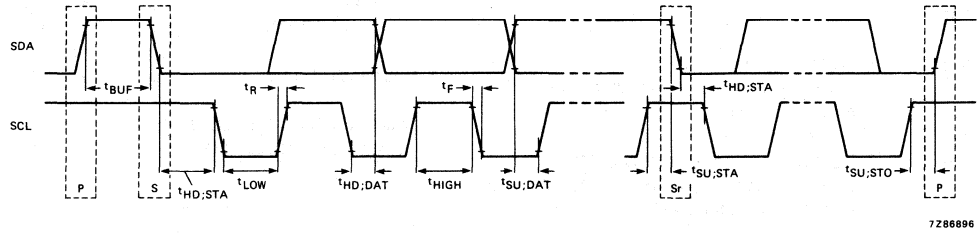


Fig.54 I²C Interface Timing.

Table 26 I²C interface timing

parameter	symbol	min.	max.	units
SCL clock frequency	f_{SCL}	0	192	kHz
Time the bus must be free before new transmission can start	t_{BUF}	4.7	–	µs
Hold time START condition. After this period the first clock pulse is generated	$t_{HD;STA}$	4.0	–	µs
LOW period of clock	t_{LOW}	4.7	–	µs
HIGH period of clock	t_{HIGH}	4.0	–	µs
Set-up time for START condition (only relevant for a repeated start condition)	$t_{SU;STA}$	4.7	–	µs
Hold time DATA for I²C devices	$t_{HD;DAT}$	0	–	µs
Set-up time DATA	$t_{SU;DAT}$	250	–	ns
Rise time of both SDA and SCL lines	t_R	–	1	µs
Fall time of both SDA and SCL lines	t_F	–	300	ns
Set-up time for stop condition	$t_{SO;STO}$	4.7	–	µs

Notes to Table 26

1. All values are referenced to V_{IH} and V_{IL} levels.
2. Timings given above are for SCL = 100 kHz (maximum I²C system frequency).

UART INTERFACE TIMING

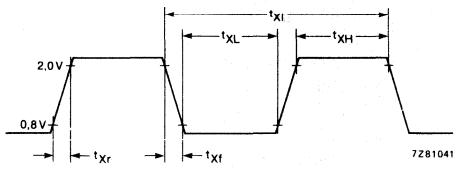


Fig.55 XCKI input timing.

Table 27 UART interface timing

parameter	symbol	10 MHz		12.5 MHz		15 MHz		unit
		min.	max.	min.	max.	min.	max.	
XCKI frequency of operation	f_{XCKI}	2	5	2	10	2	10	MHz
XCKI cycle time	t_{XI}	200	500	100	500	100	500	ns
XCKI pulse width	t_{XH}	60	250	30	250	30	250	ns
	t_{XL}	60	250	30	250	30	250	ns
XCKI rise and fall times	t_{Xr}	–	10	–	10	–	10	ns
	t_{Xf}	–	10	–	10	–	10	ns

TIMER SPECIFICATION

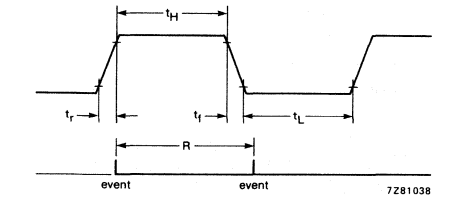


Fig.56 Input timing to T1 or T2.

T1 and T2 input signals must be held HIGH or LOW longer than t_H or t_L to be latched at the input to the Timer. Events must be separated by more than the resolution R of the Timer.

Table 28 Input timing T1 or T2

parameter	symbol	10 MHz		12.5 MHz		15 MHz		unit
		min.	max.	min.	max.	min.	max.	
T1 or T2 pulse width	t_H	700	–	560	–	466	–	ns
	t_L	700	–	560	–	466	–	ns
T1 or T2 rise and fall times	t_r	–	–	–	–	–	50	ns
	tf	–	–	–	–	–	50	ns
Resolution (the time between two events to be taken into account)	R	9.6	–	7.68	–	6.4	–	µs

SUMMARY OF ON-CHIP ADDRESSES

HEX address	symbol	register
8000 0000 to 8000 1000	–	reserved
8000 1001	LIR	Latched Interrupt Priority Register
8000 1002 to 8000 2000	–	reserved
8000 2001	IDR	I^2C Data Register
8000 2002	–	reserved
8000 2003	IAR	I^2C Address Register
8000 2004	–	reversed
8000 2005	ISR	I^2C Status Register
8000 2006	–	reversed
8000 2007	ICR	I^2C Control Register
8000 2008	–	reversed
8000 2009	ICC	I^2C Clock Control Register
8000 200A to 8000 2010	–	reserved
8000 2011	UMR	UART Mode Register
8000 2012	–	reserved
8000 2013	USR	UART Status Register
8000 2014	–	reserved
8000 2015	UCS	UART Clock Select Register
8000 2016	–	reserved
8000 2017	UCR	UART Command Register
8000 2018	–	reserved
8000 2019	UTH	UART Transmit Holding Register
8000 201A	–	reserved
8000 201B	URH	UART Receive Holding Register
8000 201C to 8000 201F	–	reserved
8000 2020	TSR	Timer Status Register
8000 2021	TCR	Timer Control Register
8000 2022	RRH	Reload Register High
8000 2023	RRL	Reload Register Low
8000 2024	T0H	Timer 0 High
8000 2025	TOL	Timer 0 Low
8000 2026	T1H	Timer 1 High
8000 2027	T1L	Timer 1 Low
8000 2028	T2H	Timer 2 High
8000 2029	T2L	Timer 2 Low
8000 202A to 8000 2044	–	reserved
8000 2045	PICR1	Peripheral Interrupt Control Register 1
8000 2046	–	reserved
8000 2047	PICR2	Peripheral Interrupt Control Register 2
8000 2048 to 8000 3FFF	–	reserved
8000 4000	CSR	Channel Status Register Channel 1
8000 4001	CER	Channel Error Register Channel 1
8000 4002 to 8000 4003	–	reserved

HEX address	symbol	register
8000 4004	DCR	Device Control Register Channel 1
8000 4005	OCR	Operation Control Register Channel 1
8000 4006	SCR	Sequence Control Register Channel 1
8000 4007	CCR	Channel Control Register Channel 1
8000 4008 to 8000 4009	–	reserved
8000 400A	MTCH	Memory Transfer Counter High Channel 1
8000 400B	MTCL	Memory Transfer Counter Low Channel 1
8000 400C	MACH	Memory Address Counter High Channel 1
8000 400D	MACMH	Memory Address Counter Middle High Channel 1
8000 400E	MACML	Memory Address Counter Middle Low Channel 1
8000 400F	MACL	Memory Address Counter Low Channel 1
8000 4010 to 8000 402C	–	reserved
8000 402D	CPR	Channel Priority Register Channel 1
8000 402E to 8000 403F	–	reserved
8000 4040	CSR	Channel Status Register Channel 2
8000 4041	CER	Channel Error Register Channel 2
8000 4042 to 8000 4043	–	reserved
8000 4044	DCR	Device Control Register Channel 2
8000 4045	OCR	Operation Control Register Channel 2
8000 4046	SCR	Sequence Control Register Channel 2
8000 4047	CCR	Channel Control Register Channel 2
8000 4048 to 8000 4049	–	reserved
8000 404A	MTCH	Memory Transfer Counter High Channel 2
8000 404B	MTCL	Memory Transfer Counter Low Channel 2
8000 404C	MACH	Memory Address Counter High Channel 2
8000 404D	MACMH	Memory Address Counter Middle High Channel 2
8000 404E	MACML	Memory Address Counter Middle Low Channel 2
8000 404F	MACL	Memory Address Counter Low Channel 2
8000 4050 to 8000 4053	–	reserved
8000 4054	DACH	Device Address Counter High Channel 2
8000 4055	DACHMH	Device Address Counter Middle High Channel 2
8000 4056	DACML	Device Address Counter Middle Low Channel 2
8000 4057	DACL	Device Address Counter Low Channel 2
8000 4058 to 8000 406C	-	reserved
8000 406D	CPR	Channel Priority Register Channel 2
8000 406E to 8000 7FFF	–	reserved
8000 8000	MSR	MMU Status Register
8000 8001	MCR	MMU Control Register
8000 8002 to 8000 803F	–	reserved
8000 8040	SAH	Segment Attributes High, Descriptor 0
8000 8041	SAL	Segment Attributes Low, Descriptor 0
8000 8042	SLH	Segment Length High, Descriptor 0
8000 8043	SLL	Segment Length Low, Descriptor 0
8000 8044	–	reserved
8000 8045	SNR	Segment Number, Descriptor 0
8000 8046	SBH	Segment Base Address High, Descriptor 0
8000 8047	SBL	Segment Base Address Low, Descriptor 0

SUMMARY OF ON-CHIP ADDRESSES (continued)

HEX address	symbol	register
8000 8048	SAH	Segment Attributes High, Descriptor 1
8000 8049	SAL	Segment Attributes Low, Descriptor 1
8000 804A	SLH	Segment Length High, Descriptor 1
8000 804B	SLL	Segment Length Low, Descriptor 1
8000 804C	–	reserved
8000 804D	SNR	Segment Number, Descriptor 1
8000 804E	SBH	Segment Base Address High, Descriptor 1
8000 804F	SBL	Segment Base Address Low, Descriptor 1
8000 8050	SAH	Segment Attributes High, Descriptor 2
8000 8051	SAL	Segment Attributes Low, Descriptor 2
8000 8052	SLH	Segment Length High, Descriptor 2
8000 8053	SLL	Segment Length Low, Descriptor 2
8000 8054	–	reserved
8000 8055	SNR	Segment Number, Descriptor 2
8000 8056	SBH	Segment Base Address High, Descriptor 2
8000 8057	SBL	Segment Base Address Low, Descriptor 2
8000 8058	SAH	Segment Attributes High, Descriptor 3
8000 8059	SAL	Segment Attributes Low, Descriptor 3
8000 805A	SLH	Segment Length High, Descriptor 3
8000 805B	SLL	Segment Length Low, Descriptor 3
8000 805C	–	reserved
8000 805D	SNR	Segment Number, Descriptor 3
8000 805E	SBH	Segment Base Address High, Descriptor 3
8000 805F	SBL	Segment Base Address Low, Descriptor 3
8000 8060	SAH	Segment Attributes High, Descriptor 4
8000 8061	SAL	Segment Attributes Low, Descriptor 4
8000 8062	SLH	Segment Length High, Descriptor 4
8000 8063	SLL	Segment Length Low, Descriptor 4
8000 8064	–	reserved
8000 8065	SNR	Segment Number, Descriptor 4
8000 8066	SBH	Segment Base Address High, Descriptor 4
8000 8067	SBL	Segment Base Address Low, Descriptor 4
8000 8068	SAH	Segment Attributes High, Descriptor 5
8000 8069	SAL	Segment Attributes Low, Descriptor 5
8000 806A	SLH	Segment Length High, Descriptor 5
8000 806B	SLL	Segment Length Low, Descriptor 5
8000 806C	–	reserved
8000 806D	SNR	Segment Number, Descriptor 5
8000 806E	SBH	Segment Base Address High, Descriptor 5
8000 806F	SBL	Segment Base Address Low, Descriptor 5
8000 8070	SAH	Segment Attributes High, Descriptor 6
8000 8071	SAL	Segment Attributes Low, Descriptor 6
8000 8072	SLH	Segment Length High, Descriptor 6
8000 8073	SLL	Segment Length Low, Descriptor 6
8000 8074	–	reserved
8000 8075	SNR	Segment Number, Descriptor 6
8000 8076	SBH	Segment Base Address High, Descriptor 6
8000 8077	SBL	Segment Base Address Low, Descriptor 6

HEX address	symbol	register
8000 8078	SAH	Segment Attributes High, Descriptor 7
8000 8079	SAL	Segment Attributes Low, Descriptor 7
8000 807A	SLH	Segment Length High, Descriptor 7
8000 807B	SLL	Segment Length Low, Descriptor 7
8000 807C	–	reserved
8000 807D	SNR	Segment Number, Descriptor 7
8000 807E	SBH	Segment Base Address High, Descriptor 7
8000 807F	SBL	Segment Base Address Low, Descriptor 7
8000 8080 to BFFF FFFF	–	reserved

DEVELOPMENT DATA

SYNCHRONIZATION PROCESSOR FOR TELEVISION RECEIVERS

GENERAL DESCRIPTION

The TDA8370 is a sync processor designed to generate and synchronize horizontal and vertical signals in medium and high performance television receivers. The device is particularly suitable for application with teletext decoders and video tape recorders.

A video switch controlled by I²C bus command or analogue switched voltage selects internal or external composite video signals.
The processing of not line-locked vertical sync in non-standard mode is also possible.

Features

- Two separate video inputs adapted to:
  I.F. detector (front-end output)
  or
  peri-television connector selected by the video switch
- Buffered video output
- Horizontal sync separator with self-aligning levels
- Vertical sync separator 1 with self-aligning levels when standard mode selected
- Vertical sync separator 2 with self-aligning levels when non-standard mode selected (e.g. video tape recorder signal)
- Noise invertor
- Gated phase discriminator with switchable time constant for non-standard applications
- 6 MHz VCO for generation of clock signal for teletext display
- Noise level detector
- Automatic low-current starting circuit
- φ 2 phase control with shift adjustment not affecting gain or time constant
- Horizontal output optimized for operation with self-oscillating power supply
- Vertical divider system with automatic selection of 625 or 525 standard
- 50/60 Hz identification output voltage
- Mute output
- Coincidence detector
- Vertical shaping and feedback system with automatic 60 Hz amplitude correction
- 3-level sandcastle output
- Vertical guard circuit active via sandcastle output
- Scan composite sync ($\overline{\text{S.C.S.}}$) output as slave input for teletext decoder
- Special "sense" ground pin to ensure correct feedback voltage in the frame deflection circuit
- I²C bus controlled teletext non-interlaced signal (N.I.L.)
- Line and frame frequencies switched to nominal when noise only is received in standard mode

PACKAGE OUTLINES

28-lead DIL; plastic (SOT-117).

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 22)	V_P	10	12	13,2	V
Supply current (pin 22)	I_P	–	125	150	mA
Starting current (pin 23)	I_{23}	5	5,5	10	mA
Video input voltage (positive video)					
pin 1 (peak-to-peak value)	$V_{1\text{-}20(p\text{-}p)}$	–	2,25	3	V
pin 5 (peak-to-peak value)	$V_{5\text{-}20(p\text{-}p)}$	–	1	1,4	V
Horizontal flyback input current (pin 18)	I_{18}	0,3	1	4	mA
Vertical comparator input (pin 14)					
a.c. input voltage (peak-to-peak value)	$V_{14\text{-}20(p\text{-}p)}$	–	3	–	V
d.c. input voltage	$V_{14\text{-}20}$	–	2,5	–	V
I^2C clock input/analogue input (pin 7)					
analogue video switching voltage level	$V_{7\text{-}20}$	6,5	–	7,5	V
I^2C data input/analogue input (pin 8) for selecting peri-television connector input					
analogue switching voltage level for selecting non-standard mode (equal to V.T.R.)	$V_{8\text{-}20}$	6,5	–	7,5	V
Max. horizontal output voltage (pin 17)	$V_{17\text{-}20}$	14	–	16	V
Max. vertical drive output voltage (pin 13)	$V_{13\text{-}20}$	–	–	10	V
Sandcastle 3-level output voltage (pin 9)					
burstkey	$V_{9\text{-}20}$	–	10,8	–	V
horizontal blanking	$V_{9\text{-}20}$	4,1	4,4	4,9	V
vertical blanking	$V_{9\text{-}20}$	2,1	2,6	2,9	V
Scan composite sync output (pin 10)					
high output voltage at $-I_{10} = 5$ mA	$V_{10\text{-}20}$	4,3	4,8	5,3	V
output current	$-I_{10}$	–	1	–	mA
Video output (pin 3)					
a.c. output voltage (peak-to-peak value)	$V_{3\text{-}20(p\text{-}p)}$	2,6	3	3,4	V
d.c. level top sync	$V_{3\text{-}20}$	2,8	3,2	3,7	V
50/60 Hz identification output voltage (pin 4)					
50 Hz at $I_4 = 0,1$ mA	$V_{4\text{-}20}$	–	1,3	1,7	V
60 Hz at $-I_4 = 5$ mA	$V_{4\text{-}20}$	8	10	–	V
output current	$-I_4$	–	–	5	mA
Mute output voltage (pin 28)					
in-sync at $I_{28} = 0,1$ mA	$V_{28\text{-}20}$	–	1,2	1,5	V
out-of-sync/no sync at $-I_{28} = 0,5$ mA	$V_{28\text{-}20}$	–	10,5	–	V

DEVELOPMENT DATA

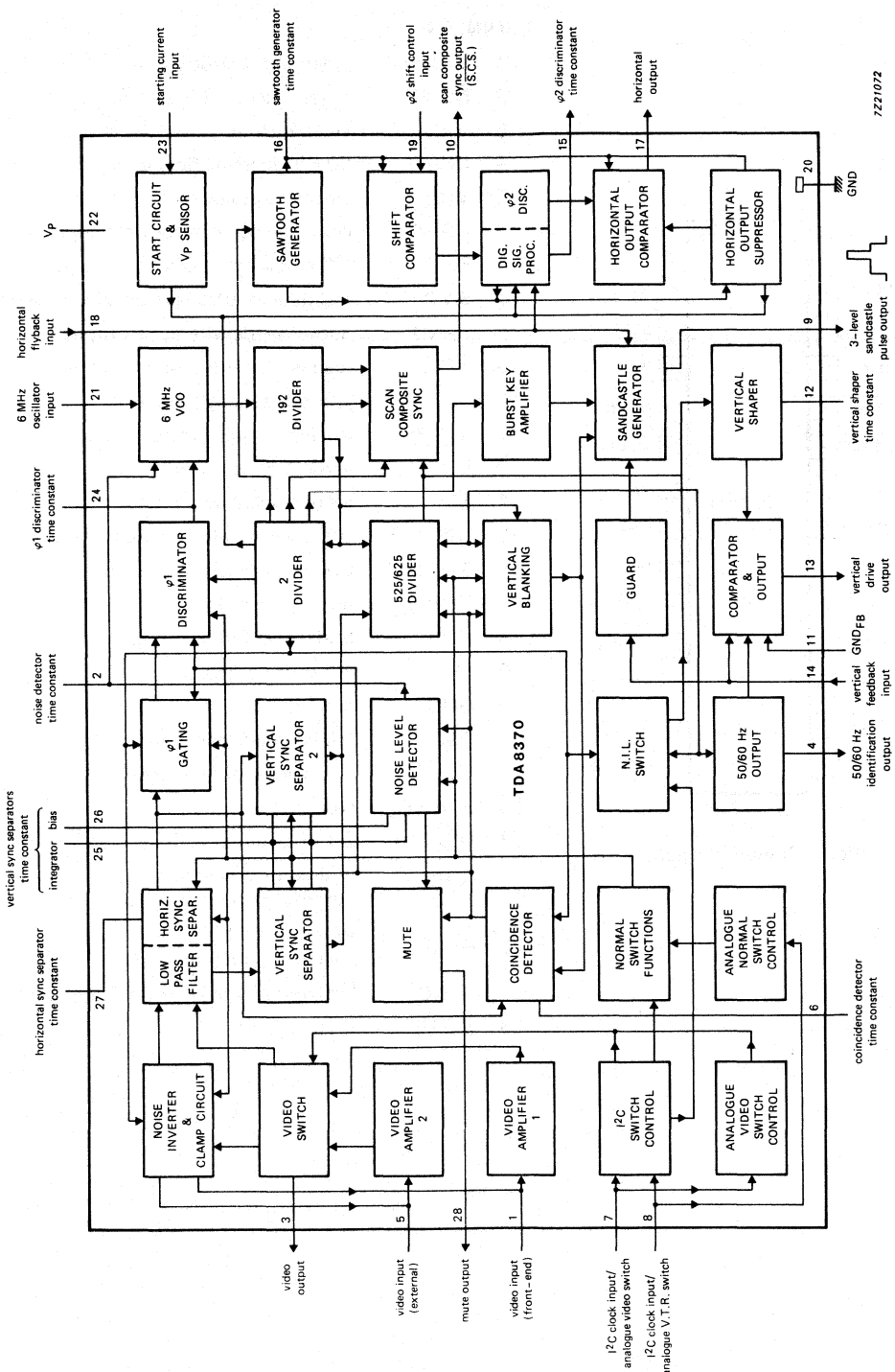


Fig. 1 Block diagram.

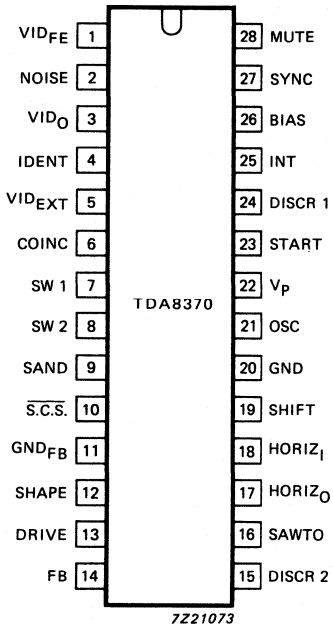


Fig. 2 Pinning diagram.

PINNING

1	VID_{FE}	video input (front-end)
2	NOISE	noise detector time constant
3	VID_O	video output
4	IDENT	50/60 Hz identification output
5	VID_{EXT}	video input (external)
6	COINC	coincidence detector time constant
7	SW 1	I^2C clock input/analogue video switch
8	SW 2	I^2C data input/analogue V.T.R. switch
9	SAND	3-level sandcastle pulse output
10	$\overline{S.C.S.}$	scan composite sync output
11	GND_{FB}	ground feedback input
12	SHAPE	vertical shaper time constant
13	DRIVE	vertical drive output
14	FB	vertical feedback input
15	DISCR 2	φ 2 discriminator time constant
16	SAWTO	sawtooth generator time constant
17	$HORIZ_O$	horizontal output
18	$HORIZ_I$	horizontal flyback input
19	SHIFT	φ 2 shift control input
20	GND	ground
21	OSC	6 MHz oscillator time constant
22	V_P	positive supply voltage
23	START	starting current input
24	DISCR 1	φ 1 discriminator time constant
25	INT	integrator time constant vertical sync separators
26	BIAS	time constant bias vertical sync separators
27	SYNC	horizontal sync separator time constant
28	MUTE	mute output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 22)	V_P	max.	13,2	V
Starting current (pin 23)	I_{23}	max.	10	mA
Power dissipation	P_{tot}	max.	2	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C
Thermal resistance				
From junction to ambient (in free)	$R_{th\ j\ a}$	=	40	K/W
Operating junction temperature	T_j	max.	150	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; I_{23} = 5,5 mA; 6 MHz clock oscillator operating at nominal frequency; synchronized; T_{amb} = 25 °C; measured in test set-up Fig. 6; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 22)	V_P	10	12	13,2	V
Supply current (pin 22)	I_P	–	125	150	mA
Starting current (pin 23)	I_{23}	5,0	5,5	10	mA
Video input (pin 1)					
A.C. coupled input voltage positive video (peak-to-peak value)	$V_{1\text{-}20(p\text{-}p)}$	–	2,25	3,0	V
D.C. level top sync	$V_{1\text{-}20}$	5,0	5,5	6,5	V
Input impedance	$\lvert Z_{1\text{-}20}\rvert$	–	20	–	kΩ
Generator resistance	R_G	–	75	150	Ω
Allowable sync compression *		20	–	–	dB
Video input (pin 5)					
A.C. coupled input voltage positive video (peak-to-peak value)	$V_{5\text{-}20(p\text{-}p)}$	–	1,0	1,4	V
D.C. level top sync	$V_{5\text{-}20}$	3,5	4,2	4,9	V
Input impedance	$\lvert Z_{5\text{-}20}\rvert$	–	20	–	kΩ
Generator resistance	R_G	–	75	150	Ω
Allowable sync compression		20	–	–	dB
Video output (pin 3)					
Output voltage** positive video (peak-to-peak value)	$V_{3\text{-}20(p\text{-}p)}$	2,7	3,0	3,3	V
D.C. level top sync	$V_{3\text{-}20}$	2,8	3,2	3,7	V
Resistance npn emitter follower	$R_{3\text{-}20}$	–	–	50	Ω
Bandwidth at $-I_3$ = 5 mA	B	10	15	–	MHz
Crosstalk between video signals pin 1 or pin 5 to pin 3		–	–	–54	dB
Noise inversion threshold level	$V_{3\text{-}20}$	1,9	2,1	2,3	V

* When not selected the negative-going input voltage is clamped at 0 V.

** Measured at $V_{1\text{-}20(p\text{-}p)}$ = 2,25 V or $V_{5\text{-}20(p\text{-}p)}$ = 1 V.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Horizontal sync separator (pin 27)					
D.C. voltage level	$V_{27\text{-}20}$	–	6,2	–	V
Line ripple voltage (peak-to-peak value)					
during standard mode	$V_{27\text{-}20}$	–	2,8	–	mV
during non-standard mode	$V_{27\text{-}20}$	–	0,6	–	mV
φ **1 discriminator** (pin 24)					
Catching range	$\pm \Delta f$	600	1000	1400	Hz
Holding range	$\pm \Delta f$	*	1000	1200	Hz
Phase shift		–	0,5	–	μs/kHz
Input resistance during sync pulse					
with slow time constant	$R_{24\text{-}20}$	–	12,6	–	kΩ
with fast time constant	$R_{24\text{-}20}$	–	2,2	–	kΩ
6 MHz VCO (pin 21)					
Output frequency free running at $V_{2\text{-}20} > 7$ V	f_o	–	6	–	MHz
Frequency variation without tolerance of external components	Δf_o	–	–	± 4	%
Frequency variation as a function of supply voltage	$\Delta f_o/\Delta V_p$	–	–	0,01	
Temperature coefficient of oscillator frequency	TC_{osc}	–	1400	–	Hz/K
A.C. input voltage (peak-to-peak value)	$V_{21\text{-}20(p\text{-}p)}$	–	0,3	–	V
D.C. input voltage	$V_{21\text{-}20}$	–	1,6	–	V
Sawtooth generator (pin 16)					
Start of negative slope of sawtooth	$V_{16\text{-}20}$	–	7,2	–	V
Start flyback of sawtooth	$V_{16\text{-}20}$	–	3,7	–	V
φ 2 trigger pulse width (see Fig. 3)	t_W	–	6,8	–	μs
φ 2 loop not synchronized by φ 1 loop					
Start of negative slope of sawtooth	$V_{16\text{-}20}$	–	7,2	–	V
Start flyback of sawtooth	$V_{16\text{-}20}$	–	3,4	–	V
Flyback time (see Fig. 3)	t_{fb}	0,9	1,3	1,7	μs
Output frequency free running at $V_p = 8{,}5$ V	f_o	–	15,4	–	kHz
Frequency variation without tolerance of external components	Δf_o	–	–	± 4	%

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Horizontal output (pin 17)					
Output current open collector npn; V_{17-20} = 0,5 V	I_{17}	–	–	10	mA
Output voltage protection (2 internal zener diodes)	V_{17-20}	14	–	16	V
Maximum output current during voltage protection	I_{17}	–	0	1	mA
Delay between start of sawtooth output pulse at pin 16 and:					
negative-going edge of horizontal output voltage (see Fig. 3)	t_{d1}	14,5	16	17,5	μs
positive-going control edge of horizontal output voltage (see Fig. 3)	$t_{d2(min.)}$	25	28	31	μs
	$t_{d2(max.)}$	–	T_H	–	μs
	t_{d2}*	–	T_H	–	μs
Condition: I_{23} = 5 to 10 mA					
Horizontal output pulse present if:	V_{23-20}	–	–	6	V
Horizontal output pulse not present if:	V_{23-20}	4	–	–	V
and	I_{23}	3	–	–	mA
δ Horizontal output is a function of the input voltage at pin 23					
δ = 0	V_{23-20}	–	–	4	V
δ = maximum	V_{23-20}	8,5	–	–	V
Horizontal output suppression time	t_s	20	22	24	μs
φ 2 discriminator (pin 15)					
Control current	$\pm I_{15}$	600	800	1000	μA
Control sensitivity	$\Delta\varphi_i/\Delta\varphi_o$	–	400	–	
Input current at V_{15-20} = 4 V; V_P = 0 V	I_{15}	–	–	0,6	μA
Condition: No flyback pulse and $V_{23-20} > 5$ V					
Output voltage at pin 15	V_{15-20}	2,7	3	3,3	V
Condition: $V_P < 8,9$ V					
Output voltage at pin 15	V_{15-20}	2,7	3	3,3	V

* Delay with no horizontal flyback pulse present at pin 18.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
φ 2 shift control input (pin 19)					
Shift control range		–	$1/16T_H+\Delta$	–	μs
Δ		0,2	–	1	μs
Delay between rising edge of horizontal flyback at the slicing level and rising edge of burst key pulse (see Fig. 2)	$t_{d3(min.)}$	–	3	–	μs
	$t_{d3(max.)}$	–	$7+\Delta$	–	μs
t_{d3} = min. when:	V_{19-20}	–	–	4,5	V
t_{d3} = max. when:	V_{19-20}	0	–	–	V
Shift control is active when:	V_{22-20}	$>8,9$	$>9,5$	>10	V
Starting control input (pin 23)					
Starting by current to pin 23: minimum	I_{23}	3	–	5	mA
maximum allowed	I_{23}	–	–	10	mA
Starting by a voltage on pin 22: required input current	I_{23}	0	–	10	mA
Stabilized voltage	V_{23-20}	8,2	8,7	9,2	V
Supply current is added to starting current if: $V_P > V_{23-20}$ and $V_{23-20} < 8,5$ V	V_{23-20}	–	V_P-V_{BE}	–	V
Horizontal flyback input (pin 18)					
Slicing level input voltage	V_{18-20}	0,7	0,9	1,1	V
Input current	I_{18}	0,3	1	4	mA
Maximum input current	$-I_{18}$	–	–	1	mA
Maximum input voltage	V_{18-20}	–	–	V_P	V
Vertical sync separator integrator time constant (pin 25)					
Condition: Standard mode					
D.C. voltage level of vertical sync top of integrated video	V_{25-20}	8,5	9,0	9,5	V
black level of integrated video during vertical blanking	V_{25-20}	4,0	4,5	5,0	V
Input resistance	R_{25-20}	–	5,1	–	kΩ
Condition: Non-standard mode					
Input voltage level of integrated vertical sync top level	V_{25-20}	9,5	10,7	11,0	V
integrated vertical sync amplitude (peak-to-peak value)	$V_{25-20(p-p)}$	–	8,9	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Vertical sync separator biasing (pin 26)					
Input voltage in standard mode	$V_{26\text{-}20}$	–	5,9	–	V
Input voltage in non-standard mode	$V_{26\text{-}20}$	–	8,4	–	V
Vertical shaper (pin 12)					
Condition: 50 Hz					
Ramp voltage starting level	$V_{12\text{-}20}$	–	2	–	V
Flyback voltage starting level	$V_{12\text{-}20}$	6,0	6,25	6,5	V
Condition: 60 Hz					
Ramp voltage starting level	$V_{12\text{-}20}$	–	2	–	V
Flyback voltage starting level	$V_{12\text{-}20}$	5,35	5,6	5,85	V
Flyback time (normal)	t_{fb}	170	220	270	μs
Flyback time controlled by second half of N.I.L. signal		–	$t_{fb}-32$	–	μs
Vertical drive output (pin 13)					
Open collector pnp					
Maximum output current at $V_{13\text{-}20}$ = 8 V	$-I_{13}$	3	–	–	mA
Output voltage LOW with 100 kΩ resistor to ground	$V_{13\text{-}20}$	–	–	300	mV
Vertical feedback input (pin 14)					
A.C. input voltage not synchronized					
50 and 60 Hz condition: non-standard mode input voltage (peak-to-peak value)	$V_{14\text{-}11(p\text{-}p)}$	–	3	–	V
d.c. average input voltage	$V_{14\text{-}11}$	–	2,8	–	V
Parabolic pre-correction convex (50 Hz)		–	4	–	%
Parabolic pre-correction convex (60 Hz)		–	3,3	–	%
Guard circuit input					
input voltage HIGH	$V_{14\text{-}11}$	5,3	5,7	6,1	V
input voltage LOW	$V_{14\text{-}11}$	–	–	0	V
input voltage at $V_{14\text{-}20}$ = 2,5 V	$-I_{14}$	–	1,5	6,1	μA
Ground feedback input (pin 11)					
A.C. feedback voltage	$V_{11\text{-}20}$	–	0	–	V

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
50/60 Hz identification output (pin 4)					
50 Hz output voltage at I_4 = 0,1 mA	V_{4-20}	–	1,3	1,7	V
60 Hz output voltage at $-I_4$ = 5 mA	V_{4-20}	8	10	–	V
3-level sandcastle output (pin 9)					
Output voltage during burst key at $-I_9$ = 0,5 mA	V_{9-20}	–	10,8	–	V
at $-I_9$ = 5 mA	V_{9-20}	8,0	9,7	–	V
Output voltage during horizontal blanking at $-I_9$ = 0,5 mA	V_{9-20}	4,1	4,4	4,9	V
Output voltage during vertical blanking at $-I_9$ = 0,5 mA	V_{9-20}	2,1	2,6	2,9	V
Zero level output voltage at I_9 = 0,5 mA	V_{9-20}	–	0,25	0,5	V
Pulse width:					
burst key at V_{9-20} = 7 V	t_W	3,7	4,0	4,3	μs
horizontal blanking at V_{9-20} = 3,5 V	t_W	–	*	–	
Vertical blanking (see Fig. 4)					
Condition: 50 Hz direct synchronization					
Start of vertical blanking with respect to start of vertical sync, dependent on integration at pin 25	t_{bk}	–	16	–	μs
Duration of vertical blanking	t_d	–	$22{,}5T_H - t_{bk}$	–	μs
Condition: 50 Hz indirect synchronization					
Start of vertical blanking with respect to start of vertical sync	t_{bk}	–	$-(2{,}5T_H + 20\ \mu s)$	–	
Duration of vertical blanking	t_d	–	$25T_H + 2\ \mu s$	–	
Condition: 60 Hz direct synchronization					
Start of vertical blanking with respect to start of vertical sync, dependent on integration at pin 25	t_{bk}	–	16	–	μs
Duration of vertical blanking	t_d	–	$18{,}5T_H - t_{bk}$	–	μs
Condition: 60 Hz indirect synchronization					
Start of vertical blanking with respect to start of vertical sync	t_{bk}	–	0	–	μs
Duration of vertical blanking	t_d	–	$18{,}5T_H$	–	μs
Phase position of burst key delay between the middle of the sync pulse on the video input and the rising edge of the burst key pulse at a slicing level of 7 V		2,5	2,9	3,3	μs

* Width of horizontal flyback on pin 18 pulse at the slicing level.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
$\overline{\text{S.C.S.}}$ output (pin 10)					
Output voltage HIGH at $-I_{10} = 5$ mA	V_{10-20}	4,3	4,8	5,3	V
Output voltage LOW at $I_{10} = 0{,}5$ mA	V_{10-20}	–	0,2	0,5	V
Conditions:*					
Noise only on video input pin 1 or 5 or indirect sync 50 Hz with a 4,7 μs horizontal sync pulse width on pin 1 or 5					
Delay between the starting edge of the horizontal sync pulse of the video input signal and the starting edge of the horizontal sync pulse in the $\overline{\text{S.C.S.}}$ signal		–0,25	0	0,25	μs
Noise detector time constant (pin 2)					
Condition: Standard mode					
Output voltage					
strong signal	V_{2-20}	–	4,6	5,3	V
noise only**	V_{2-20}	–	7,2	–	V
Switching voltage level					
strong signal → noise only	V_{2-20}	5,7	6,2	6,7	V
noise only → strong signal	V_{2-20}	–	5,6	–	V
Coincidence detector (pin 6)					
Average voltage level					
in-sync	V_{6-20}	6,8	8	–	V
out-of-sync	V_{6-20}	–	–	2,1	V
noise only	V_{6-20}	–	–	2,4	V
Switching voltage level (see also Fig. 5)					
fast → normal$^{\Delta}$	V_{6-20}	–	4,4	–	V
normal → fast$^{\Delta}$	V_{6-20}	–	2,4	–	V

* All other conditions will cause distorted vertical sync pulses and/or equalizing pulses in the $\overline{\text{S.C.S.}}$ signal.

** When noise only is received the 6 MHz oscillator is switched to nominal frequency and the frame divider to the 625 standard.

Δ This switching level is also valid for clamp gating, φ 1 gating, muting, frame divider indirect/direct sync, horizontal sync separator gated/self-aligned and noise detector inhibit/inhibit off.

parameter	symbol	min.	typ.	max.	unit
Mute output (pin 28)					
Output voltage					
not synchronized					
at $-I_{28}$ = 0,5 mA	V_{28-20}	–	10,5	–	V
at $-I_{28}$ = 5 mA	V_{28-20}	7,0	8,5	–	V
synchronized					
at I_{28} = 0,1 mA	V_{28-20}	–	1,2	1,5	V
I²C clock input/ analogue input video switch (pin 7)					
Input voltage					
analogue input inactive	V_{7-20}	5	–	–	V
analogue input switching level (external video selected)	V_{7-20}	6,5	–	7,5	V
Input current					
at V_P = 0 V	$\|I_7\|$	–	–	10	μA
at V_P = 12 V	$-I_7$	–	–	10	μA
I²C clock input switching voltage level	V_{7-20}	1,5	2,6	3,0	V
I²C data input/ * analogue V.T.R. switch (pin 8)					
Input voltage					
analogue input inactive	V_{8-20}	5	–	–	V
analogue input switching level (non-standard mode)	V_{8-20}	6,5	–	7,5	V
Input current					
at V_P = 0 V	$\|I_8\|$	–	–	10	μA
at V_P = 12 V	$-I_8$	–	–	10	μA
I²C data input switching voltage level	V_{8-20}	1,5	2,6	3,0	V
During acknowledge					
pull-down current	$-I_8$	–	–	5	mA
saturation voltage	V_{8-20}	–	–	1,5	V

DEVELOPMENT DATA

* For address and data byte definition see Fig. 6 and Table 1 respectively.

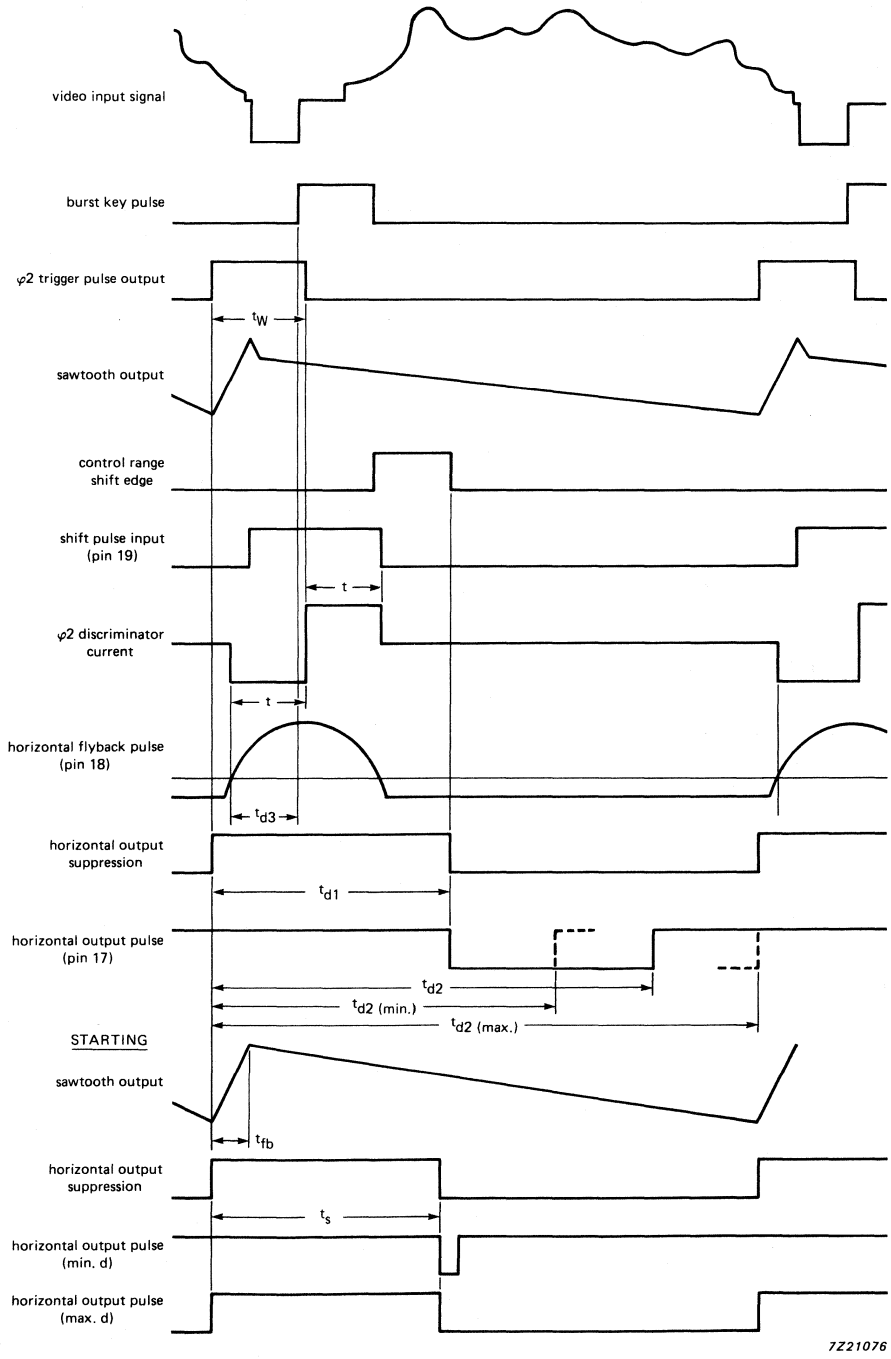


Fig. 3 Timing diagram; video input and starting time.

DEVELOPMENT DATA

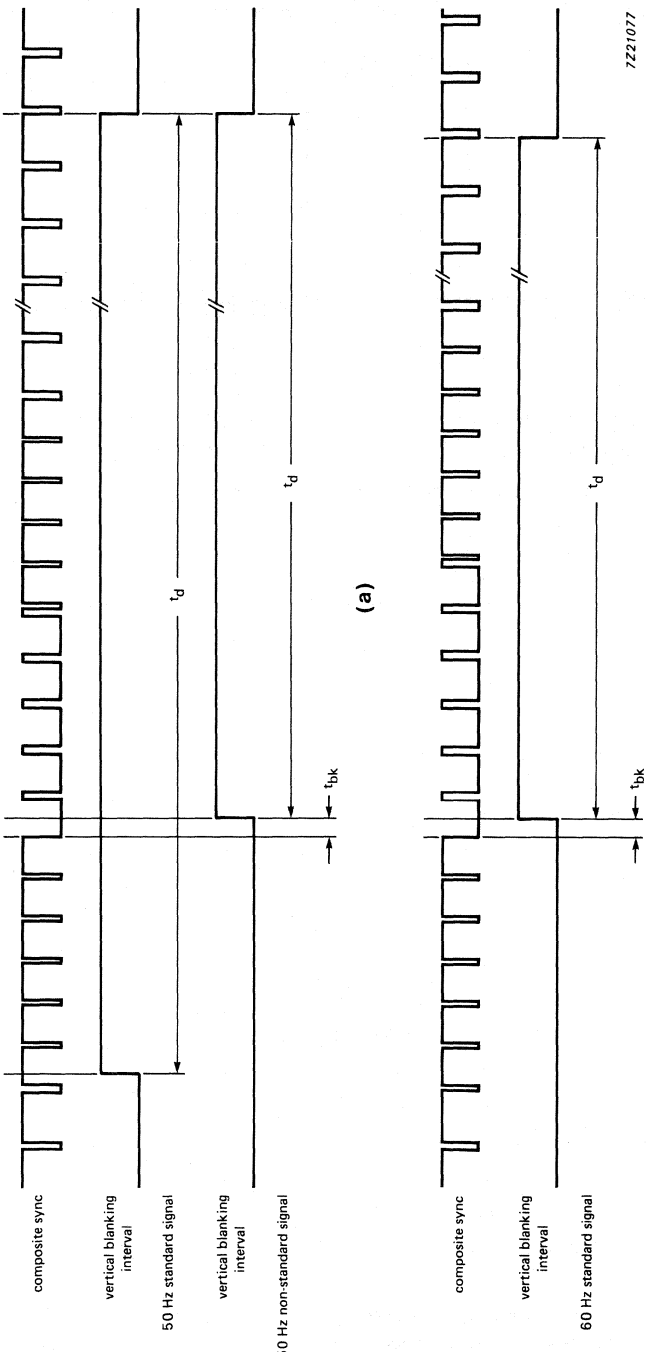
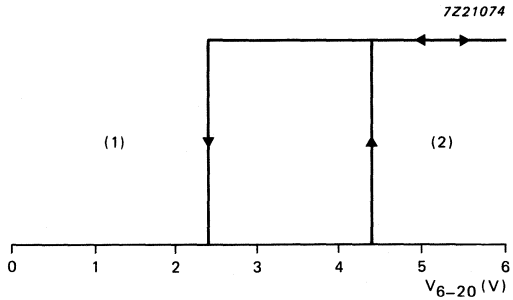


Fig. 4 Timing diagram; vertical blanking synchronization
(a) 50 Hz standard (b) 60 Hz standard.



(1) φ 1 gating circuit off
φ 1 discriminator to fast mode
clamping gate off
mute output HIGH
frame divider direct sync
horizontal sync separator self-aligned
noise detector not inhibited

(2) φ 1 gating circuit on
φ 1 discriminator to slow mode
clamping gate on
mute output LOW
frame divider indirect sync
horizontal sync separator gated
noise detector inhibited

Fig. 5 Coincidence detector time constant switching levels.

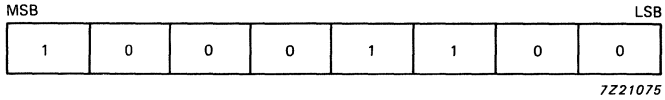


Fig. 6 Address byte.

Table 1 Data byte

	bit no.	logic level	description
MSB	D7	1	*
	D6	1	*
	D5	1	*
	D4	1	*
	D3	1	bit number D5 = don't care
	D3	0	bit numbers D6 and D7 = don't care
	D2	1	$\overline{\text{N.I.L.}}$ (inactive)
	D2	0	N.I.L. (active)
	D1	1	$\overline{\text{VID}_{\text{EXT}}}$ (inactive)
	D1	0	VID_{EXT} (active)
	D0	1	standard mode
LSB	D0	0	non-standard mode

* Bits D7 to D4 are used for measuring procedure in the IC factory. For application use they must be inactive (logic 1).

DEVELOPMENT DATA

APPLICATION INFORMATION

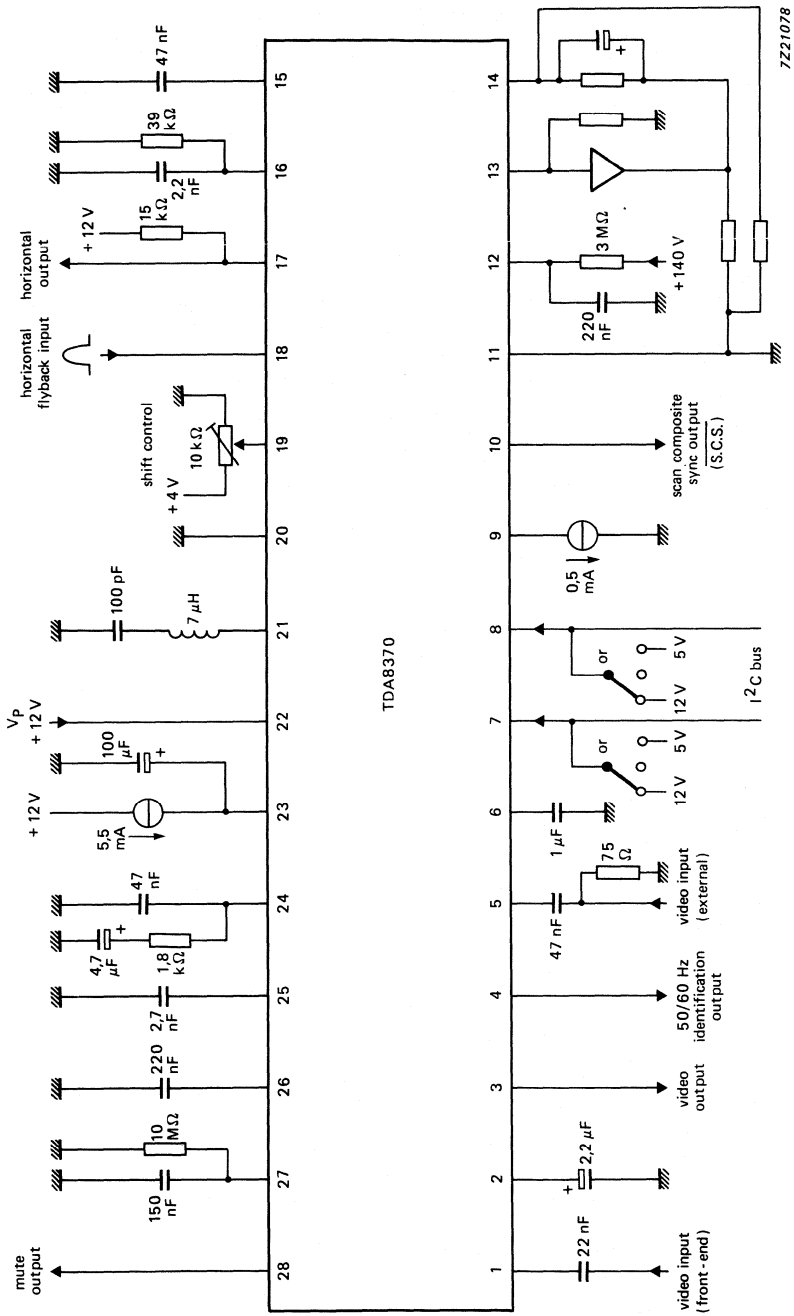


Fig. 7 Application diagram and test circuit.

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH I²C BUS CONTROL

GENERAL DATA

The TDA8405 integrated circuit is a processor for stereo/dual-language signals for stereo-sound television receivers and VTR. The modulated signals at the TDA8405 inputs need to be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The second channel is also modulated with the pilot carrier. The IC is controlled via the two-line, bidirectional I²C bus.

Features

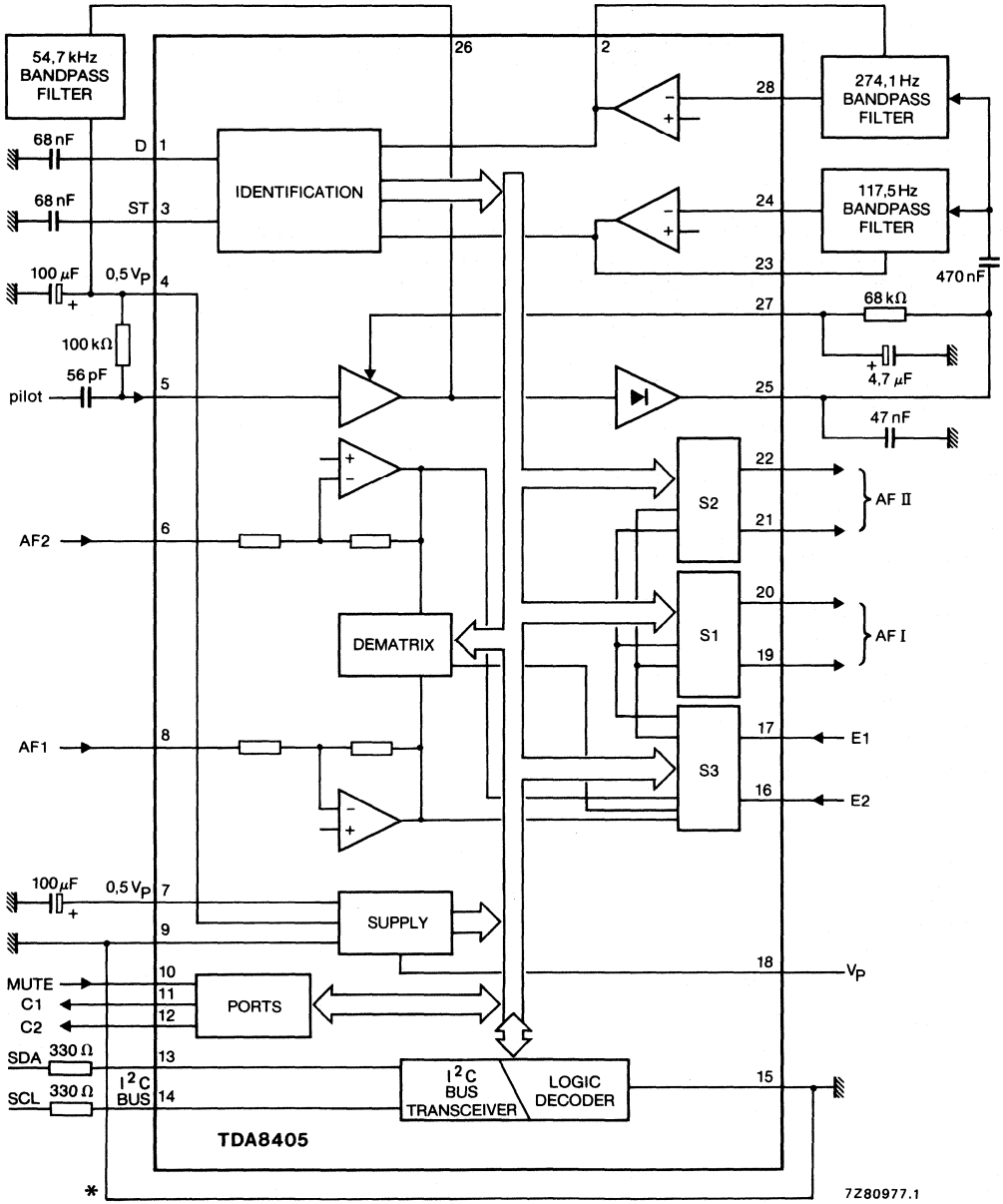
- Amplification of the two a.f. input signals by integrated operational amplifiers.
- Low distortion stereo dematrix
- All operational amplifiers are offset compensated
- I²C bus transceiver for system control (port control, mute, mode select, identification, etc.)
- Input port for fast muting
- Two general purpose output ports (three-state, bus-controlled)

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{18\text{-}9\text{-}15}$	typ.	12 V
Supply current	$I_P = I_{18}$	typ.	25 mA
A.F. input signal	$V_{i(rms)} = V_{6\text{-}9}, V_{8\text{-}9}$	typ.	1 V
Weighted signal-to-noise ratio of the a.f. output-signals (CCIR 468/2)	(S+N)/N	⩾	70 dB
Crosstalk attenuation: stereo mode at f = 1 kHz	α_S	>	40 dB
dual sound mode at f = 40 to 12 500 Hz	α_{DS}	>	70 dB
Pilot signal input sensitivity	$V_i = V_{5\text{-}9(rms)}$	typ.	5 mV
Pilot signal amplifier gain control range	ΔG_V	>	40 dB

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).



* Direct connection between pins 9 and 15 is needed.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)*	$V_P = V_{18\text{-}9,15}$	max. 13,2	V
Output current (pins 19, 20, 21, 22)	I_n	max. 5	mA
Output current (pins 2, 23)	I_n	max. 1	mA
Output current (pins 11, 12)	I_n	max. 3	mA
Voltage range at any pin	V_n	0 to V_P	V
Total power dissipation	P_{tot}	max. 1	W
Storage temperature range	T_{stg}	−40 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when pins 9 and 15 are connected to ground.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; $V_{i(af)rms}$ = 1 V; f = 1 kHz; dematrix aligned; $V_{i\ pilot(rms)}$ = 16 mV; test circuit Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage	$V_P = V_{18-9, 15}$	10,8	12	13,2	V
Supply current at V_P = 12 V	$I_P = I_{18}$	–	25	–	mA
Reference voltage	$V_{ref} = V_{4-9, 15}$	–	$V_P/2$	–	V
DC levels (pins 5, 6, 7, 8, 16 17, 19, 20, 21, 22, 24, 28)	$V_{n-9, 15}$	–	$V_P/2$	–	V
BUS TRANSCEIVER (pins 13, 14) (note 1)					
Clock SCL					
Voltage level LOW	V_{14-15}	−0,3	–	1,5	V
Voltage level HIGH	V_{14-15}	3,0	–	–	V
Timing LOW period	t_{PL}	4,7	–	–	μs
Timing HIGH period	t_{PH}	4,0	–	–	μs
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	0,3	μs
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	$-I_{IL}$	–	–	10	μA
Data					
Voltage level LOW	V_{13-15}	−0,3	–	1,5	V
Voltage level HIGH	V_{13-15}	3,0	–	–	V
Rise time	t_r	–	–	1,0	μs
Fall time	t_f	–	–	0,3	μs
Set-up time data	t_{SU}	0,25	–	–	μs
Input current HIGH	I_{13}	–	–	10	μA
Input current LOW	$-I_{13}$	–	–	10	μA
Output current LOW	$+I_{13}$	3,0	–	–	mA
MUTE PORT (pin 10) note 2					
Input voltage LOW	V_{10-15}	–	–	1,5	V
Input voltage HIGH	V_{10-15}	8	–	–	V

parameter	symbol	min.	typ.	max.	unit
CONTROL PORTS (pins 11, 12)					
3-state HIGH, LOW, high ohmic					
Output resistance in open state	$R_{11, 12\text{-}15}$	50	–	–	kΩ
Output voltage LOW	$V_{11, 12\text{-}15}$	–	–	0,8	V
Output voltage HIGH	$V_{11, 12\text{-}15}$	V_{P}-1	–	–	V
Output current LOW	$I_{11, 12}$	500	–	–	μA
Output current HIGH	$-I_{11, 12}$	80	–	–	μA
IDENTIFICATION (See Fig. 3)					
Input amplifier and demodulator					
Input voltage	$V_{5\text{-}9(p\text{-}p)}$	–	–	2,0	V
Min. input voltage	$V_{5\text{-}9(rms)}$	5,0	–	–	mV
Input resistance	$R_{5\text{-}9}$	500	–	–	kΩ
Gain	$G_{25\text{-}9}$	–	42	–	dB
Gain control range	ΔG	40	–	–	dB
Output voltage (gain-controlled)	$V_{25\text{-}9(p\text{-}p)}$	–	1,5	–	V
Operational amplifiers					
Input current	$I_{24, 28}$	–	70	–	nA
Gain at f = 200 Hz	$G_{23\text{-}24}$, $G_{2\text{-}28}$	78	–	–	dB
Output current	$I_{2, 23}$	1,5	–	–	mA
Output resistance	$R_{2, 23\text{-}9}$	–	2	–	kΩ
Output load capacitance	$C_{2, 23\text{-}9}$	–	–	30	pF
Schmitt trigger					
A.C. input signal	$V_{2, 23\text{-}9(rms)}$	–	1	–	V
Internal discharge resistors	$R_{1, 3\text{-}9}$	–	3	–	kΩ
A.F. STAGES					
Input resistance (pins 6, 8, 16 and 17)	$R_{n\text{-}9}$	10	–	–	kΩ
Gain ($V_{19, 20, 21, 22\text{-}9}/V_{6, 8\text{-}9}$)	G1	–	6	–	dB
Gain ($V_{19, 20, 21, 22\text{-}9}/V_{16, 17\text{-}9}$)	G2	–	0	–	dB
Input voltage	$V_{6, 8\text{-}9(rms)}$	–	1	–	V
Crosstalk attenuation (notes 3, 4 and 9)					
dual sound	α_{DS}	70	–	–	dB
stereo f = 250 Hz to 6,3 kHz	α_{S}	40	–	–	dB
stereo f = 40 Hz to 250 Hz; 6,3 kHz to 12,5 kHz	α_{S}	30	–	–	dB

DEVELOPMENT DATA

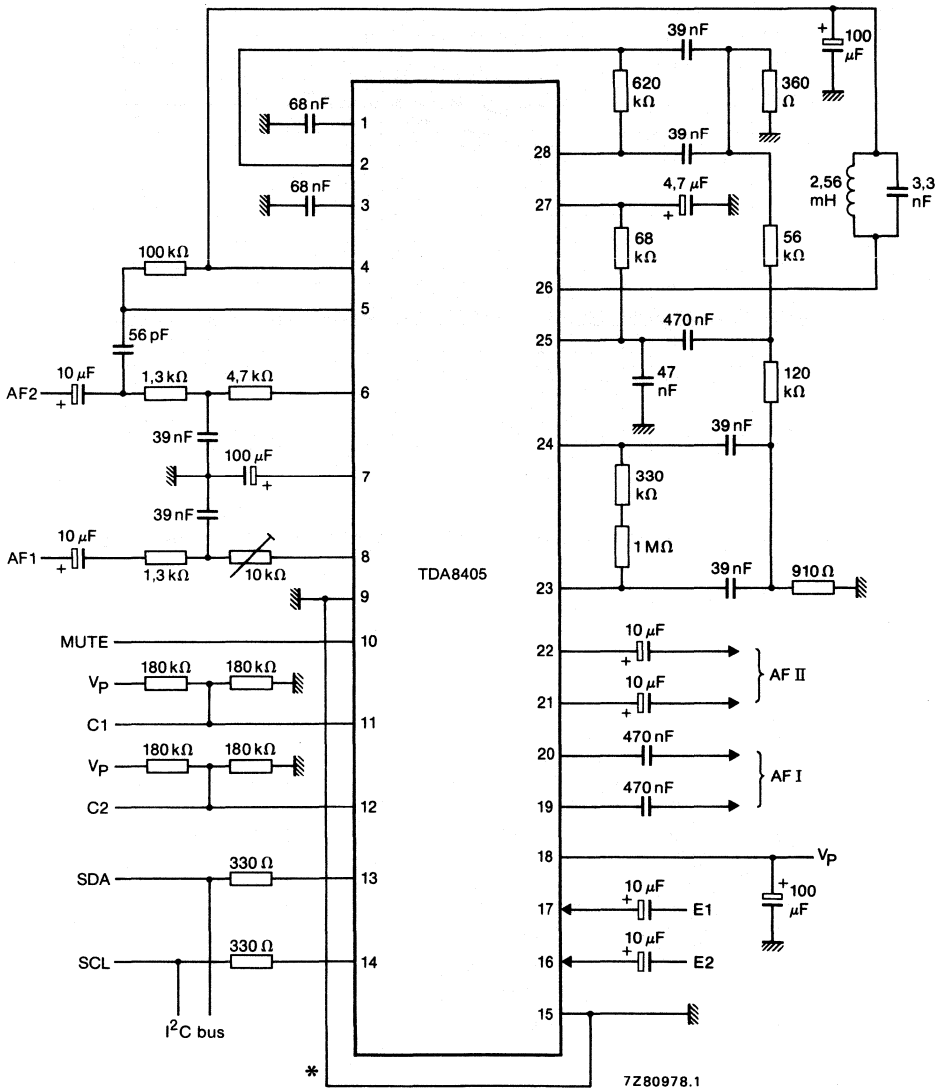
CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
A.F. STAGES (continued)					
Output resistance	$R_{19,20,21,22}$	–	200	300	Ω
Output load capacitance (pins 19, 20, 21 and 22)	$C_{n\text{-}9}$	–	–	1,5	nF
D.C. offsets (note 8) at pins 19,20,21 and 22	ΔV	–	–	30	mV
Total harmonic distortion (notes 4 and 5)	THD	–	0,1	0,5	%
Output signal (r.m.s. value) (pins 19, 20, 21 and 22)	$V_{n\text{-}9(rms)}$	–	–	2,0	V
Ripple rejection (note 6)	RR	30	35	–	dB
Noise rejection (note 7) (noise from I^2C bus)	NR	80	–	–	dB
Signal-to-noise ratio (note 7)	(S+N)/N	70	–	–	dB
Ident signal suppression		70	–	–	dB
Signal suppression during mute (notes 4 and 7)		70	–	–	dB

Notes to the characteristics

1. Full specification of the I^2C bus will be supplied on request.
2. Programmable mute state. If the SC3 bit in the I^2C bus is LOW then the mute input is active LOW; if the mute bit is set to HIGH then the mute input is active HIGH.
3. Crosstalk attenuation definition: 20 log (unwanted output signal/input signal).
4. Frequency range: 40 Hz $< f <$ 12,5 kHz.
5. In dual sound mode.
6. Test circuit as in Fig. 4: ripple rejection = output modulation due to hum on the supply line.
7. Related to 2 V (r.m.s.) output signal at pin 19, 20, 21 or 22; noise weighted according to CCIR 468/2.
8. Caused by any change of the switch position.
9. α_S measured without de-emphasis network.

DEVELOPMENT DATA



* Direct connection between pins 9 and 15 is needed.

Fig. 2 Test circuit.

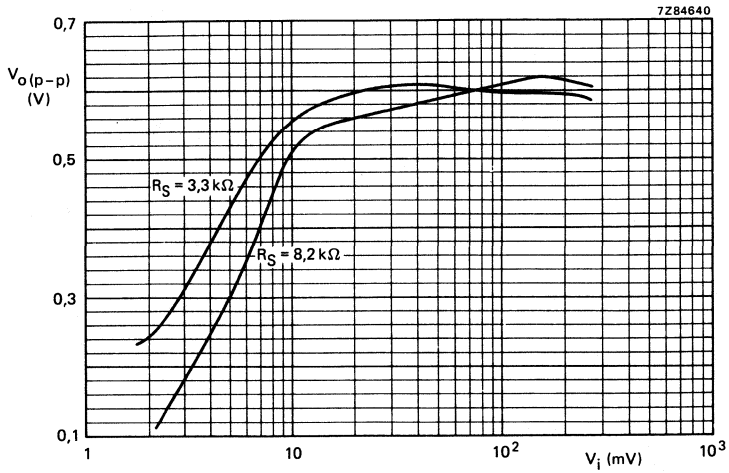


Fig. 3 Controlled output voltage as a function of the input signal (Q = 80); pilot frequency f_o = 54 kHz; R_S = source resistance.

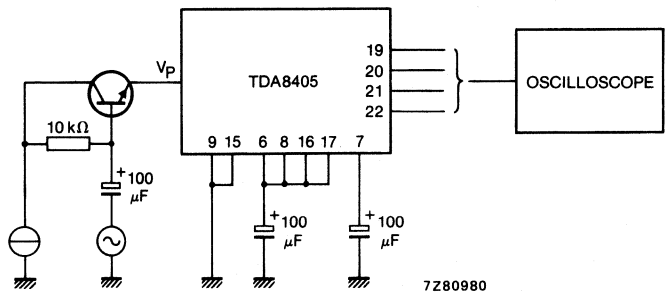
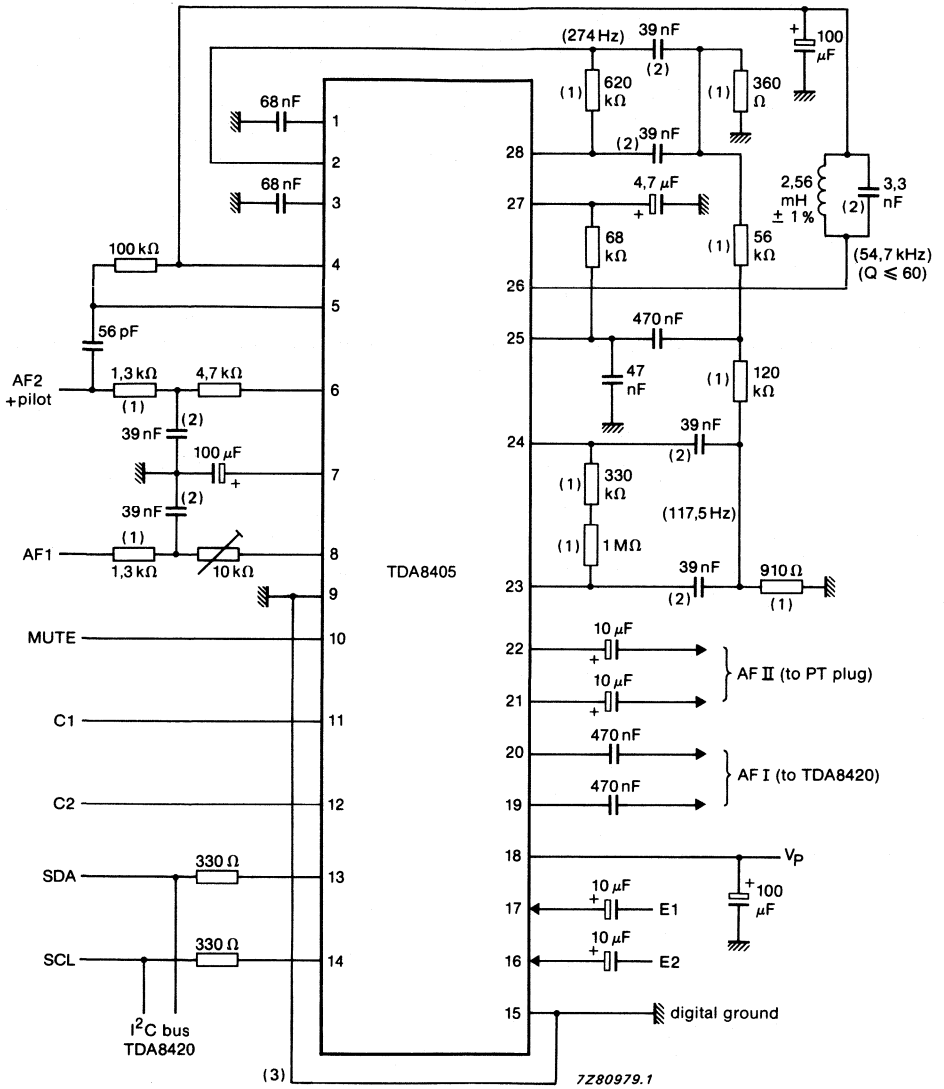


Fig. 4 Test circuit for ripple rejection: supply (d.c.) + pulse (r.m.s.) voltage at 100 Hz = 12 V + 50 mV.

DEVELOPMENT DATA



(1) ± 1 % tolerance

(2) polystyrene film/foil capacitors (KS) : ± 1 % tolerance

metallized polyethylenetherephthalate film capacitors (MKT) : ± 10 % tolerance

(3) Direct connection is needed between pins 9 and 15

Fig. 5 Application diagram.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8420 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	–46	–	16	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB
Volume control range CH2	G	–62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT-117).

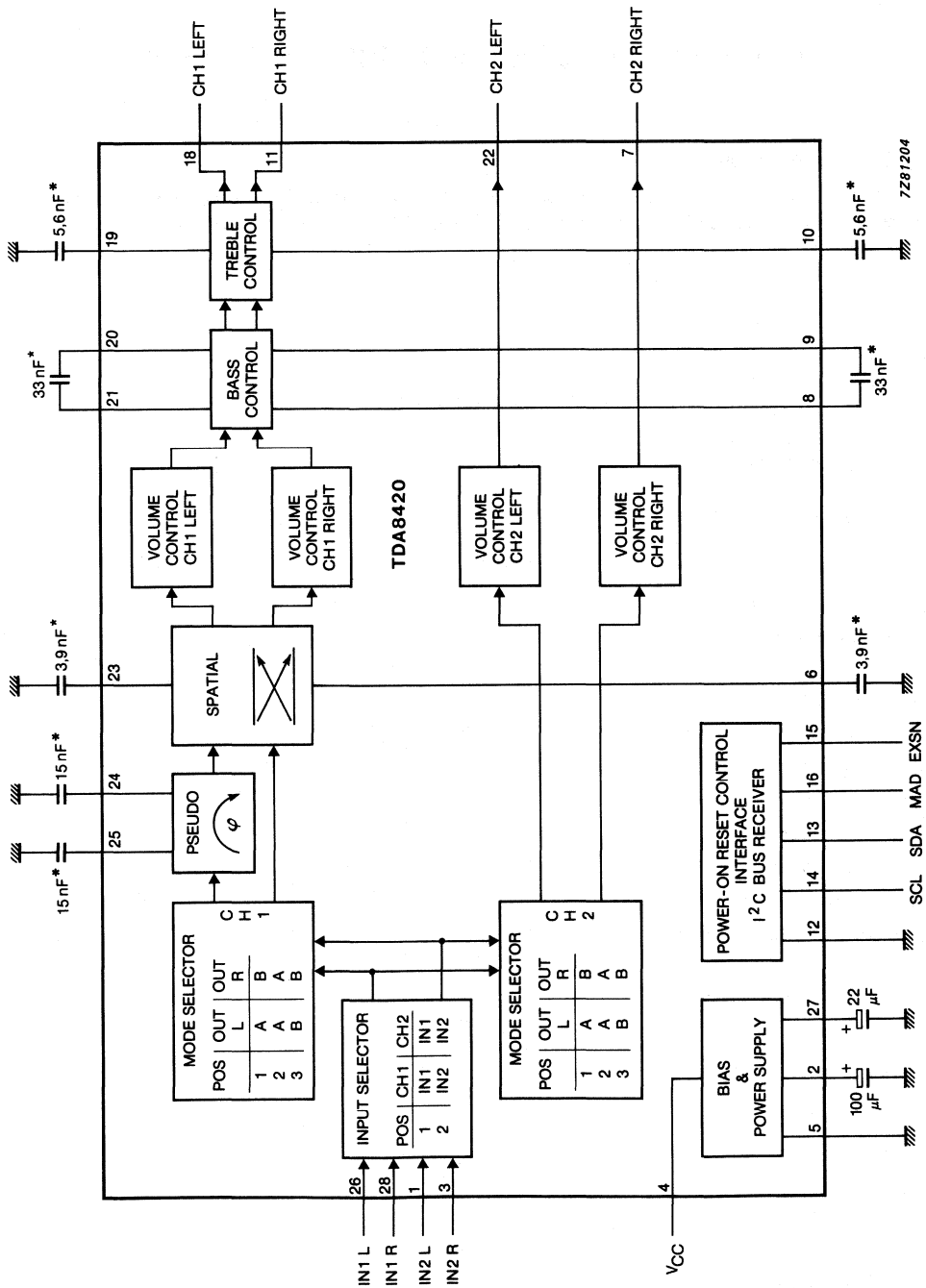


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

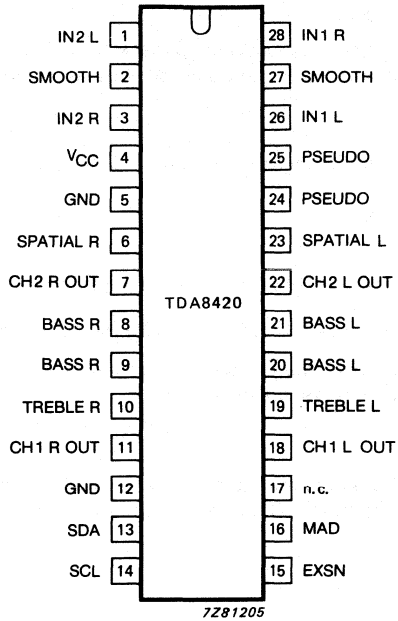


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8420 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8420 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA — serial data, SCL — serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8420 starts with the module address MAD.

MSB								LSB
1	0	0	0	0	0	MAD	R/W	ACK

Fig. 3 TDA8420 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8420s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8420. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8420. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
CH1	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
CH2	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Where: POR = Power-On Reset.

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	Vx5	Vx4	Vx3	Vx2	Vx1	Vx0
16	0	1	1	1	1	1	1
–46	–62	1	0	0	0	0	0
⩽ –90	⩽ –90	0	1	1	1	1	1
⩽ –90	⩽ –90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation ⩾ 90 dB.

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

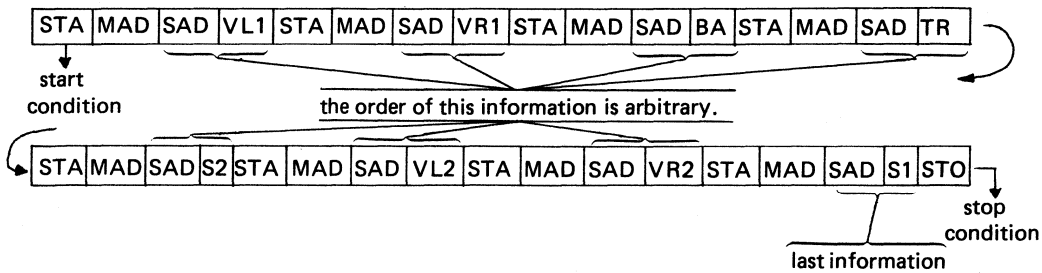


Fig. 4 Data transmission after a power-on reset.

Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Input voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I	0	V_{CC}	V
Output voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation				
at $T_{amb} < 70$ °C	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	−25	150	°C

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current					
at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Input voltage					
IN1 L, IN1 R, IN2 L, IN2 R					
DC voltage internally generated;					
capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage					
CH1 (pins 11 and 18);					
CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
External capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15)					
at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = −4 dB; THD ⩽ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value)					
at THD ≤ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level					
weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = ≤ −90 dB	V_n	–	15	–	μV
Total harmonic distortion					
(f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,5 V;					
gain = + 16 dB to −30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V;					
gain = + 2 dB to −30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V;					
gain = −4 dB to −30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz					
gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB;					
bass and treble in linear position)					
f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic					
inputs to AF outputs (gain = 0 dB;					
bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–46 dB step)	G_{min}	–43	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –46 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for $C_{10\text{-}5}$; $C_{19\text{-}5}$ = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for $C_{8\text{-}9}$; $C_{20\text{-}21}$ = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	50	–	%
Pseudo: Phase shift			(see Fig. 15)		

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD ⩽ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = ⩽ –90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz) for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to –30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to –30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = –4 dB to –30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.

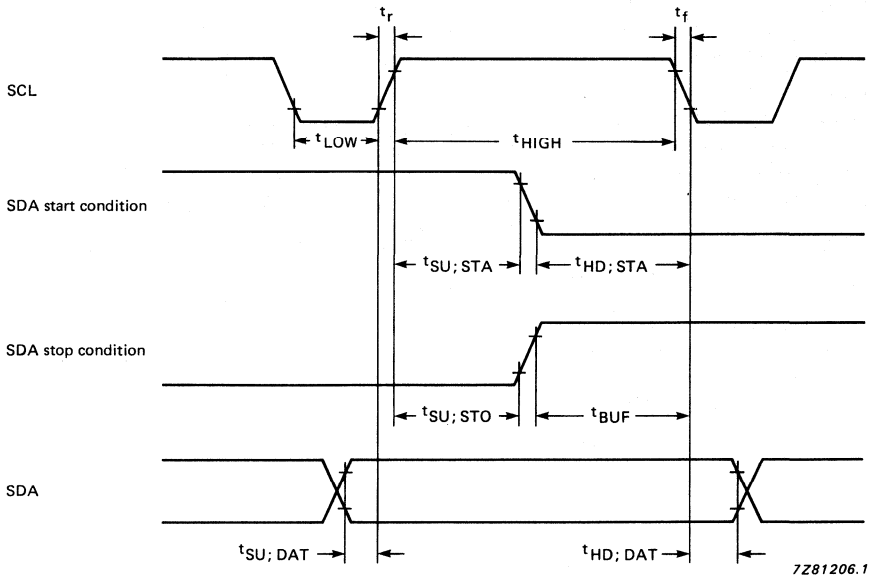


Fig. 6 Timing requirements for I²C bus.

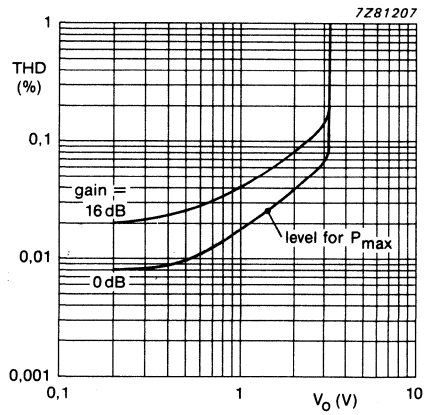


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

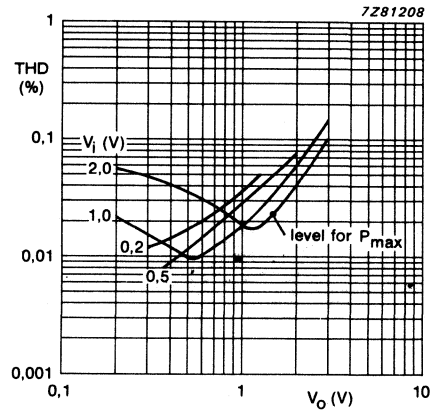


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

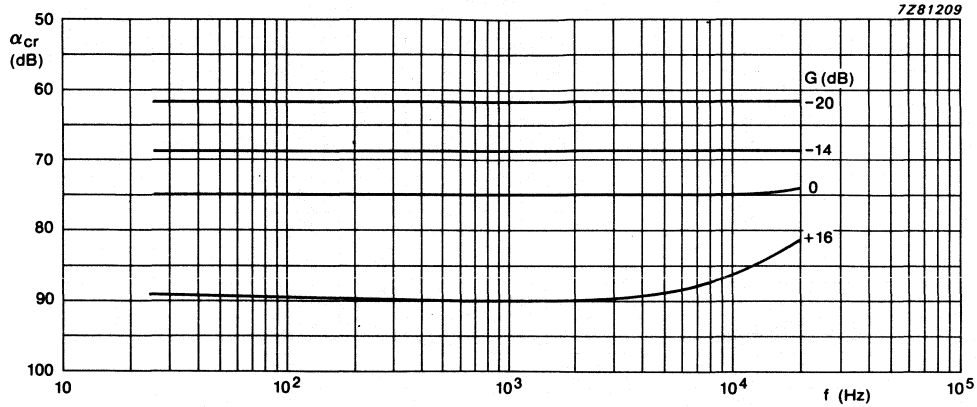


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

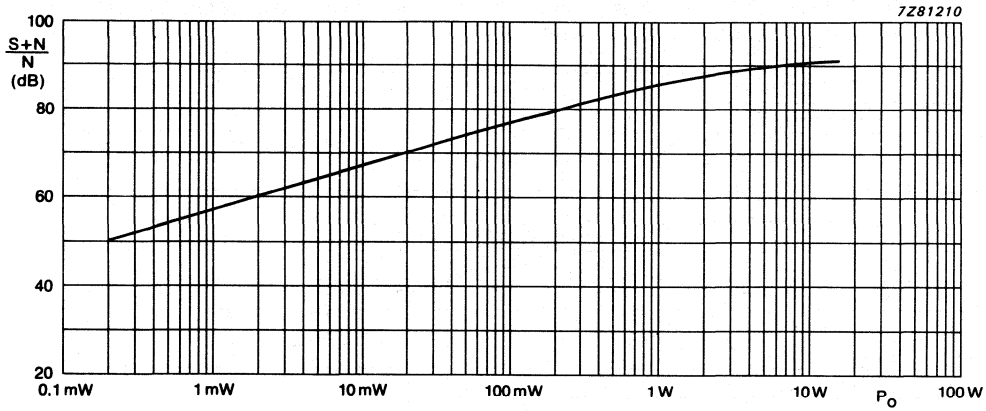


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

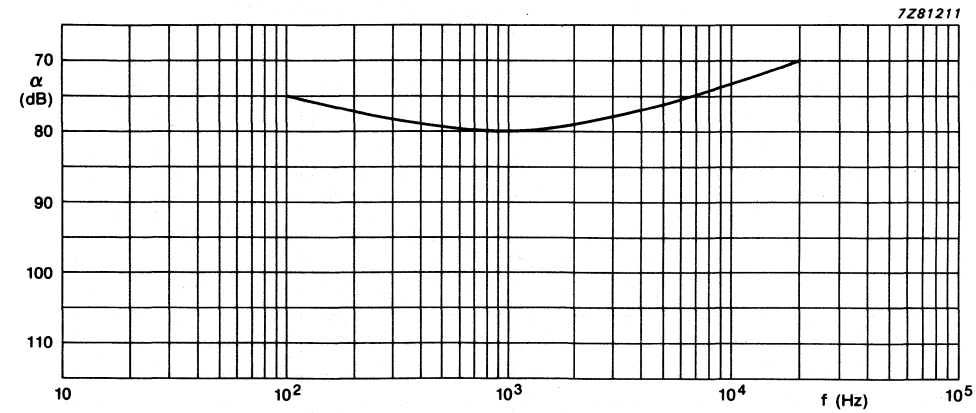


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

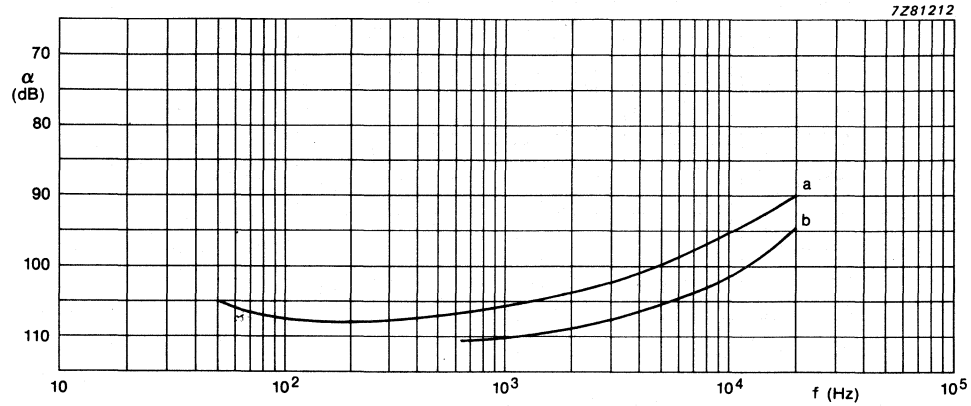


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

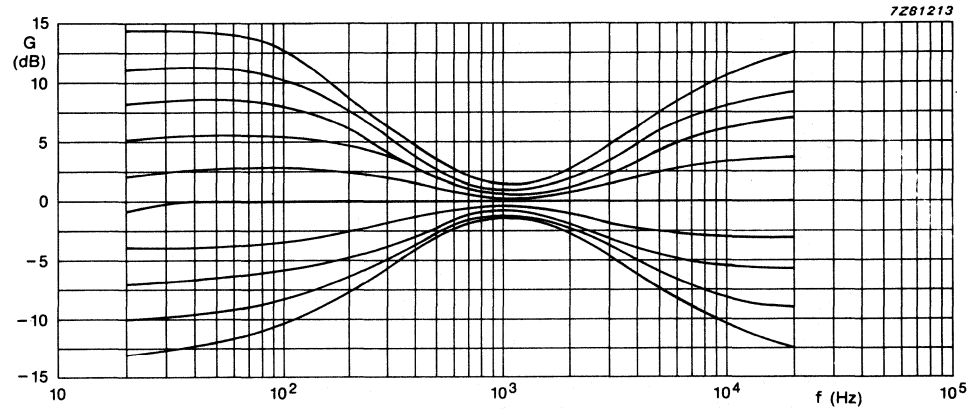


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

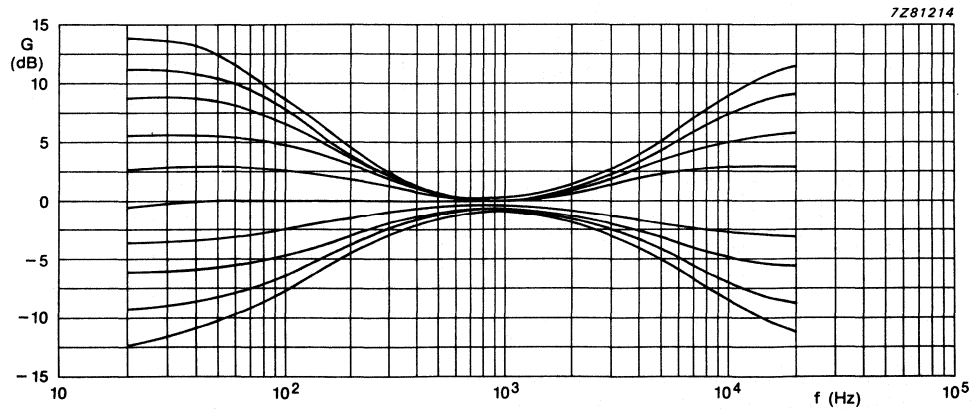
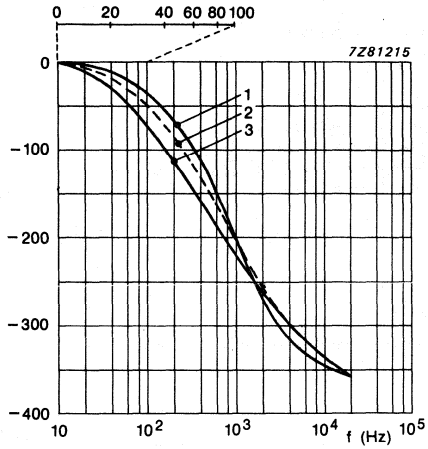


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	C_{24} (nF)	C_{25} (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

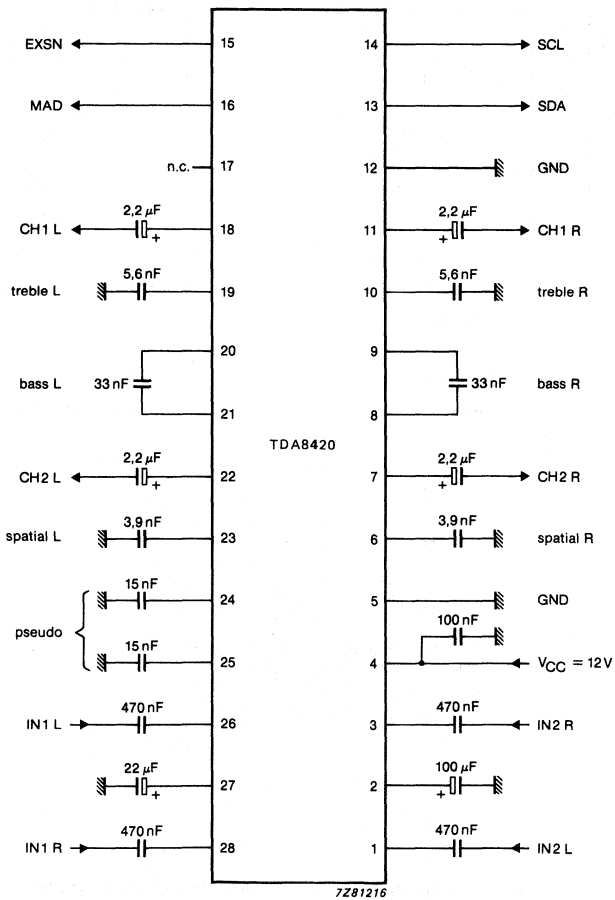
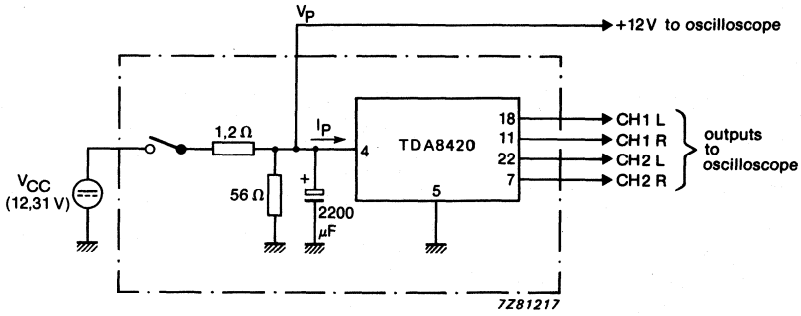


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

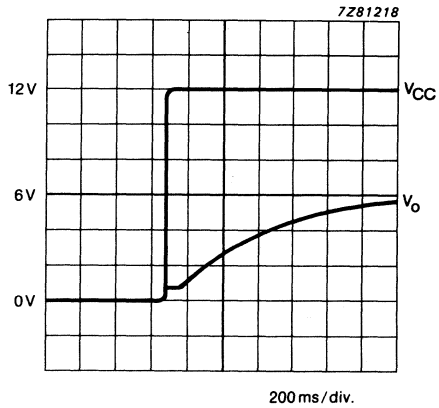


Fig. 18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

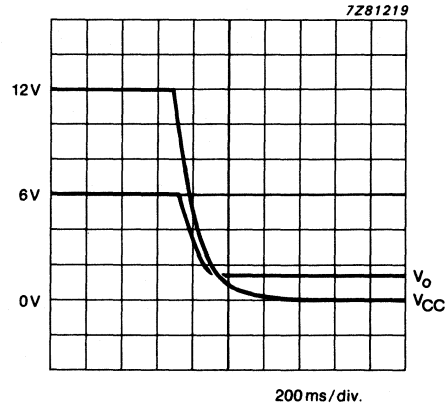


Fig. 19 Turn-off behaviour;
without modulation.

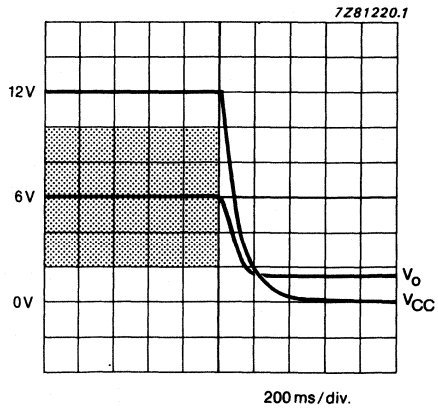


Fig. 20 Turn-off behaviour; with modulation (shaded area).

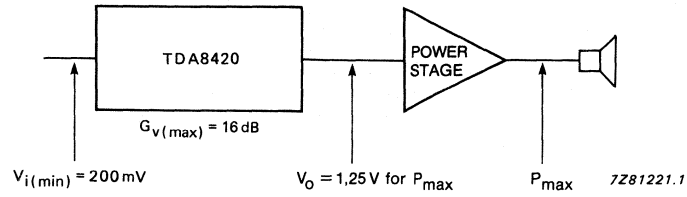


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

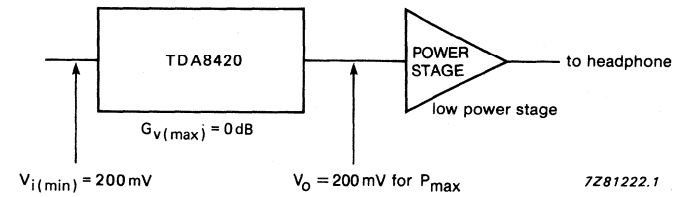


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8421 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control
- Electrostatic discharge protection diodes

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	−62	–	16	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB
Volume control range CH2	G	−62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

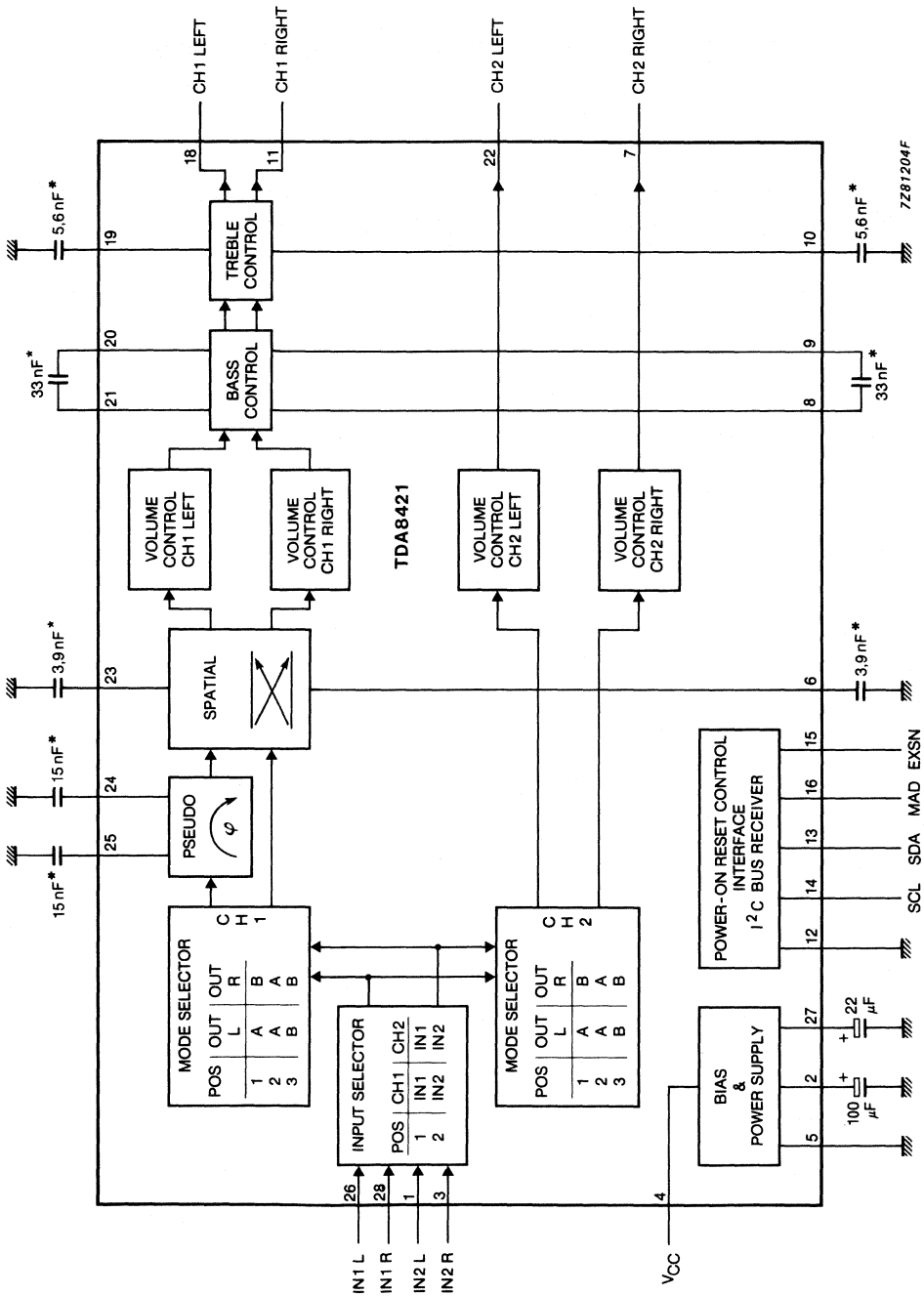


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

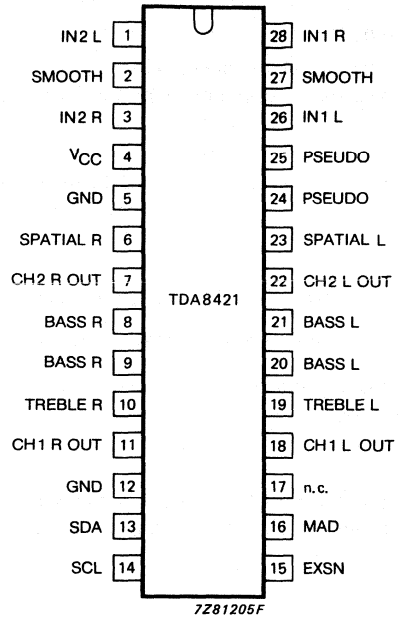


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8421 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8421 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8421 starts with the module address MAD.

MSB								LSB
1	0	0	0	0	0	MAD	R/W	ACK

Fig. 3 TDA8421 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8421s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8421. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8421. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
CH1	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
CH2	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Where: POR = Power-On Reset.

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
16	0	1	1	1	1	1	1
14	−2	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
−46	−62	1	0	0	0	0	0
−48	⩽−90	0	1	1	1	1	1
.	.	.	.	.	.	.	.
−62	⩽−90	0	1	1	0	0	0
⩽−90	⩽−90	0	1	0	1	1	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
⩽−90	⩽−90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation ⩾ 90 dB

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

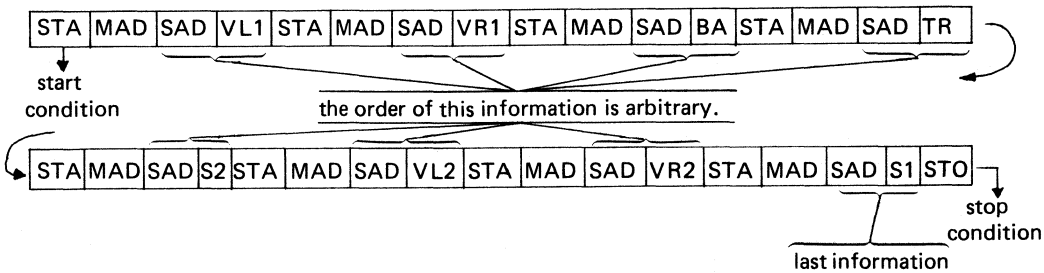


Fig. 4 Data transmission after a power-on reset.

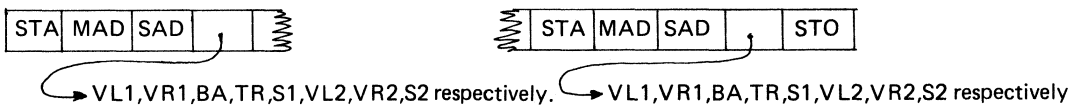


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range at pins for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Voltage range at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I, V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	−25	150	°C
Electrostatic handling *	$\pm V_{ESD}$	–	2000	V

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ resistor.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Internal input voltage IN1 L,R (pins 26,28) IN2 L,R (pins 1,3) DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage at CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
pins with external capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15) at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = −4 dB; THD ≤ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = $\leqslant$ –90 dB	V_n	–	15	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to –30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = + 2 dB to –30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = –4 dB to –30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–62 dB step)	G_{min}	–60	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –62 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for C_{10-5}; C_{19-5} = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for C_{8-9}; C_{20-21} = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	50	–	%
Pseudo: Phase shift (see Fig. 15)					

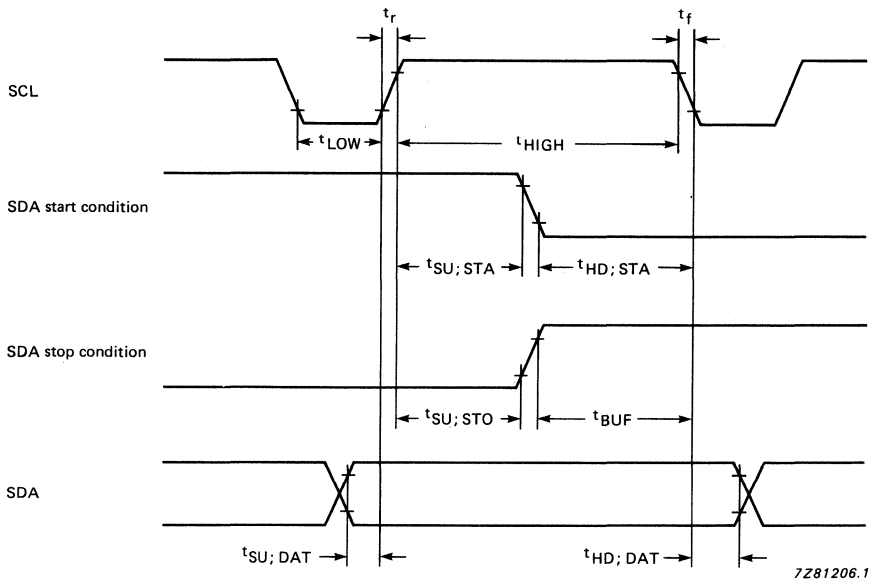
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD ⩽ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = ⩽ −90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz) for $V_{i(rms)}$ = 0,2 V;					
gain = 0 dB to −30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V;					
gain = 0 dB to −30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V					
gain = −4 dB to −30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz					
gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position)					
f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.



$t_{SU;STA}$ = start code set-up time
$t_{HD;STA}$ = start code hold time
$t_{SU;STO}$ = stop code set-up time

t_{BUF} = BUS free time
$t_{SU;DAT}$ = data set-up time
$t_{HD;DAT}$ = DATA hold time

Fig. 6 Timing requirements for I²C bus.

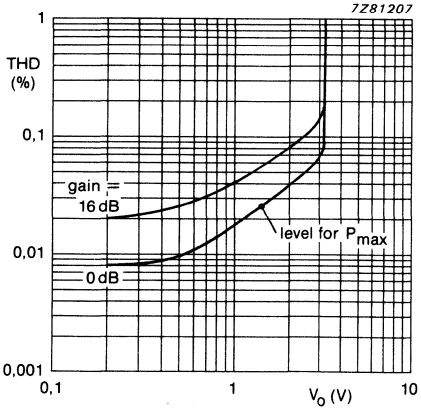


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

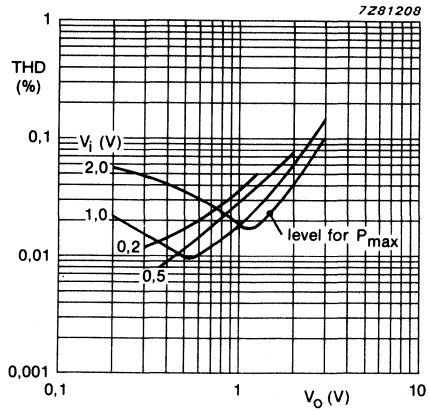


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

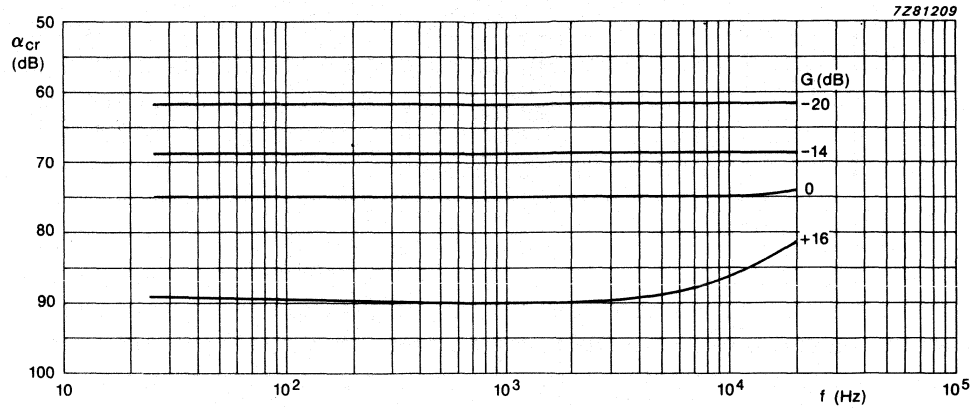


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

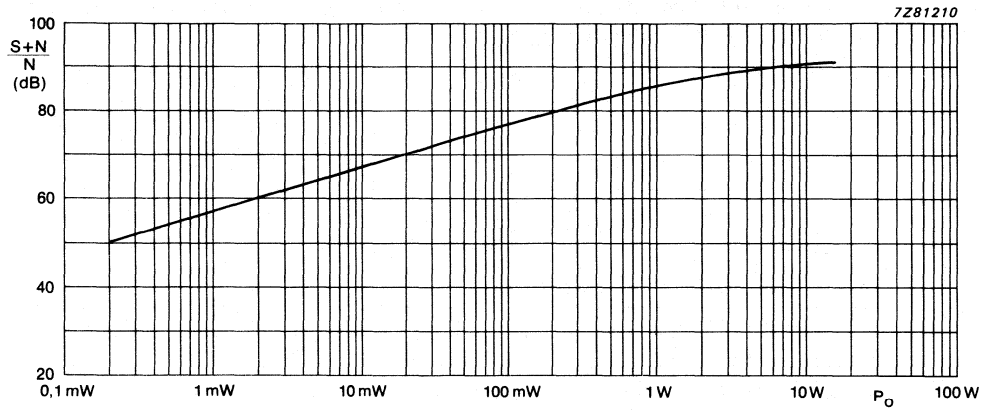


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

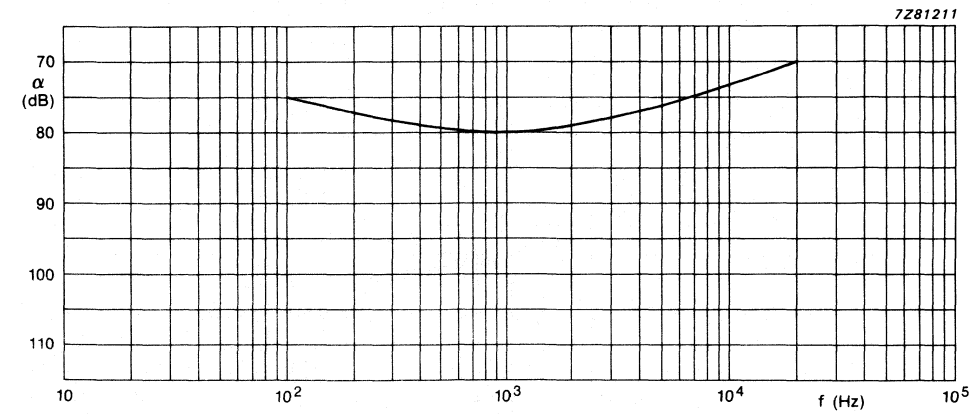


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

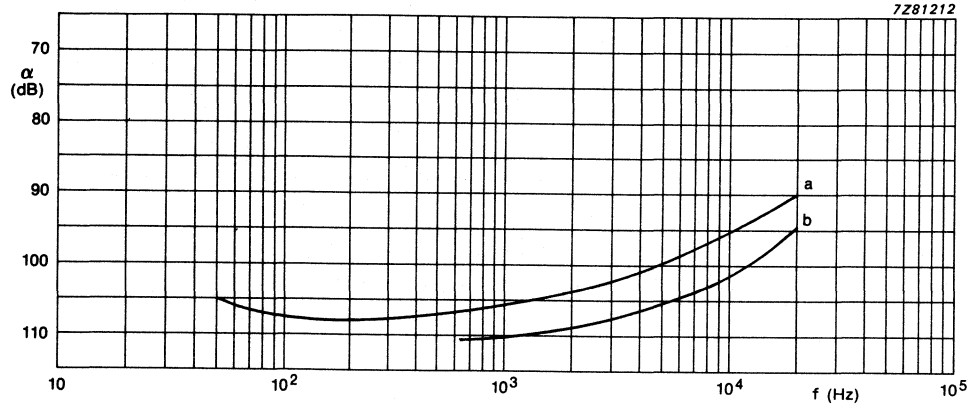


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

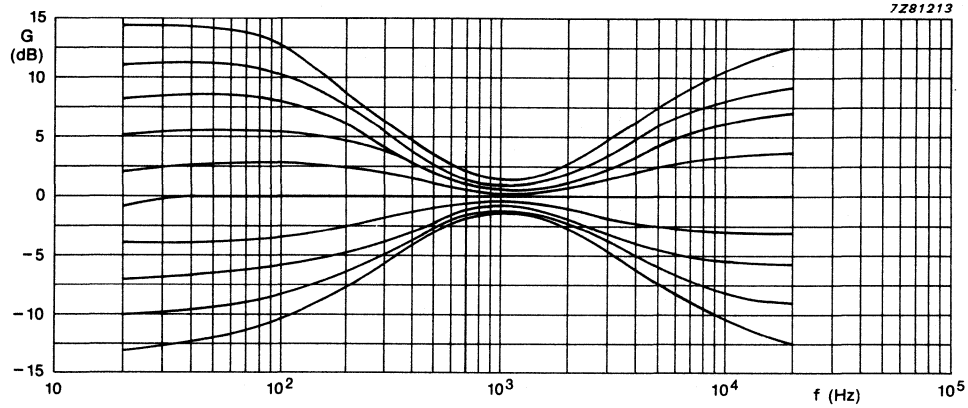


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

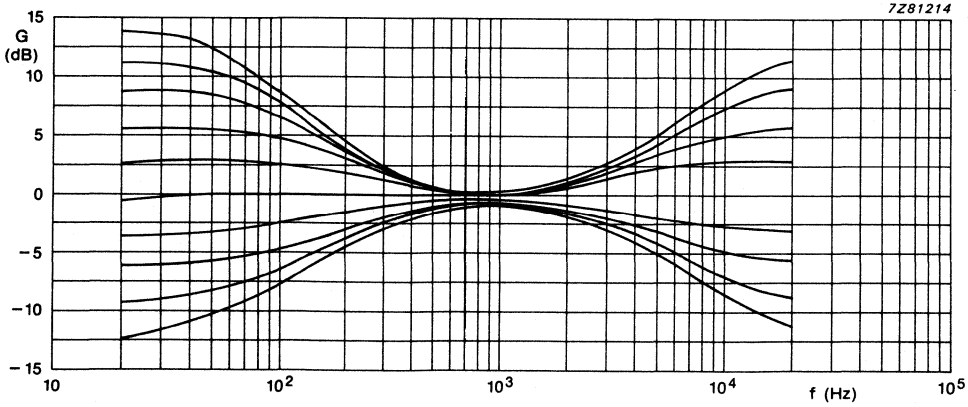
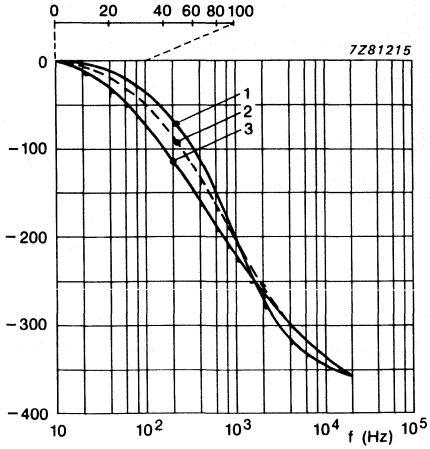


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	pin 24 (nF)	pin 25 (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

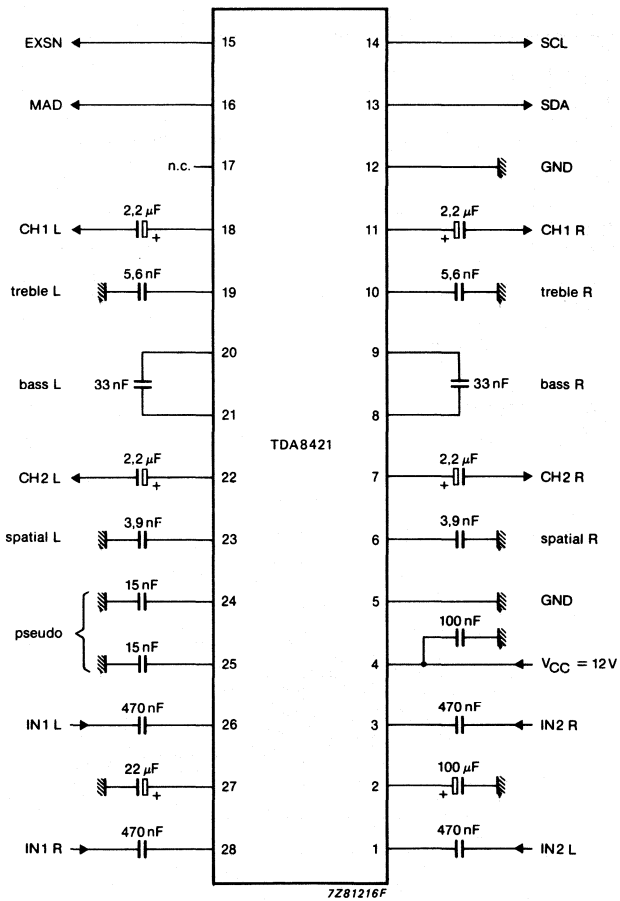
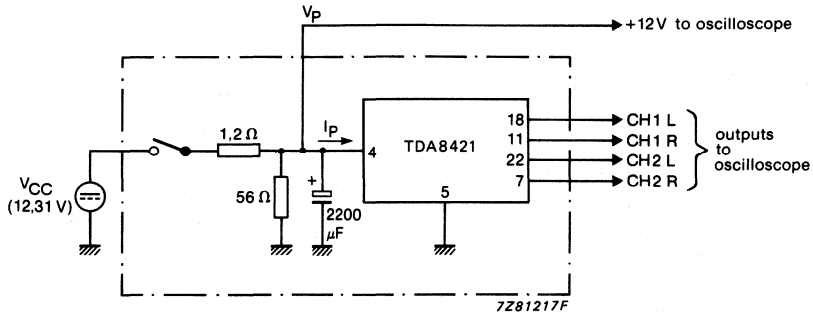


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

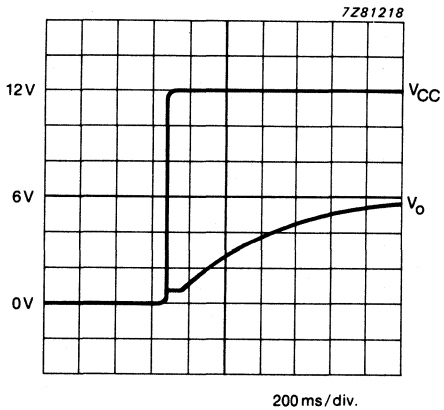


Fig. 18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

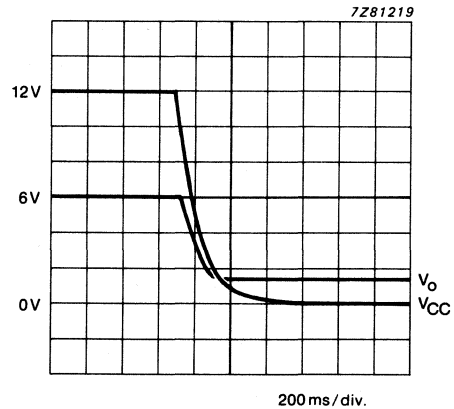


Fig. 19 Turn-off behaviour;
without modulation.

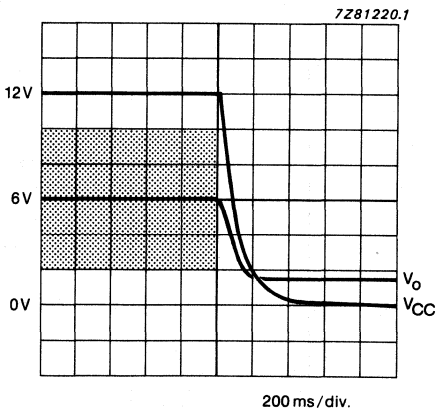


Fig. 20 Turn-off behaviour; with modulation (shaded area).

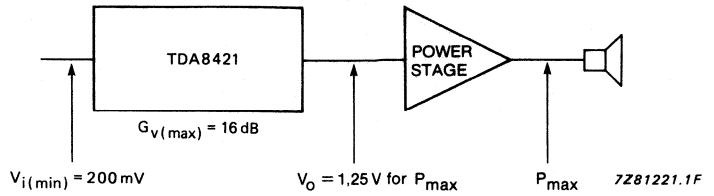


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

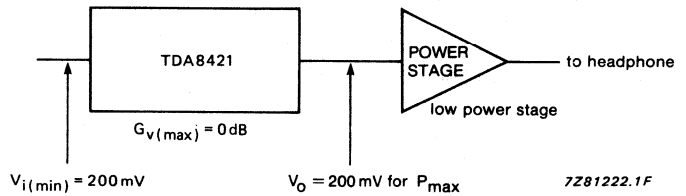


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

HI-FI STEREO AUDIO PROCESSOR; I²C-BUS

GENERAL DESCRIPTION

The TDA8425 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel facility, digitally controlled via the I²C-bus for application in hi-fi audio and television sound.

Features

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	10.8	12.0	13.2	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	–64	–	6	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB

PACKAGE OUTLINE

20-lead dual in-line; plastic (SOT146).

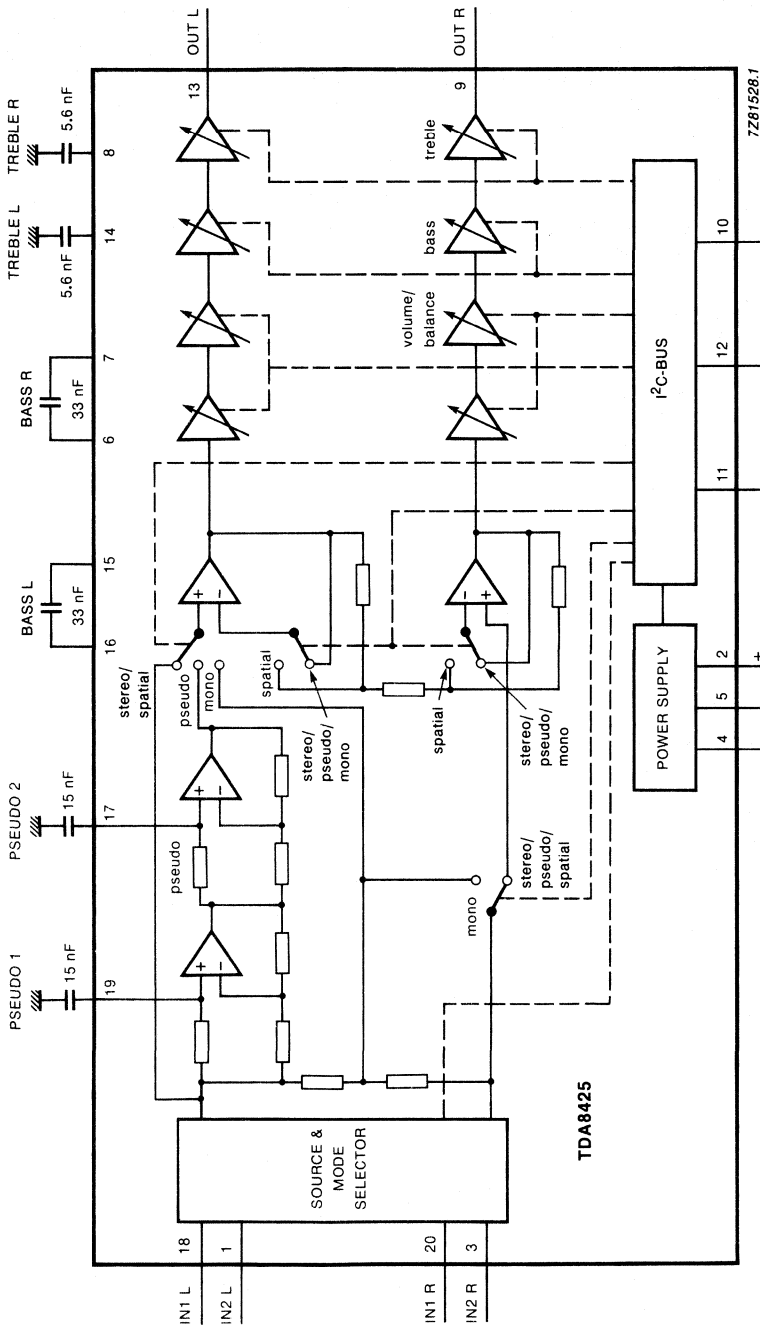


Fig. 1 Block diagram.

PINNING

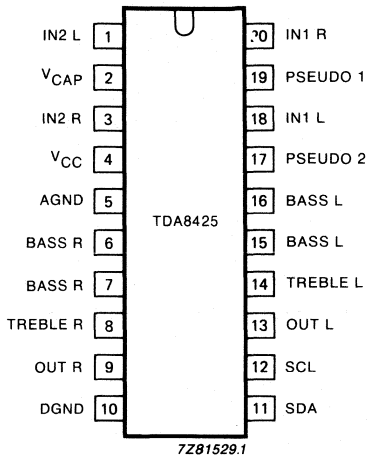


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN1 L (pin 18); IN1 R (pin 20)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and −64 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode*

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

* During forced mono mode the pseudo stereo mode cannot be used.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8425 includes a bias and power supply stage, which generates a voltage of $0.5 \times V_{CC}$ with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I^2C-bus receiver and data handling

Bus specification

The TDA8425 is controlled via the 2-wire I^2C-bus by a microcomputer.
The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8425 starts with the module address MAD.

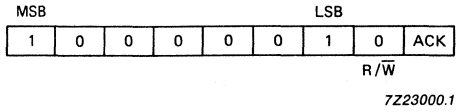


Fig. 3 TDA8425 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8425. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
function	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig. 5).

Definition of 3rd byte

A third byte is used to transmit data to the TDA8425. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

		MSB							LSB
function		7	6	5	4	3	2	1	0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

DEVELOPMENT DATA

Truth tables

Truth tables for the switch functions

Table 3 Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

Table 4 Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono*	0	0

Table 5 Mute

mute	MU
active; automatic after POR	1
not active	0

Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/step (dB)	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
−62	0	1	1	1	0	1
−64	0	1	1	1	0	0
⩽ −80	0	1	1	0	1	1
⩽ −80	0	0	0	0	0	0

* Pseudo stereo function is not possible in this mode.

DEVELOPMENT DATA

Table 7 Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
15	1	0	1	1
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Table 8 Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

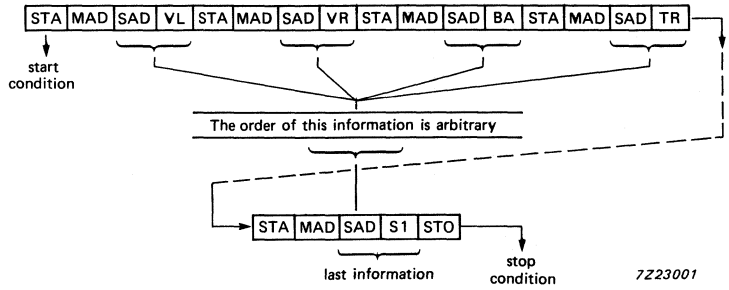


Fig. 4 Data transmission after a power-on reset.

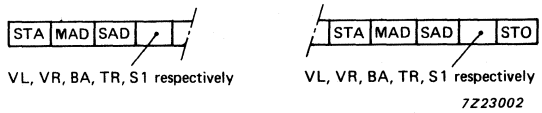


Fig. 5 Data transmission after a power-on reset with auto increment.

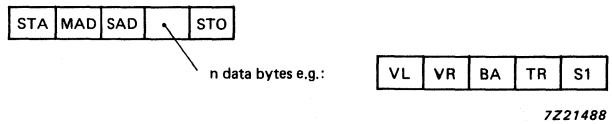


Fig. 6 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for pins with external capacitors	V_{cap}	0	V_{CC}	V
Voltage range for pins 11 and 12	$V_{SDA, SCL}$	0	V_{CC}	V
Voltage range at pins 1, 3, 9, 11, 12, 13, 18 and 20	$V_{I/O}$	0	V_{CC}	V
Output current at pins 9 and 13	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	450	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C
Electrostatic handling, classification A*				

DEVELOPMENT DATA

* Human body model: C = 100 pF, R = 1.5 kΩ and V ⩾ 4 kV; charge device model: C = 200 pF, R = 0 Ω and V ⩾ 500 V.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current					
at V_{CC} = 12 V	I_{CC}	–	26	35	mA
Internal reference voltage	V_{ref}	5.4	0.5 x V_{CC}	6.6	V
Internal voltage at pins 1, 3, 18 and 20 DC voltage internally generated; capacitive coupling recommended	V_I	–	V_{REF}	–	V
Internal voltage at pins 9 and 13	V_O	–	V_{REF}	–	V
SDA; SCL (pins 11 and 12)					
input voltage HIGH	V_{IH}	3.0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0.3	–	1.5	V
input current HIGH	I_{IH}	–	–	+ 10	μA
input current LOW	I_{IL}	−10	–	–	μA
Output voltage at pins with external capacitors					
pins 6 to 8, 14 to 17, 19	$V_{cap.n}$	–	V_{REF}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0.3	–	V

DEVELOPMENT DATA

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 1000\ pF$; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 7)					
SDA, SCL (pin 11 and 12)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4.7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0.3	μs
Set-up time for start condition	$t_{SU;STA}$	4.7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4.7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
INPUTS					
IN1 L (pin 18) IN1 R (pin 20); IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (RMS value) at V_u = −12 dB; THD ⩽ 0.5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_i	20	30	40	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz
OUTPUTS					
OUT R (pin 9); OUT L (pin 13)					
Output voltage range (rms value) at THD ⩽ 0.7%; $V_{i(max)} \leqslant 2$ V	$V_{o(rms)}$	0.6	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Signal plus noise-to-noise ratio (weighted according to CCIR 468-2); V_o = 600 mV					
gain = 6 dB	(S+N)/N	–	78	–	dB
gain = 0 dB	(S+N)/N	–	86	–	dB
gain = ⩽ −20 dB	(S+N)/N	–	68	–	dB

AC CHARACTERISTICS (continued)

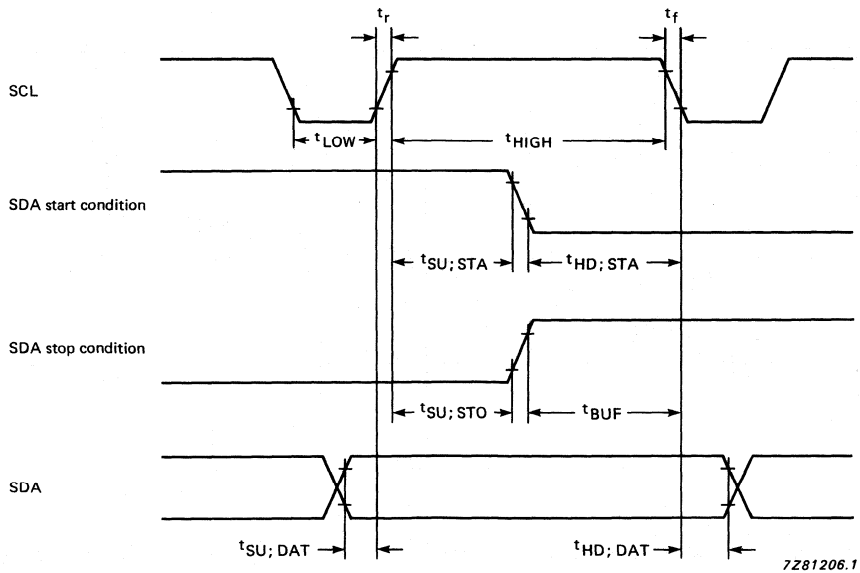
parameter	symbol	min.	typ.	max.	unit
OUTPUTS (continued)					
Crosstalk between inputs at gain = 0 dB; 1 kHz; opposite inputs grounded (50 Ω); IN1L (pin 18) to IN2L (pin 1) or IN1R (pin 20) to IN2R (pin 3)	α_{cr}	–	100	–	dB
Total harmonic distortion (f = 20 Hz to 12.5 kHz)					
for $V_{i(rms)}$ = 0.3 V; gain = + 6 dB to –40 dB	THD	–	0.05	–	%
for $V_{i(rms)}$ = 0.6 V; gain = 0 dB to –40 dB	THD	–	0.07	0.4	%
for $V_{i(rms)}$ = 2.0 V; gain = –12 dB to –40 dB	THD	–	0.1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cs}	–	80	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	100	–	dB
VOLUME CONTROL					
For truth table see Table 6					
Control range at f = 1 kHz (36 steps)					
maximum voltage gain (6 dB step)	G_{max}	5	6	–	dB
minimum voltage gain (–64 dB step)	G_{min}	–63	–64	–	dB
mute position	G_{mute}	–80	–90	–	dB
Gain tracking error; balance in mid-position	G	–	–	2	dB
Step resolution					
gain from 6 dB to –40 dB	G_{step}	1.5	2.0	2.5	dB/step
gain from –42 dB to –64 dB	G_{step}	1.0	2.0	3.0	dB/step
TREBLE CONTROL					
For truth table see Table 8					
Control range for $C_{8\text{-}5}$; $C_{14\text{-}5}$ = 5.6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step

parameter	symbol	min.	typ.	max.	unit
BASS CONTROL					
For truth table see Table 7					
Control range for C_{6-7}; C_{15-16} = 33 nF					
Maximum emphasis at 40 Hz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 Hz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	52	–	%
Pseudo: Phase shift (see Fig. 8)					

Note to the AC characteristics

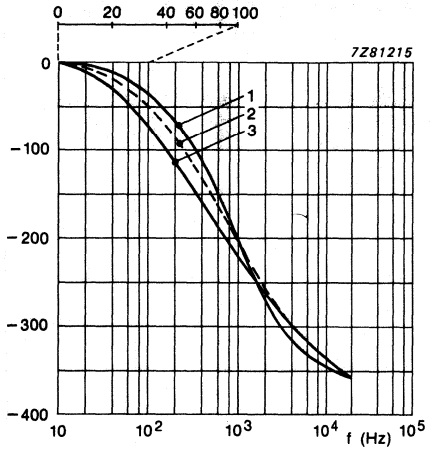
1. Balance is realized via software by different volume settings in both channels (left and right).

DEVELOPMENT DATA



$t_{SU;STA}$ = start code set-up time.
$t_{HD;STA}$ = start code hold time.
$t_{SU;STO}$ = stop code set-up time.
t_{BUF} = bus free time.
$t_{SU;DAT}$ = data set-up time.
$t_{HD;DAT}$ = data hold time.

Fig. 7 Timing requirements for I²C-bus.



curve	pin 17 (nF)	pin 19 (nF)	effect
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

Fig. 8 Pseudo (phase in degrees) as a function of frequency (left output).

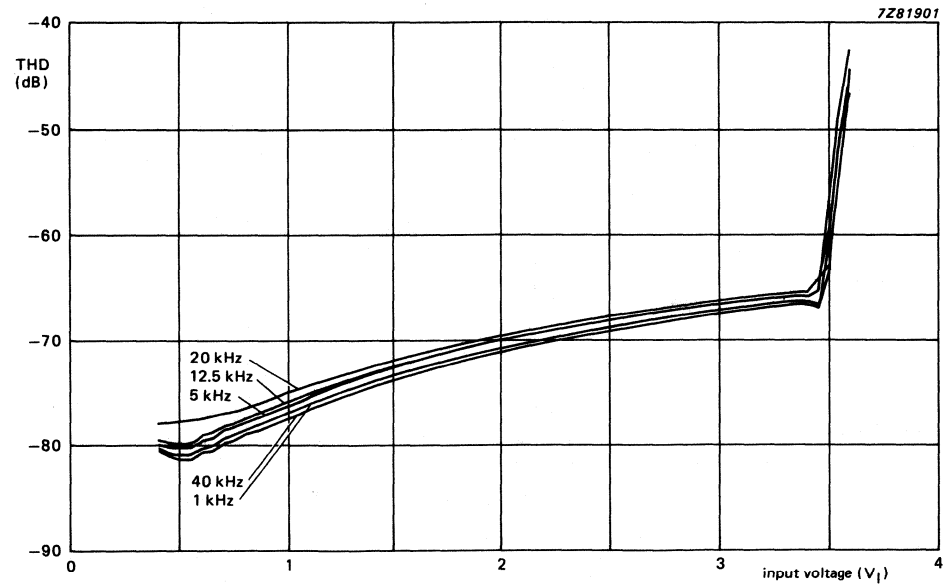


Fig. 9 Input signal handling capability; gain = −10 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

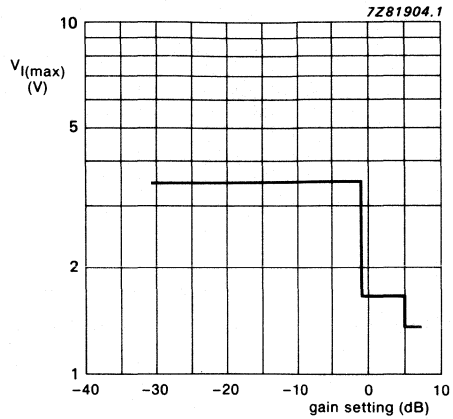


Fig. 10 Input signal handling capacility plotted against gain setting; THD = −60 dB; f = 1 kHz; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

DEVELOPMENT DATA

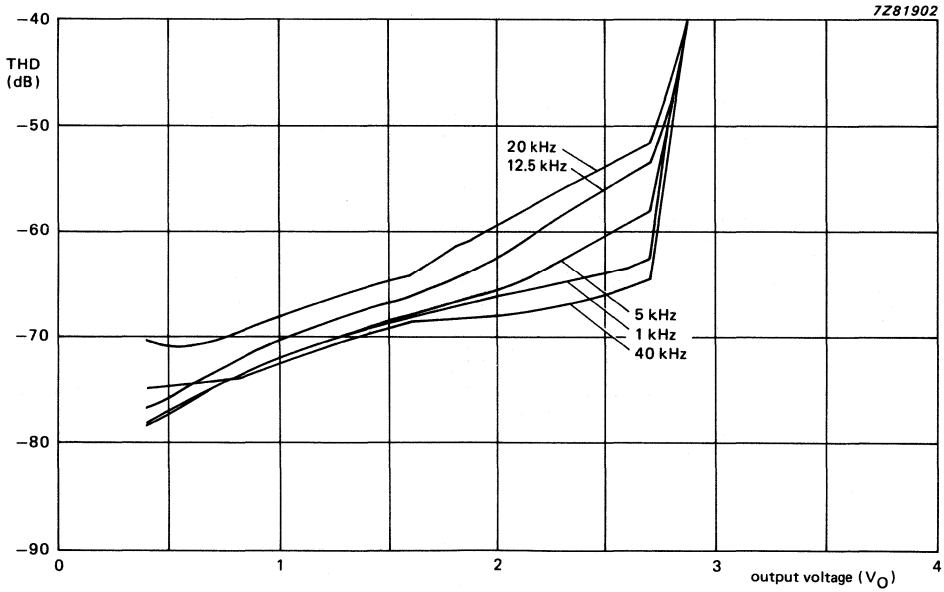


Fig. 11 Output signal handling capability; gain = 6 dB; R_S = 600 Ω; R_L = 10 kΩ, bass/trebble = 0 dB, V_{CC} = 12 V.

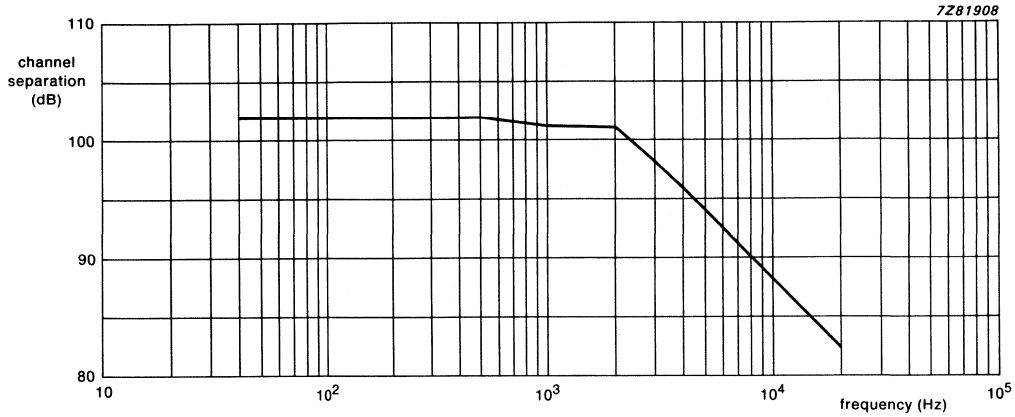
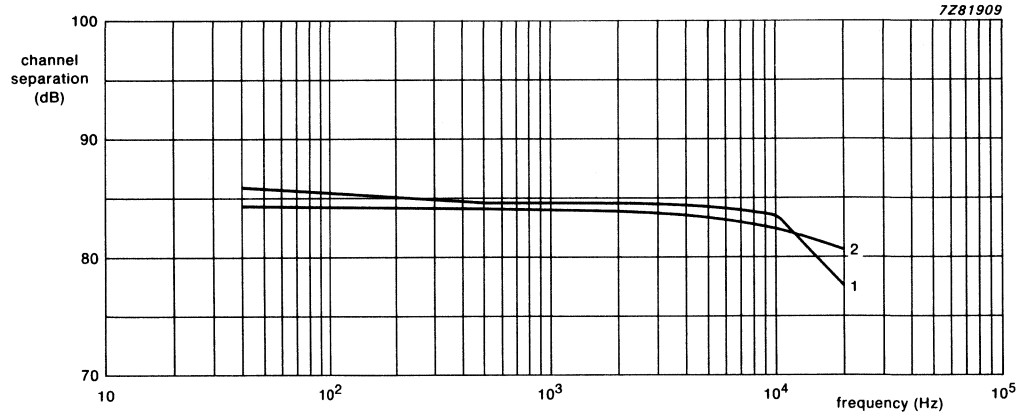


Fig. 12 Source selector separation (channel 2 and channel 1); gain = 0 dB; V_{i1} = 0 V; V_{i2} = 1 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.



(1) gain = 0 dB; V_i = 1.0 V.
(2) gain = 6 dB; V_i = 0.5 V.

Fig. 13 Stereo channel separation as a function of frequency; R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

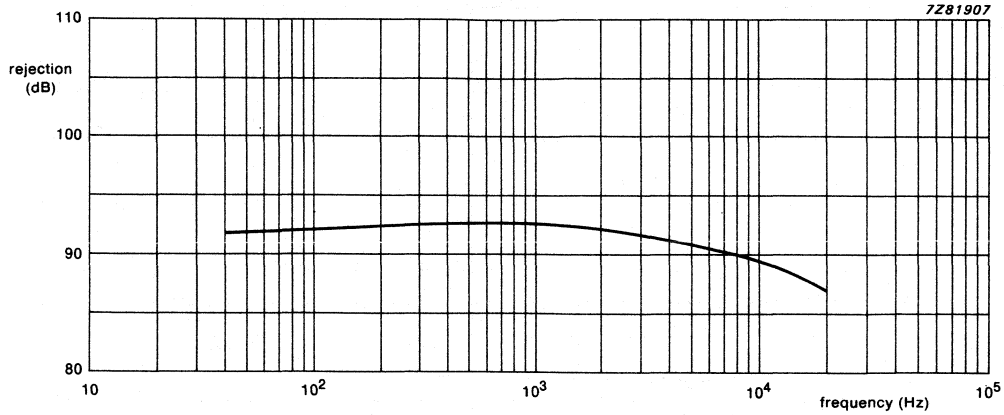


Fig. 14 Mute signal rejection as a function of frequency; gain = 0 dB; V_i = 1.0 V; R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

DEVELOPMENT DATA

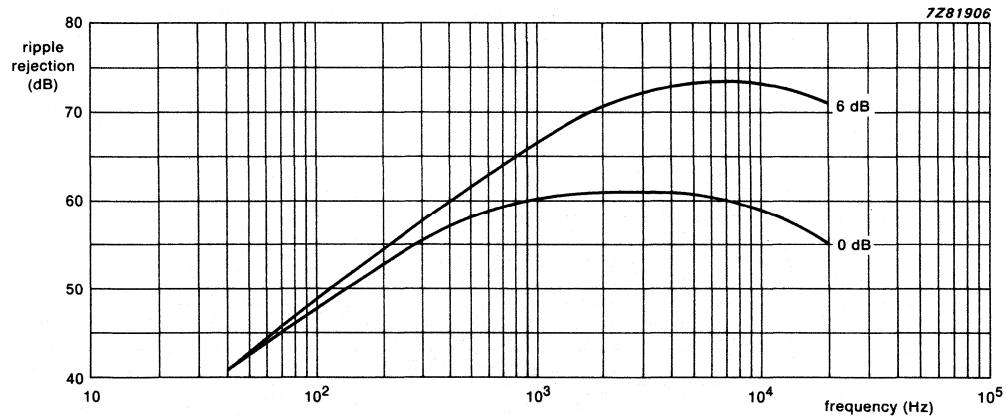


Fig. 15 Ripple rejection as a function of frequency; voltage ripple = 0.3 V (rms); R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

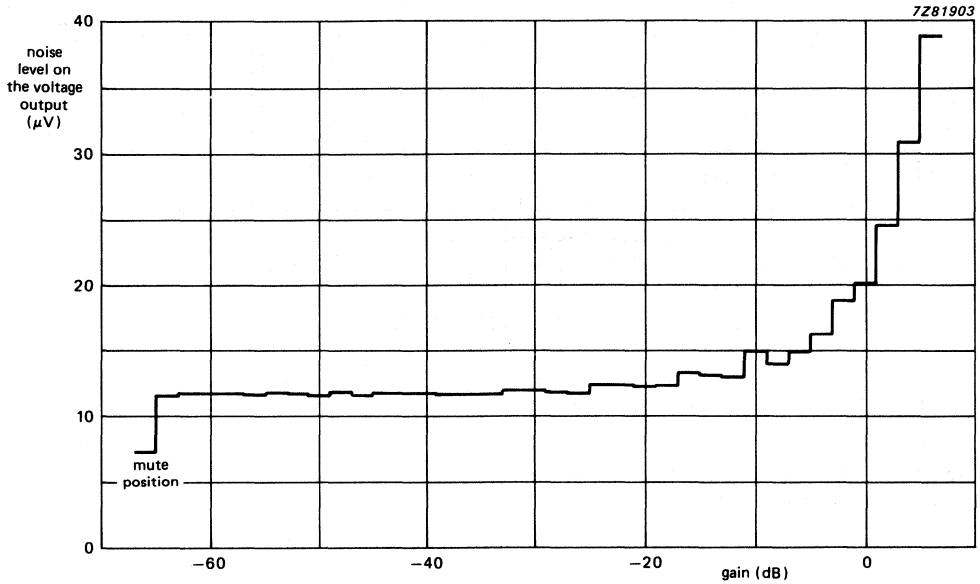


Fig. 16 Noise output voltage as a function of gain; weighted CCIR468 quasi peak gain, + 6 dB to −64 dB; V_i = 0 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

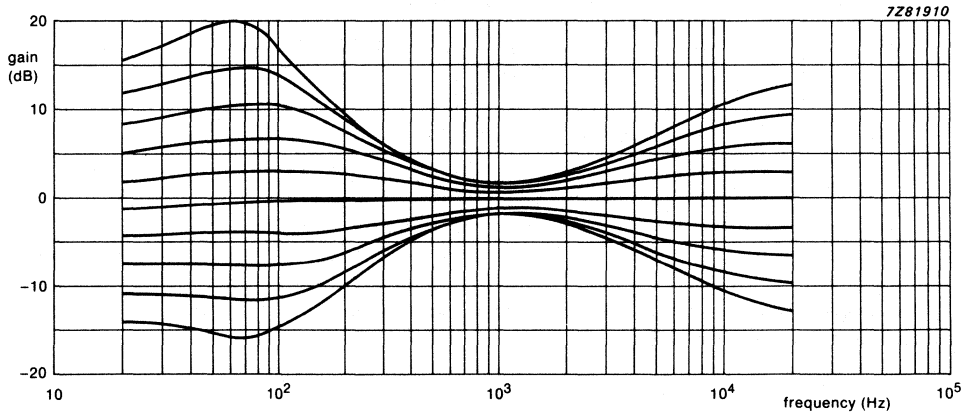


Fig. 17 Frequency response of bass and trebble control; bass and trebble gain settings = −12 to + 15 dB; gain is 0 dB; V_i = 0.1 V; R_{S9} = 600 Ω; R_L = 10 kΩ; V_{CC} = 12 V.

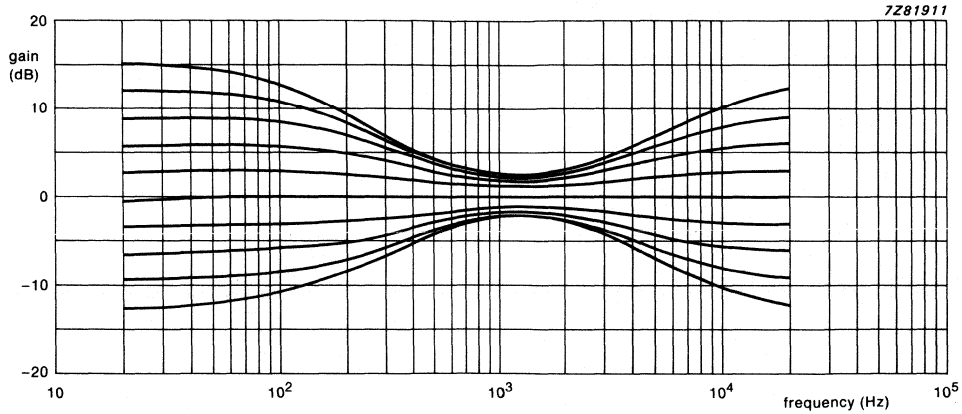


Fig. 18 Tone control with T-filter.

DEVELOPMENT DATA

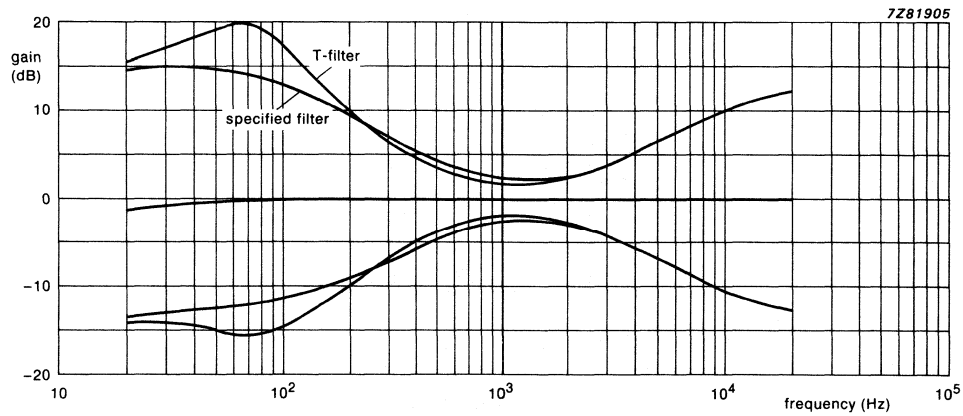


Fig. 19 Tone control.

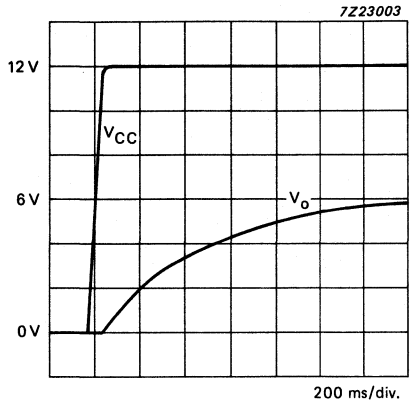


Fig. 20 Turn-on behaviour;
$C = 2.2\ \mu F$; $R_L = 10\ k\Omega$.

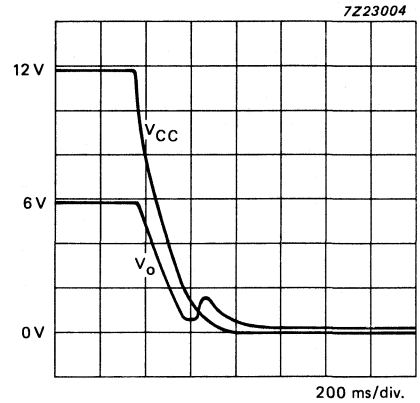


Fig. 21 Turn-off behaviour;
without modulation.

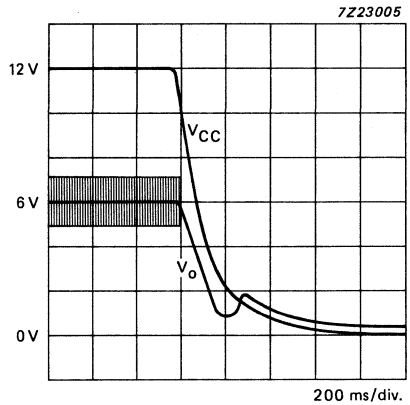
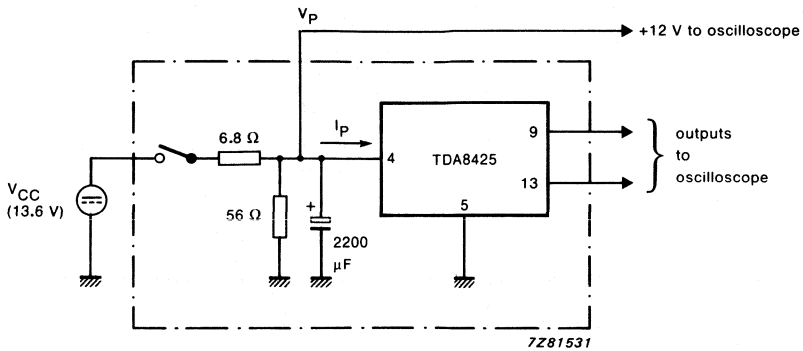


Fig. 22 Turn-off behaviour; with modulation (shaded area).



I_{CC} = 25 mA
I_{load} = 239 mA
t_{on} = 15 ms
t_{off} = 110 ms

Fig. 23 Turn-on/off power supply circuit diagram.

DEVELOPMENT DATA

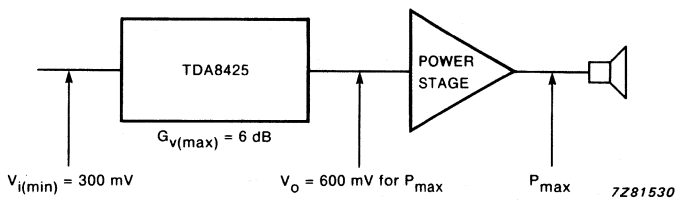


Fig. 24 Level diagram.

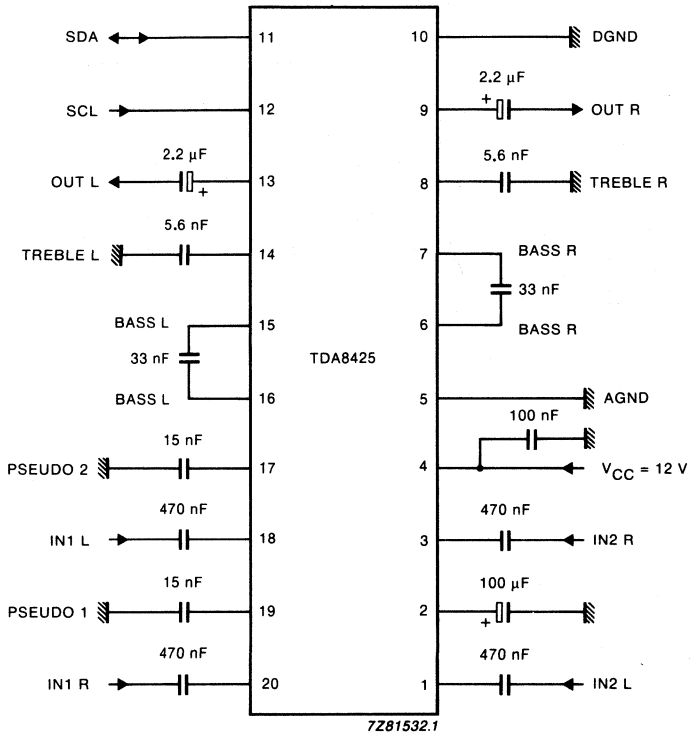


Fig. 25 Test and application circuit diagram.

SWITCH FOR CTV RECEIVERS

GENERAL DESCRIPTION

The TDA8440 is a versatile video/audio switch, intended to be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

It provides two 3-state switches for audio channels and one 3-state switch for the video channel and a video amplifier with selectable gain (times 1 or times 2).

The integrated circuit can be used in conjunction with a microcontroller from the MAB8400 family, and is controlled via a bidirectional I²C bus. Sufficient sub-addressing is provided for the I²C bus mode. It can also be controlled directly by d.c. switching signals.

Features

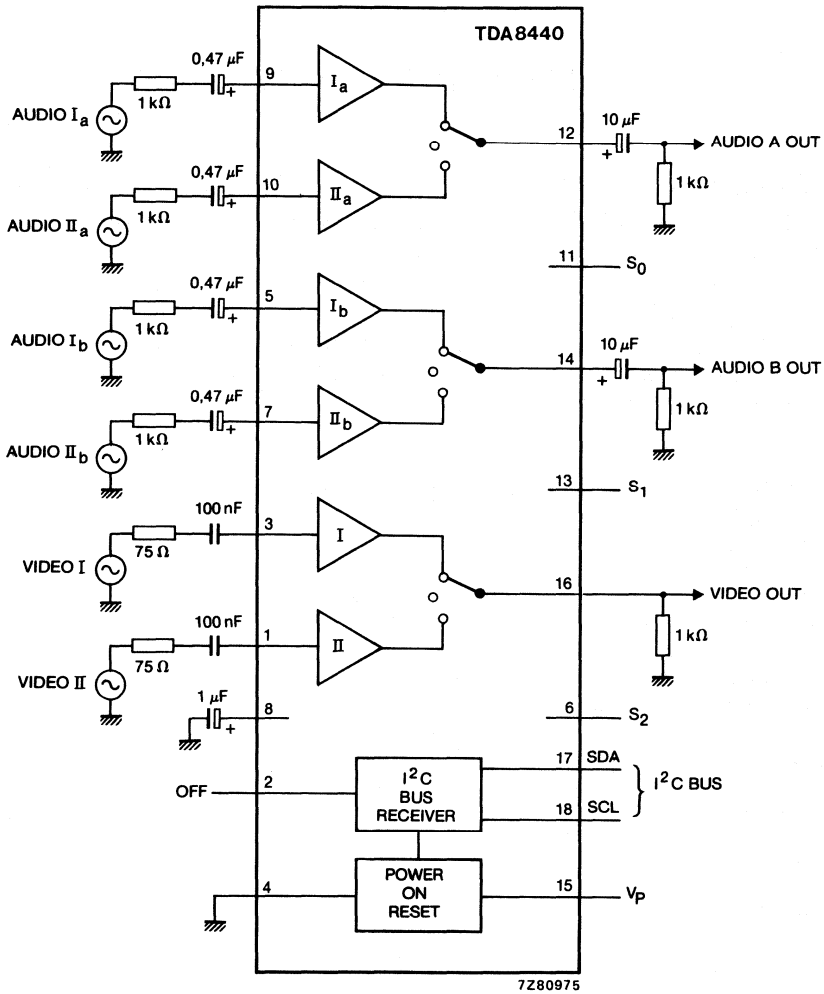
- Combined analogue and digital circuitry gives maximum flexibility in channel switching
- 3-state switches for all channels
- Selectable gain for the video channels
- Sub-addressing facility
- I²C bus or non-I²C bus mode (controlled by d.c. voltages)
- Slave receiver in the I²C bus mode
- External OFF command
- System expansion possible up to 7 devices (14 sources)
- Static short-circuit proof outputs

QUICK REFERENCE DATA

Supply voltage range	V_{15-4}	10 to 13,2	V
Supply current (without load)	I_{15}	typ. 33 max. 50	mA mA
Storage temperature	T_{stg}	max. + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



S0, S1, S2 and OFF (pins 11, 13, 6 and 2) connected to V_P or GND.
If more than 1 device is used, then the outputs and the pins 8 (bias decoupling of the audio inputs) mau may be connected in parallel.

Fig. 1 Block diagram and test circuit.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA8440 is a monolithic system of switches and can be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

The IC incorporates 3-state switches they comprise:

a) An electronic video switch with selectable gain (times 1 or times 2) for switching between an internal video signal (from the IF amplifier) and an AUXILIARY input signal.

b) Two electronic audio switches, for two sound channels (stereo or dual language), for switching between internal audio sources and signals from the AUXILIARY VIDEO/AUDIO plug.

A selection can be made between two input signals and an OFF-state. The OFF-state is necessary if more than one TDA8440 device is used.

The SDA and SCL pins can be connected to the I²C bus or to d.c. switching voltages. Inputs S_0 (pin 11), S_1 (pin 13), and S_2 (pin 6) are used for selection of sub-addresses or switching to the non-I²C mode. Inputs S_0, S_1 and S_2 can be connected to the supply voltage (H) or to ground (L). In this way no peripheral components are required for selection.

Table 1 Sub-addressing

			sub-address		
S_2	S_1	S_0	A_2	A_1	A_0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I²C addressable		

NON-I²C BUS CONTROL

If the TDA8440 switching device has to be operated via the AUXILIARY VIDEO/AUDIO plug, inputs S_2, S_1 and S_0 must be connected to the supply line (12 V).

The sources (internal and external) and the gain of the video amplifier can be selected via the SDA and SCL pins with the switching voltage from the AUXILIARY VIDEO/AUDIO plug:

- Sources I are selected if SDA = 12 V (external source)
- Sources II are selected if SDA = 0 V (TV mode)
- Video amplifier gain is 2 x if SCL = 12 V (external source)
- Video amplifier gain is 1 x if SCL = 0 V (TV mode)

If more than one TDA8440 device is used in the non-I²C bus system, the OFF pin can be used to switch off the desired devices. This can be done via the 12 V switching voltage on the AUXILIARY VIDEO/AUDIO plug.

- All switches are in the OFF position if OFF = H (12 V)
- All switches are in the selected position via SDA and SCL pins if OFF = L (0 V)

I²C BUS CONTROL

Detailed information on the I²C bus is available on request.

Table 2 TDA8440 I²C bus protocol.

STA	A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W	AC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	AC	STO

STA = start condition
A_6 = 1
A_5 = 0
A_4 = 0
A_3 = 1
} Fixed address bits
A_2 = sub-address bit, fixed via S_2 input
A_1 = sub-address bit, fixed via S_1 input
A_0 = sub-address bit, fixed via S_0 input
R/W = read/write bit (has to be 0, only write mode allowed)
AC = acknowledge bit (= 0) generated by the TDA8440
D_7 = 1 audio Ia is selected to audio output a
D_7 = 0 audio Ia is not selected
D_6 = 1 audio IIa is selected to audio output a
D_6 = 0 audio IIa is not selected
D_5 = 1 audio Ib is selected to audio output b
D_5 = 0 audio Ib output is not selected
D_4 = 1 audio IIb is selected to audio output b
D_4 = 0 audio IIb is not selected
D_3 = 1 video I is selected to video output
D_3 = 0 video I is not selected
D_2 = 1 video II is selected to video output
D_2 = 0 video II is not selected
D_1 = 1 video amplifier gain is times 2
D_1 = 0 video amplifier gain is times 1
D_0 = 1 OFF-input inactive
D_0 = 0 OFF-input active
STO = stop condition

OFF FUNCTION

With the OFF input all outputs can be switched off (mode high ohmic), depending on the value of D_0.

D_0/OFF gating

D_0	OFF input	Outputs
0 (off input active)	H	OFF
0	L	in accordance with last defined D_7-D_1 (may be entered while OFF = HIGH)
1 (off input inactive)	H	in accordance with D_7-D_1
1	L	in accordance with D_7-D_1

Power-on reset

The circuit is provided with a power-on reset function.

When the power supply is switched on an internal pulse will be generated that will reset the internal memory S_0, in the initial state all the switches will be in the off position and the OFF input is active (D_7-D_0 = 0) (I^2C mode), position defined via SDA and SCL inputs (non-I^2C mode).

When the power supply decreases below 5 V a pulse will be generated and the internal memory will be reset. The behaviour of the switches will be the same as described above.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	typ.	max.	unit
Supply voltage	pin 15 V_P	–	–	14	V
Input voltage range	pin 17 V_{SDA}	−0,3	–	V_P + 0,3	V
	pin 18 V_{SCL}	−0,3	–	V_P + 0,3	V
	pin 2 V_{OFF}	−0,3	–	V_P + 0,3	V
	pin 11 V_{S0}	−0,3	–	V_P + 0,3	V
	pin 13 V_{S1}	−0,3	–	V_P + 0,3	V
	pin 6 V_{S2}	−0,3	–	V_P + 0,3	V
Video output current	pin 16 $-I_{16}$	–	–	50	mA
Storage temperature range	T_{stg}	–	–	+ 125	°C
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Junction temperature	T_j	–	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	50	K/W

DEVELOPMENT DATA

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{15-4}	10	–	13,2	V
Supply current (without load)	I_{15}	–	37	50	mA
Video switch					
Input coupling capacitor	C_1C_3	100	–	–	nF
Voltage gain (times 1; SLC = L)	A_{3-16}	−1	0	+ 1	dB
(times 2; SCL = H)	A_{3-16}	+5	+ 6	+ 7	dB
Voltage gain (times 1; SCL = L)	A_{1-16}	−1	0	+ 1	dB
(times 2; SCL = H)	A_{1-16}	+5	+ 6	+ 7	dB
Input video signal amplitude (gain times 1)	V_{3-4}	–	–	4,5	V
Input video signal amplitude (gain times 1)	V_{1-4}	–	–	4,5	V
Output impedance	Z_{16-4}	–	7	–	Ω
Output impedance in 'OFF' state	Z_{16-4}	100	–	–	kΩ
Isolation (off state) (f_o = 5 MHz)		60	–	–	dB
Signal-to-noise ratio (note 2)	S/S + N	60	–	–	dB
Output top-sync level	V_{16-4}	2,4	2,8	3,2	V
Differential gain	G	–	–	3	%
Minimum crosstalk attenuation (note 1)	V_{16-4}	60	–	–	dB
Supply voltage rejection (note 3)	RR	36	–	–	dB
Bandwidth (1 dB)	B	10	–	–	MHz
Crosstalk attenuation for interference caused by bus signals (source impedance 75 Ω)	α	60	–	–	dB
Audio switch a and b					
Input signal level	$V_{9-4(rms)}$	–	–	2	V
	$V_{10-4(rms)}$	–	–	2	V
	$V_{5-4(rms)}$	–	–	2	V
	$V_{7-4(rms)}$	–	–	2	V
Input impedance	Z_{9-4}	50	100	–	kΩ
	Z_{10-4}	50	100	–	kΩ
	Z_{5-4}	50	100	–	kΩ
	Z_{7-4}	50	100	–	kΩ
Output impedance	Z_{12-4}	–	–	10	Ω
	Z_{14-4}	–	–	10	Ω
Output impedance (off state)	Z_{14-4}	100	–	–	kΩ

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Voltage gain	$V_{9\text{-}12}$	−1	0	+ 1	dB
	$V_{10\text{-}12}$	−1	0	+ 1	dB
	$V_{5\text{-}14}$	−1	0	+ 1	dB
	$V_{7\text{-}14}$	−1	0	+ 1	dB
Isolation (off state) (f = 20 kHz)		90	–	–	dB
Signal-to-noise ratio (note 4)	S/S + N	90	–	–	dB
Total harmonic distortion (note 6)	THD	–	–	0,1	%
Crosstalk attenuation for interferences caused by video signals (note 5)					
Weighted	α	80	–	–	dB
Unweighted	α	80	–	–	dB
Crosstalk attenuation for interferences caused by sinusoidal sound signals (note 5)	α	80	–	–	dB
Crosstalk attenuation for interferences caused by the bus signal (weighted) (source impedance = 1 kΩ)		80	–	–	dB
Supply voltage rejection	RR	50	–	–	dB
Bandwidth (−1 dB)	B	50	–	–	kHz
I^2C bus inputs/outputs SDA (pin 17) and SCL (pin 18)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current HIGH*	I_{IH}	–	–	10	μA
Input current LOW*	I_{IL}	–	–	10	μA
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Capacitance of SDA and SDL inputs, pins 17 and 18	C_I	–	–	10	pF
Sub-address inputs S_0 (pin 11), S_1 (pin 13), S_2 (pin 6)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	I_{IL}	−50	–	0	μA
OFF input (pin 2)					
Input voltage HIGH	V_{IH}	+3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	20	μA
Input current LOW	I_{IL}	−10	–	2	μA

* Also if the supply is switched off.

CHARACTERISTICS (continued)

I^2C bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{s(STA)}$	4	–	–	μs
Start condition hold time	$t_{h(STA)}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL, HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_r	–	–	1	μs
SCL, SDA fall time	t_f	–	–	0,3	μs
Data set-up time (write)	$t_{s(DAT)}$	1	–	–	μs
Data hold time (write)	$t_{h(DAT)}$	1	–	–	μs
Acknowledge (from TDA8440) set-up time	$t_{s(CAC)}$	–	–	2	μs
Acknowledge (from TDA8440) hold time	$t_{h(CAC)}$	0	–	–	μs
Stop condition set-up time	$t_{s(STO)}$	4	–	–	μs

Notes to the characteristics

1. Caused by drive on any other input at maximum level, measured in B = 5 MHz, source impedance for the used input 75 Ω,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{IN\ max}}.$$

2. $$S/N = 20 \log \frac{V_O \text{ video noise (p-p) (2 V)}}{V_O \text{ noise rms B = 5 MHz}}.$$

3. $$\text{Supply voltage ripple rejection} = 20 \log \frac{V_r \text{ supply}}{V_r \text{ on output}} \text{ at f = max. 100 kHz.}$$

4. $$S/N = 20 \log \frac{V_O \text{ nominal (0,5 V)}}{V_O \text{ noise B = 20 kHz}}.$$

5. Caused by drive of any other input at maximum level, measured in B = 20 kHz, source impedance of the used input = 1 kΩ,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{in\ max}}$$ according to DIN 45405 (CCIR 468).

6. f = 20 Hz to 20 kHz.
7. All outputs are short-circuit proof (static).
8. The inputs and output (apart from SDA, SCL and OFF) withstand tests of MIL-STD-883 C. It is advisable to connected series resistors to these pins.
9. Timings $t_{S,\ DAT}$ and $t_{H,\ DAT}$ deviate from the I^2C bus specification. After reset has been activated, transmission may only be started after a 50 μs delay.

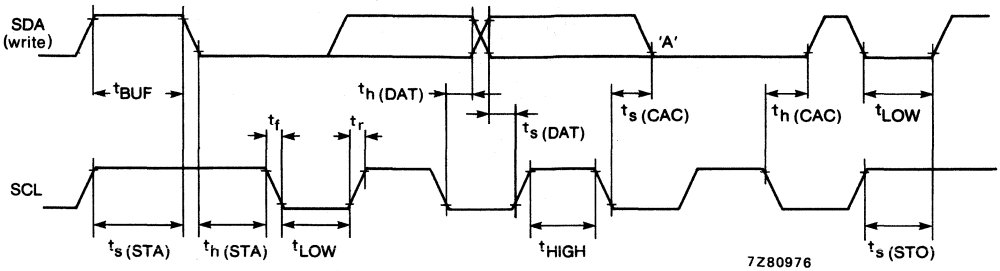


Fig. 2 Timing diagram I^2C bus.

DEVELOPMENT DATA

SUPERSEDES DATA OF OCTOBER 1985

I²C-BUS INTERFACE FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

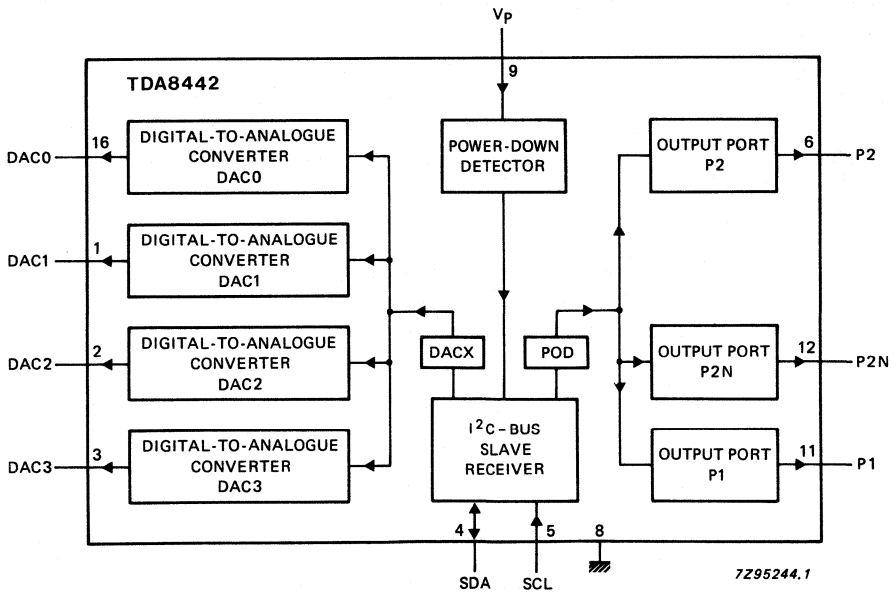


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

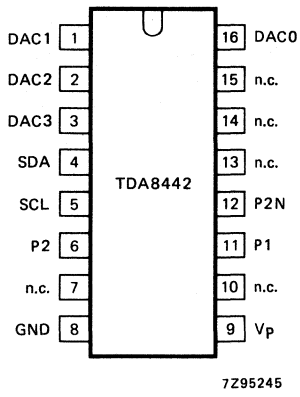


Fig. 2 Pinning diagram

PINNING

1	DAC1	analogue output 1
2	DAC2	analogue output 2
3	DAC3	analogue 3
4	SDA	serial data line } I^2C-bus
5	SCL	serial clock line } I^2C-bus
6	P2	Port 2 npn collector output with internal pull-up resistor
7	n.c.	not connected
8	GND	supply return (ground)
9	V_P	positive supply voltage
10	n.c.	not connected
11	P1	Port 1 open npn emitter output
12	P2N	inverted P2 output
13	n.c.	not connected
14	n.c.	not connected
15	n.c.	not connected
16	DAC0	analogue output 0

FUNCTIONAL DESCRIPTION

Control

Analogue control is facilitated by four 6-bit digital-to-analogue converters (DAC0 to DAC3). The values of the output voltages from the DACs are set via the I^2C-bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals. It is an open npn emitter output capable of sourcing 14 mA (min.).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are npn collector outputs with internal pull-up resistors of 10 kΩ (typ.). Both outputs are capable of sinking up to 2 mA with a voltage drop of less than 400 mV. If one output is switched on (LOW), the other output is switched off, and vice versa.

Reset

The power-down-reset mode occurs whenever the positive supply voltage falls below 8.5 V (typ.) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C-bus (specifications for the I²C-bus will be supplied on request). Programming of the TDA8442 is performed using the format shown in Fig. 3.

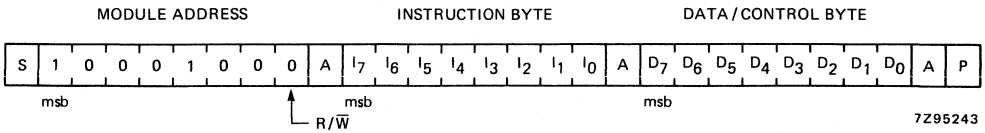


Fig. 3 TDA8442 programming format.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down-reset mode ($V_P > 8.5$ V (typ.)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) together with the corresponding data/control bytes (see Fig. 4).

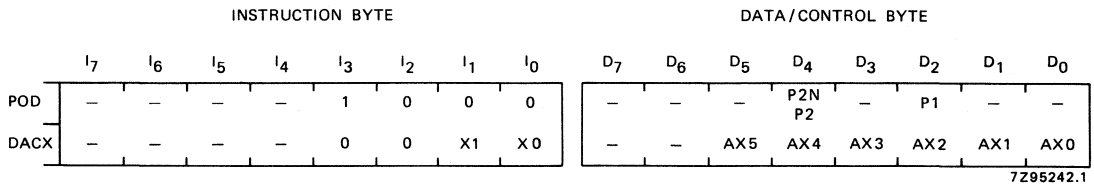


Fig. 4 Control programming.

POD bit P1: If a logic 1 is programmed, the P1 output is switched on. If a logic 0 is programmed or after a power-down-reset, the P1 output is switched off (high-impedance state).

POD bit P2/P2N: If a logic 1 is programmed, the P2 output is switched off and the P2N output is switched on (LOW). If a logic 0 is programmed or after a power-down-reset, the P2 output is switched on (LOW) and the P2N output is switched off.

DAX bits AX5 to AX0: The digital-to-analogue converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using bits AX5 to AX0, the lowest value being with all data AX5 to AX0 at logic 0 or when power-down-reset has been activated.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 9)	V_P	−0.3	+ 13.2	V
Input/output voltage ranges				
pin 4	V_{SDA}	−0.3	+ 13.2	V
pin 5	V_{SCL}	−0.3	+ 13.2	V
pin 6	V_{P2}	−0.3	V_P*	V
pin 11	V_{P1}	−0.3	V_P*	V
pin 12	V_{P2N}	−0.3	V_P*	V
pins 1 to 3 and pin 16	V_{DAX}	−0.3	V_P*	V
Total power dissipation	P_{tot}	–	1	W
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = + 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current (pin 9)	no outputs loaded	I_P	8	13	18	mA
I²C-bus inputs						
SDA (pin 4); SCL (pin 5)						
Input voltage HIGH	note 1	V_{IH}	3.0	–	V_P−1	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH	note 1	I_{IH}	–	–	10	μA
Input current LOW	note 1	I_{IL}	–	–	10	μA
I²C-bus output						
SDA (pin 4)	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	3	5	–	mA

* Pin voltage may exceed V_P if the current in that pin is limited to 10 mA.

parameter	conditions	symbol	min.	typ.	max.	unit
Ports P2 and P2N (pins 6 and 12)	npn collector output with pull-up resistor to V_P					
Internal pull-up resistor to V_P		R_O	5	10	15	kΩ
Output voltage switched on (LOW)	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	2	5	–	μA
Leakage current output switched off		$-I_{leak}$	–	–	25	μA
Port P1 (pin 11)	open npn emitter output					
Output current switched on	V_O = 0 to 5 V	I_O	14	–	–	mA
Leakage current switched off	V_O = 0 to V_P	$\pm I_{leak}$	–	–	100	μA
Digital-to-analogue outputs	note 2					
DAC0 (pin 16)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	3.0	–	4.25	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.15	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	16	–	72	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	45	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC1 (pin 1)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Digital-to-analogue outputs (continued)						
DAC2 (pin 2)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = −2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC3 (pin 3)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	10.0	–	11.2	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.1	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	70	–	250	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	150	mV
Output impedance	I_O = −2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
Power-down reset						
Maximum value of V_P at which power-down reset is active		V_{PD}	6	–	10	V
Rise time of V_P during power-on	V_P rising from 0 V to V_{PD}	t_r	5	–	–	μs

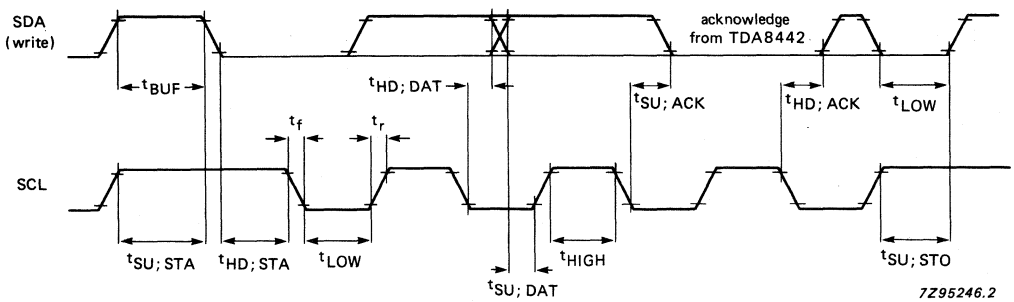
Notes to the characteristics

1. If $V_p < 1$ V, the input current is limited to 10 μA at input voltages up to 13.2 V.
2. Pure capacitive load should be avoided because of possible oscillations.
3. Values are proportional to V_P.

I²C-BUS TIMING

Bus loading conditions: 4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND. All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4.0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
LOW period SCL, SDA	t_{LOW}	4.0	–	–	μs
HIGH period SCL	t_{HIGH}	4.0	–	–	μs
Rise time SCL, SDA	t_r	–	–	1.0	μs
Fall time SCL, SDA	t_f	–	–	0.30	μs
Data set-up time (write)	$t_{SU;DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD;DAT}$	1	–	–	μs
Acknowledge (from TDA8442) set-up time	$t_{SU;ACK}$	–	–	3.5	μs
Acknowledge (from TDA8442) hold time	$t_{HD;ACK}$	0	–	–	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs



Reference levels are 10 and 90%.

Fig. 5 I²C-bus timing; TDA8442.

I²C-BUS CONTROLLED YUV/RGB INTERFACE

GENERAL DESCRIPTION

The TDA8443A is intended for use in a colour television receiver with a peritelevision connector, for switching and matrixing of external RGB and internal YUV signals. The IC is controlled by an I²C-bus compatible microcontroller, such as the MAB8400, with seven sub-addresses or can be used in a non-I²C-bus mode. In the non-I²C-bus mode, control of the circuit is achieved by DC voltages. The TDA8443A is designed for use with standard decoder levels.

Features

- Two RGB/YUV selectable clamped inputs with associated synchronization
- RGB/YUV matrix
- 3-state switching with an OFF-state
- Four amplifiers with selectable gain
- I²C-bus or non-I²C-bus mode
- Slave receiver in the I²C-bus mode
- External OFF command
- Expandable system (up to seven devices on the same bus)
- Fast switching to allow for mixed modes

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 18)		$V_P = V_{18-22}$	10.8	12.0	13.2	V
Supply current		I_P	–	65	90	mA
RGB/YUV channels						
Output impedance						
pin 19		$\|Z_{19-22}\|$	–	7	30	Ω
pin 20		$\|Z_{20-22}\|$	–	7	30	Ω
pin 21		$\|Z_{21-22}\|$	–	7	30	Ω
Bandwidth						
–3 dB	mode 0 or 2	B	–	25	–	MHz
+3 dB	mode 0 or 2	B	–	12	–	MHz
+3 dB	mode 1	B	–	10	–	MHz
Maximum output amplitude of YUV signals (peak-to-peak)	gain x 1	$V_{O(p-p)}$	2.1	–	–	V
	gain x 2	$V_{O(p-p)}$	4.1	–	–	V
Operating ambient temperature range		T_{amb}	0	–	+70	°C

PACKAGE OUTLINE

24-lead DIL; plastic with internal heat spreader (SOT101B).

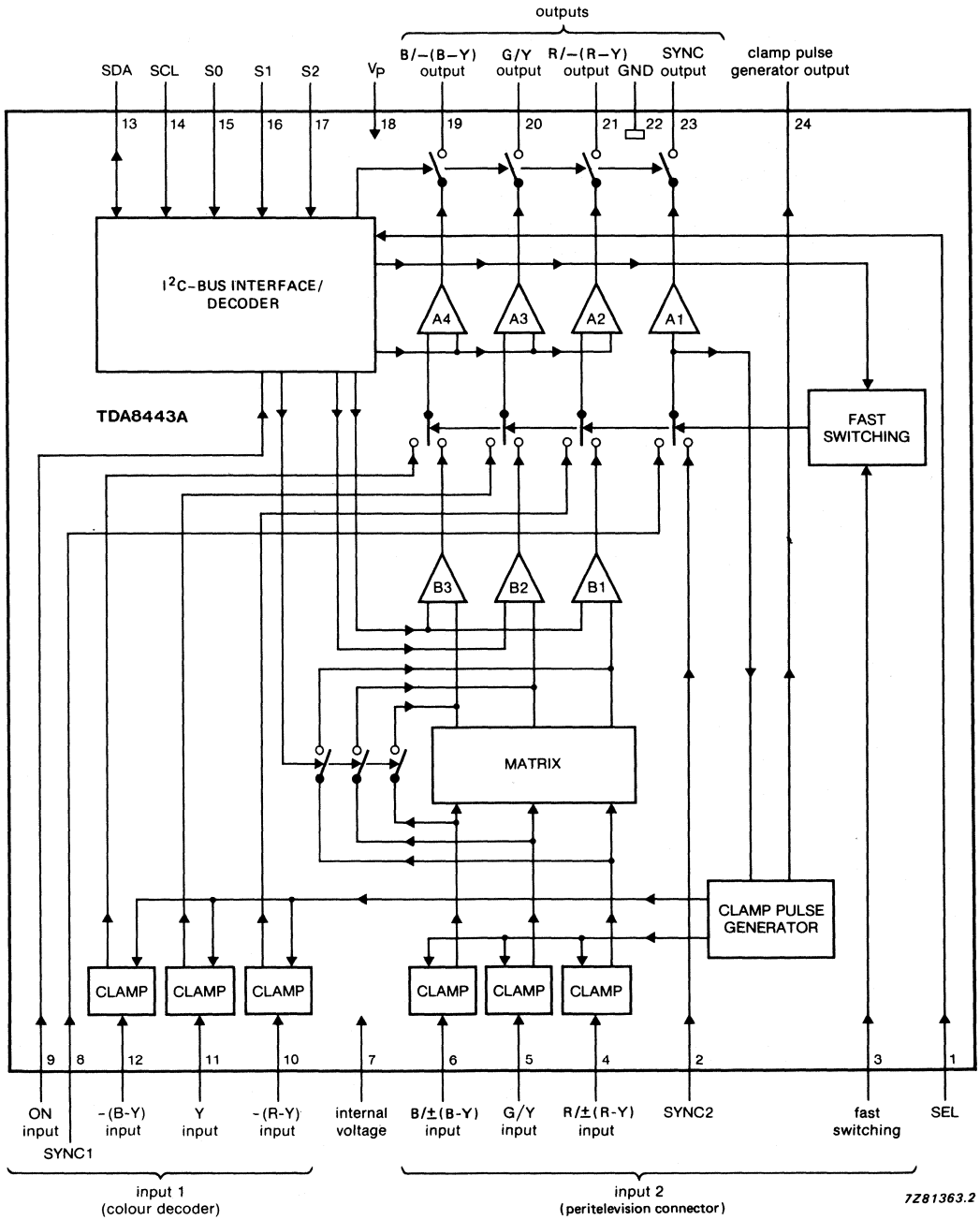


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

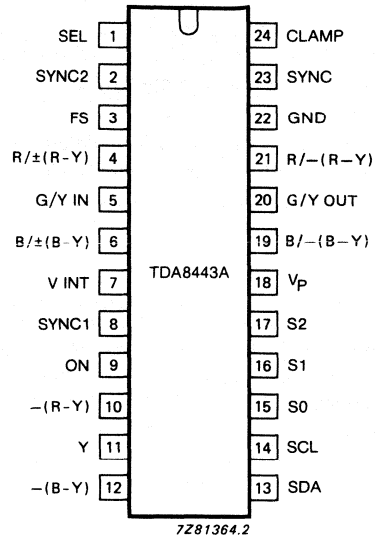


Fig.2 Pinning diagram.

1	SEL	select input (non-I²C-bus mode only)	
2	SYNC2	synchronization input via the peritelevision connector	
3	FS	fast switching input	
4	R/± (R-Y)	R or (R-Y) input	
5	G/Y IN	G or Y input	
6	B/± (B-Y)	B or (B-Y) input	
7	V INT	internal voltage supply	
8	SYNC1	synchronization input from a standard colour decoder	
9	ON	ON input	
10	−(R-Y)	−(R-Y) signal input	
11	Y	Y signal input	
12	−(B-Y)	−(B-Y) signal input	
13	SDA	serial data input/output	I²C-bus
14	SCL	serial clock input	I²C-bus
15	S0	subaddress inputs	I²C-bus
16	S1		I²C-bus
17	S2		I²C-bus
18	V_P	positive supply voltage	
19	B/−(B-Y)	B or −(B-Y) signal output	
20	G/Y OUT	G or Y signal output	
21	R/−(R-Y)	R or −(R-Y) signal output	
22	GND	ground	
23	SYNC	synchronization output	
24	CLAMP	clamping pulse generator output	

FUNCTIONAL DESCRIPTION

The circuit contains two sets of inputs (see Fig.1): input 1 receives colour difference signals from a colour decoder and input 2 receives RGB/YUV signals via a peritelevision connector. Each set of inputs has its own synchronization input. The inputs are clamped by a clamping pulse, which is internally generated from the synchronization inputs.

In the RGB mode the signals are internally matrixed to form colour difference signals, before further processing is carried out by a control circuit (such as the TDA8461).

The outputs can be set in a high impedance OFF state, which allows the use of up to seven devices in parallel (I^2C-bus mode).

Control

The circuit can be controlled by an I^2C-bus compatible microcontroller or directly by DC voltages. The fast switching input can be operated via pin 16 of the peritelevision connector. Inputs can also be changed by applying a signal, (e.g. a sandcastle pulse) to pin 24. The internal clamping pulse will occur during the time that the signal at pin 24 is between 5.5 and 6.5 V. If both a sync signal and a pin 24 signal are used the signal should be applied to pin 24 via a 1 kΩ resistor.

I²C-bus mode

The protocol for the devices in I²C-bus mode is shown in Fig.3.

STA : start condition
A6 : 1
A5 : 1
A4 : 0
A3 : 1
} fixed address bits
A2 : subaddress bit set by S2
A1 : subaddress bit set by S1
A0 : subaddress bit set by S0
R/$\overline{W}$: read/write bit (= 0 only write mode allowed)
ACK : acknowledge, generated by the TDA8443A
D7 : MOD1
D6 : MOD0
} mode control bits, see Table 2
D5 : G2
D4 : G1
D3 : G0
} gain control bits, see Table 4
D2 : PRIOR, priority bit
D1 : ON/OFF bit
D0 : ON/OFF active bit

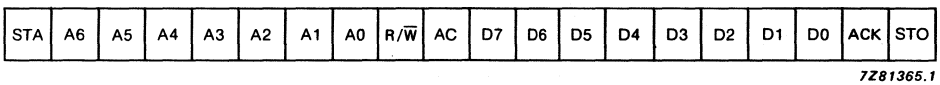


Fig.3 I²C-bus protocol.

Table 1 subaddressing

slave addressing bit			address select pins		
A2	A1	A3	S2	S1	S0
*	*	*	L	L	L
0	0	1	L	L	H
0	1	0	L	H	L
0	1	1	L	H	H
1	0	0	H	L	L
1	0	1	H	L	H
1	1	0	H	H	L
1	1	1	H	H	H

Where:

L = input voltage LOW
H = input voltage HIGH
* = non-I²C-bus operation

I²C-bus mode (continued)

Table 2 Mode control bits (note 1)

MOD 1 (bit)	MOD 0 (bit)	mode
0	0	0
0	1	1
1	0	2
1	1	3

Table 3 Priority/fast switching (note 1)

PRIOR (bit)	fast switching pin	mode
0	X	0 to 2 (note 2)
1	0.4 V	2
1	1 to 3 V	0 or 1 (note 3)

Notes to Tables 2 and 3

1. In Mode 0 input 2 is directly selected;
   In Mode 1 input 2 is selected via RGB/YUV matrix;
   In Mode 2 input 1 is directly selected.
   Mode 3 is reserved, do not use.
2. Defined by mode control bits.
3. Defined by mode control except mode 2 which revers to mode 0.

Table 4 Gain setting

G2 (bit)	G1 (bit)	G0 (bit)	A1	A2, A3, A4	B1, B3	B2
0	0	0	1	1	−1	0.45
0	0	1	1	1	1	1
0	1	0	reserved, do not use			
0	1	1	1	1	−1	0.45
1	0	0	2	2	−1	0.45
1	0	1	2	1	1	1
1	1	0	2	2	1	1
1	1	1	2	1	−1	0.45

Matrix equations

The relationship between output and input signals of the matrix is as follows:

$Y = 0.3\ R + 0.59\ G + 0.11\ B$
$R\text{-}Y = 0.7\ R - 0.59\ G - 0.11\ B$
$B\text{-}Y = -0.3\ R - 0.59\ G + 0.89\ B$

Table 5 ON bit

ON	function
0	OFF, no output signal, high impedance OFF state
1	ON, normal function

Table 6 OFF active – ON (pin 9)

OFF active (bit)	ON (bit)	function
0	L	OFF
0	H	according to protocol, last defined D7 to D1 (maybe entered when ON = L)
1	X	according to protocol, last defined D7 to D1

Power-on reset

If the circuits are switched on in the I²C-bus mode, all bits of D0 to D7 are set to zero.

Timing specifications

I²C-bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	max.	unit
Bus free before start	t_{BUF}	4.7	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	μs
SCL and SDA LOW time	t_{LOW}	4.7	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	μs
SCL and SDA rise time	t_r	–	1.0	μs
SCL and SDA fall time	t_f	–	0.3	μs
Data set-up time (write)	$t_{SU;DAT}$	250	–	ns
Data hold time (write)	$t_{HD;DAT}$	1.0	–	μs
Acknowledge set-up time	$t_{SU;ACK}$	–	2	μs
Acknowledge hold time	$t_{HD;ACK}$	0	–	μs

Note

Timing $t_{HD,\ DAT}$ deviates from the I²C-bus specification. After reset has been activated, a delay of 50 μs must occur before transmission may be resumed.

DEVELOPMENT DATA

I²C-bus mode (continued)

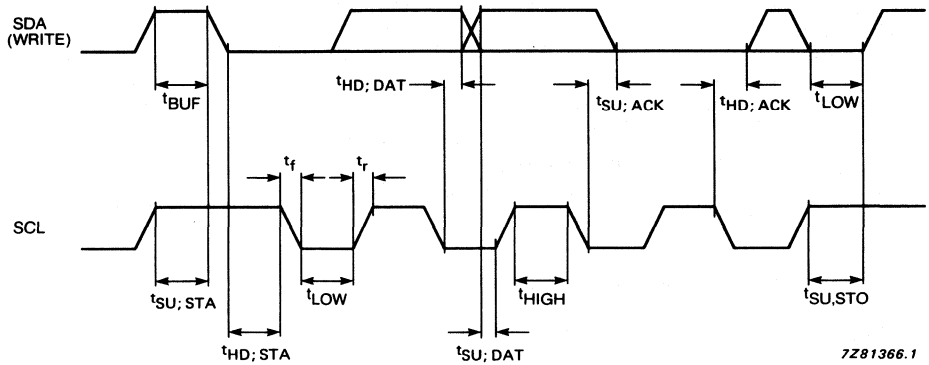


Fig.4 I²C-bus timing diagram.

Non-I²C-bus mode

Table 7 Non-I²C-bus mode (S2 = S1 = S0 = L)

control			mode switched	gain settings			
SDA	SCL	SEL	by FS	A1	A4, A3, A2	B1, B3	B2
L	L	L	2/0	1	1	1	1
L	L	H	2/0	1	2	1	1
L	H	L	2/1	1	1	−1	0.45
L	H	H	2/0	1	1	−1	0.45
H	L	L	2/0	2	1	1	1
H	L	H	2/0	2	2	1	1
H	H	L	2/1	2	1	−1	0.45
H	H	H	2/0	2	1	−1	0.45

Table 8 Fast switching input (pin 3)

FS	mode selected
⩽ 0.4 V	mode 2
1 to 3 V	mode 0 or mode 1 as set by control

Table 9 ON input (pin 9)

ON	function
L	OFF, no output signal, high impedance OFF state
H	function is determined in Table 7

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 18)	V_P	–	14	V
Input voltage range				
SDA (pin 13)	V_I	–0.3	14	V
SCL (pin 14)	V_I	–0.3	14	V
any other pin	V_i	–0.3	V_P + 0.3	V
Maximum output current	I_O	–	20	mA
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Storage temperature range	T_{stg}	–55	+ 125	°C
Maximum junction temperature	T_j	–	+ 125	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 18)		V_P	10.8	12.0	13.2	V
Supply current		I_P	–	65	90	mA
RGB/YUV channels						
Absolute gain difference (programmed value)			–	0	10	%
Relative gain difference						
between Y output and the (R-Y) and (B-Y) channel inputs			–	0	10	%
between any two channels			–	0	5	%
Input current		I_I	–	0.5	1.0	μA
Output impedance						
pin 19		$\lvert Z_{19-22}\rvert$	–	7	30	Ω
pin 20		$\lvert Z_{20-22}\rvert$	–	7	30	Ω
pin 21		$\lvert Z_{21-22}\rvert$	–	7	30	Ω
Bandwidth						
–3 dB	mode 0 or 2	B	–	25	–	MHz
+3 dB	mode 0 or 2	B	–	12	–	MHz
+3 dB	mode 1	B	–	10	–	MHz
Mutual time difference at output	all inputs of one source connected together		–	–	25	ns
Maximum output amplitude of YUV signals (peak-to-peak value)	gain x 1	$V_{O(p-p)}$	2.1	–	–	V
	gain x 2	$V_{O(p-p)}$	4.2	–	–	V
Crosstalk between	note 1					
inputs of same source	f = 5 MHz	α	–	–	–30	dB
different sources		α	–	–	–40	dB
Isolation (OFF state)	f = 10 MHz		50	–	–	dB

DEVELOPMENT DATA

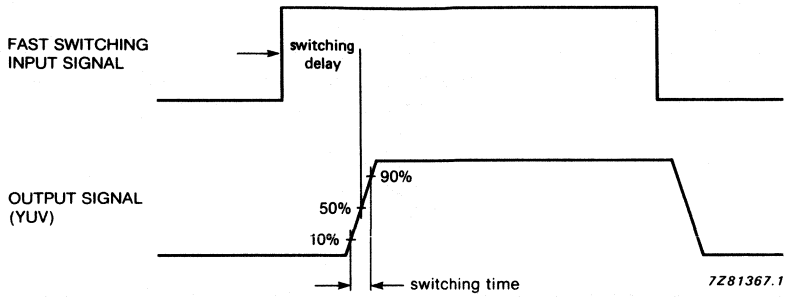
parameter	conditions	symbol	min.	typ.	max.	unit
Differential gain at nominal output signals (peak-to-peak value)	R-Y = 1.05 $V_{(p-p)}$		–	–	10	%
	B-Y = 1.33 $V_{(p-p)}$		–	–	10	%
	Y = 0.34 $V_{(p-p)}$		–	–	10	%
Signal-to-noise ratio nominal input	note 2 B = 5 MHz	S/N	50	–	–	dB
Supply voltage ripple rejection	note 3	RR	30	–	–	dB
DC output levels during clamping		V_O	–	5.3	–	V
Synchronization channels						
Gain difference (programmed value)			–	–	10	%
Bandwidth						
3 dB		B	–	50	–	MHz
+ 3 dB gain x 1		B	–	20	–	MHz
+ 3 dB gain x 2		B	–	13	–	MHz
Input amplitude of sync signal for correct operation of clamp pulse generator (peak-to-peak value)		$V_{I(p-p)}$	0.2	–	2.5	V
Output impedance (pin 23)		$\lvert Z_{23-22}\rvert$	–	20	30	Ω
Maximum undistorted output amplitude (pin 23) (peak-to-peak value)		$V_{O(p-p)}$	2.5	–	–	V
DC output level on top of sync pulse		V_O	1.5	1.9	2.4	V
I²C-bus inputs						
SDA, SCL						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA
I²C-bus output						
SDA (open collector)						
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.4	V
Output sink current LOW		I_{OL}	–	5	–	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Subaddress inputs						
S0, S1, S2						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	−50	−10	0	μA
Fast switching input						
Input voltage HIGH		V_{IH}	1	–	3	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	500	μA
Input current LOW		I_{IL}	−100	–	–	μA
Switching time	see Fig.5	t	–	10	–	ns
Switching delay	see Fig.5	t_d	–	20	–	ns
Select input						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	−50	−10	0	μA
ON input						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA

Notes to the characteristics

1. Crosstalk is defined as the unwanted data transfer from an output, driven at nominal level, to other inputs and outputs on the IC and is expressed as a ratio in dBs.
2. Signal-to-noise ratio = $20 \log \frac{V_{O(p\text{-}p)}}{V_O \text{ noise (RMS) } B = 5 \text{ MHz}}$
3. Supply voltage ripple rejection = $20 \log \frac{V_{RR} \text{ supply}}{V_{RR} \text{ on the output}}$



Input = 0 V (input 1; Mode 2)
Input = 0.75 V (RGB; Mode 1)

Fig.5 Fast switching signal diagram.

DEVELOPMENT DATA

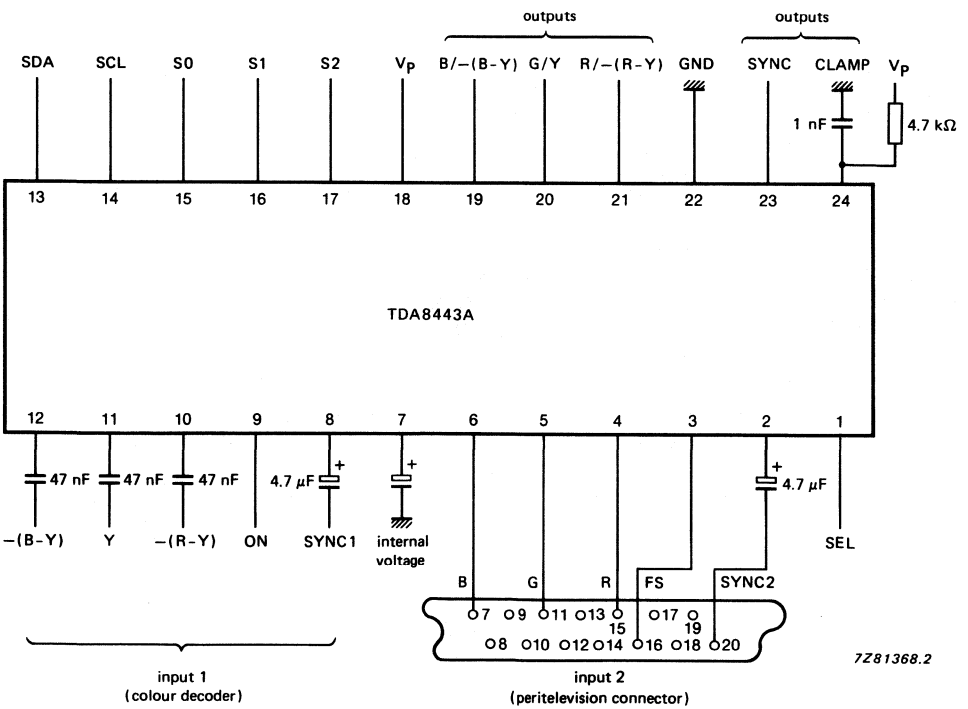


Fig.6 Application diagram.

APPLICATION INFORMATION

Table 10 Application information

input 1	input 2	output	mode	G2	G1	G0
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.6 V	2	1	1	1
	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V		1	1	1	1
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.68 V U = −2.66 V V = −2.10 V S = 0.6 V	2	1	0	0
	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V		1	1	0	0
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.6 V	2	1	0	1
	Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		0	1	0	1
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.68 V U = −2.66 V V = −2.10 V S = 0.6 V	2	1	1	0
	Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		0	1	1	0

OCTUPLE 6-BIT DAC WITH I²C-BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

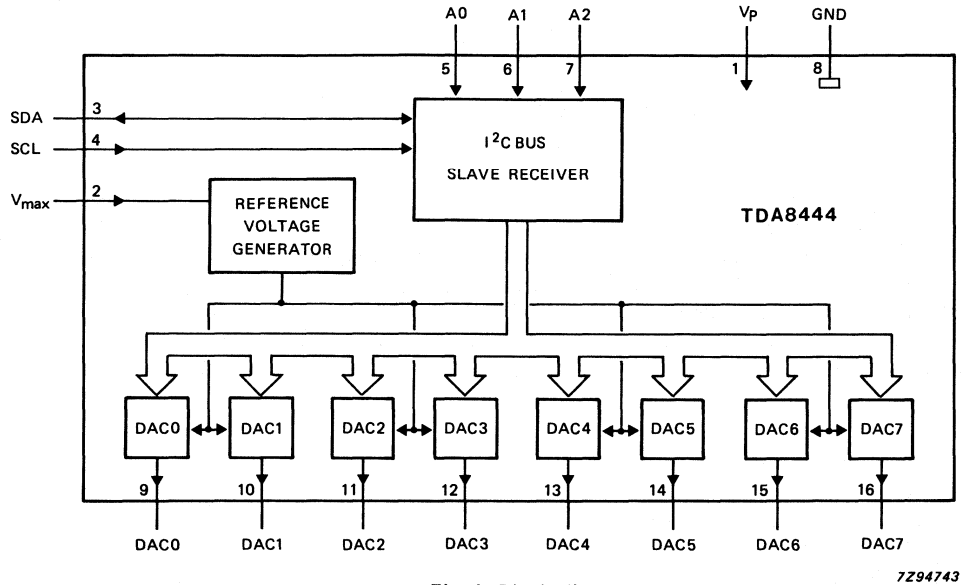


Fig. 1 Block diagram.

PINNING

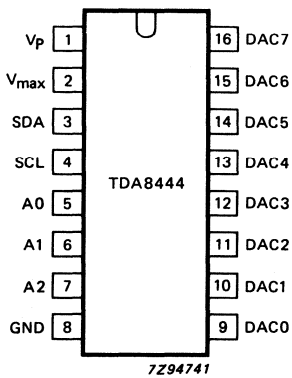


Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I^2C-bus serial data input/output
4	SCL	I^2C-bus serial data clock
5	A0	programmable address bits for I^2C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	← address byte →		← instruction byte →		← first data byte →		

Where:

S = start condition
P = stop condition
A = acknowledge
X = don't care
A2, A1, A0 = programmable address bits
I3, I2, I1, I0 = instruction bits
SD, SC, SB, SA = subaddress bits
D5, D4, D3, D2, D1, D0 = data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to Vp for An = 1. If the inputs are left floating, An = 1 will result.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_p = I_1$	−	−10	mA
		$I_P = I_I$	−	40	mA
I^2C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_I	−0.5	$V_P + 0.5$	V
Output voltage		V_O	−0.5	$V_P + 0.5$	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	−	10	mA
Total power dissipation		P_{tot}	−	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$i_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	V_P	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}	see note			V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

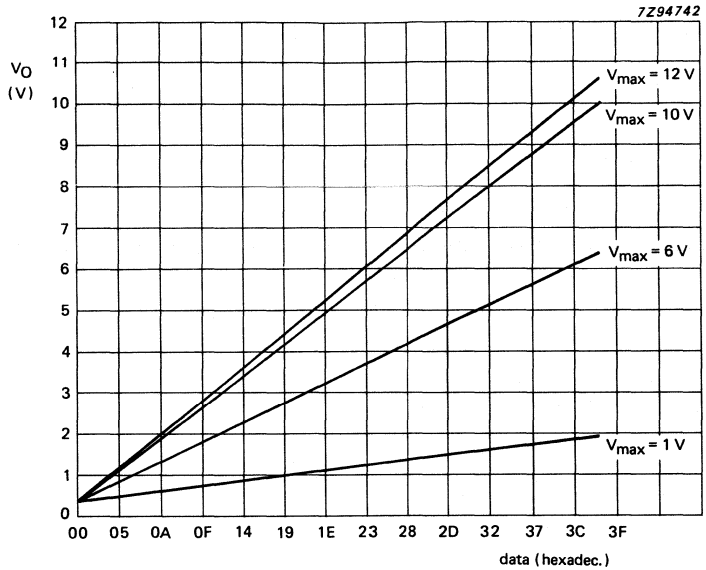


Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

PAL/NTSC DECODER WITH I²C BUS CONTROL

GENERAL DESCRIPTION

The TDA8461 is a multistandard colour decoder used in conjunction with delay line TDA8451, filter TDA8452 and SECAM decoder TDA8490. It combines all the functions required for the identification and demodulation of PAL/NTSC signals. The decoder comprises an I²C bus interface used to control the following functions:

- contrast
- saturation
- brightness
- hue, when in the NTSC position
- white point adjustment of the three colours
- peak white limiter adjustment

Via the I²C bus the decoder can be forced into the following modes: PAL, NTSC (4,43 MHz), NTSC (3,58 MHz) and SECAM when applied with the TDA8490.
The bus also indicates, as slave transmitter, the mode of the incoming signal (PAL, NTSC or SECAM).
The decoder contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. channel number display, Teletext, Antiope, etc.).

Features

- I²C bus control
- Integrated filters (TDA8452) and delay lines (TDA8451) used in combination with TDA8461 eliminate the need for wire-wound components and adjustments
- A black-current stabilizer which controls the black currents of the three electron guns to a level low enough to omit the black level adjustment
- Inputs for RGB signals and fast switching
- Contrast and brightness control of inserted RGB signals
- Self-aligned oscillator
- Capacitive coupling of the luminance, colour difference and RGB inputs with black level clamping
- Equal black levels for internal TV and external signals
- Adjustable peak white limiter
- Matrix coefficients selectable for PAL/SECAM and NTSC (correction for FCC primaries)
- 12 MHz bandwidth
- Emitter follower outputs for driving the RGB output stages
- Two sandcastle pulse inputs for maximum design flexibility
- I²C bus on controlled DAC output

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 27)	V_P	10	12	13,2	V
Supply current (pin 27)	I_P	–	110	–	mA

PACKAGE OUTLINE

TDA8461: 40-lead DIL; plastic with internal heat spreader (SOT-129).

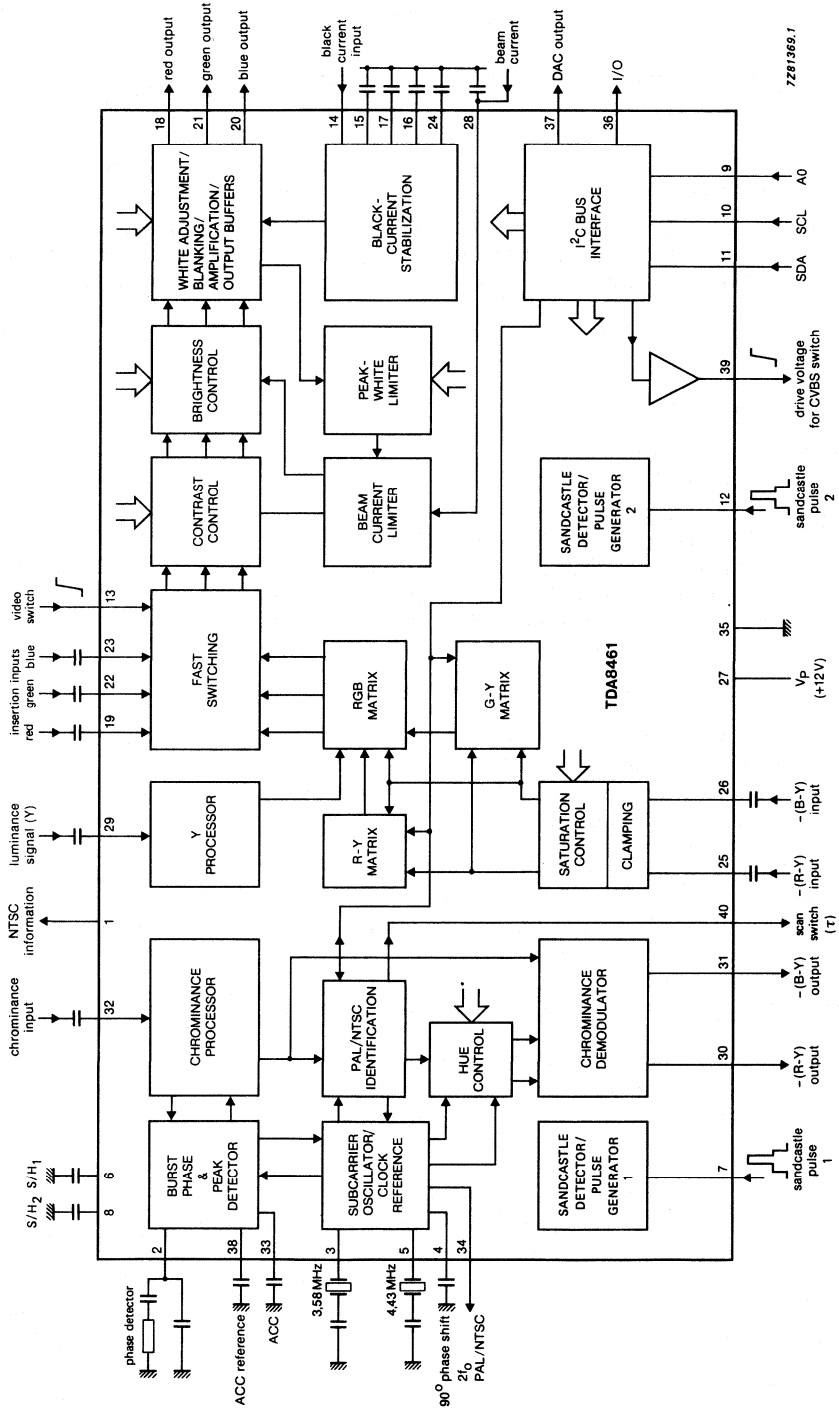


Fig. 1 Block diagram.

DEVELOPMENT DATA

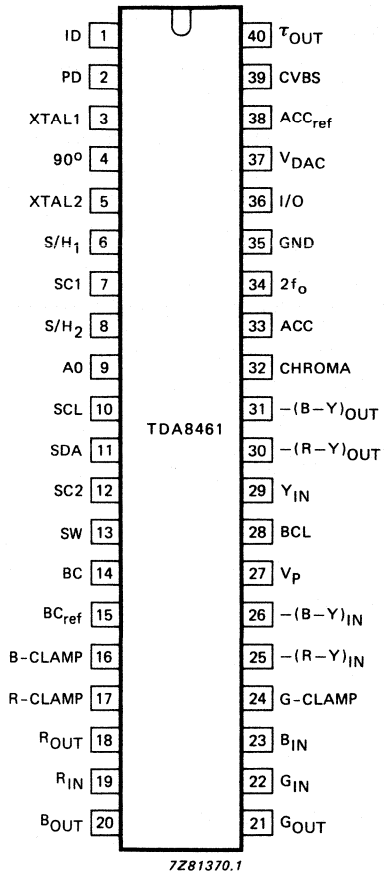


Fig. 2 Pinning diagram.

PIN FUNCTIONS

pin no.	mnemonic	description
1	ID	NTSC 3,58 identification information
2	PD	Phase detector
3	XTAL1	3,58 MHz NTSC reference frequency input
4	90^o	90^o phase shift DC reference
5	XTAL2	4,43 MHz PAL reference frequency input
6	S/H_1	Sample and hold 1 (PAL identification)
7	SC1	Sandcastle pulse input 1
8	S/H_2	Sample and hold 2 (NTSC identification)
9	AO	Programmable slave address pin
10	SCL	I^2C serial clock line
11	SDA	I^2C serial data line
12	SC2	Sandcastle pulse input 2
13	SW	Video switch input
14	BC	Black current input
15	BC_{ref}	Black current reference
16	B-CLAMP	B clamping circuit
17	R-CLAMP	R clamping circuit
18	R_{OUT}	Red signal output
19	R_{IN}	Red insertion input
20	B_{OUT}	Blue signal output
21	G_{OUT}	Green signal output
22	G_{IN}	Green insertion input
23	B_{IN}	Blue insertion input
24	G-CLAMP	G clamping circuit
25	$-(R\text{-}Y)_{IN}$	–(R-Y) colour difference input
26	$-(B\text{-}Y)_{IN}$	–(B-Y) colour difference input

pin no.	mnemonic	description
27	V_P	Positive supply voltage
28	BCL	Beam current limiter input
29	Y_{IN}	Luminance input
30	$-(R\text{-}Y)_{OUT}$	−(R-Y) signal output
31	$-(B\text{-}Y)_{OUT}$	−(B-Y) signal output
32	CHROMA	Chrominance input
33	ACC	Automatic colour control
34	$2f_o$	Frequency doubler output
35	GND	Ground
36	I/O	Input/output interface
37	V_{DAC}	DAC output voltage
38	ACC_{ref}	Automatic colour control reference voltage
39	CVBS	Drive voltage for CVBS switch (TDA8452)
40	τ_{OUT}	Scan switch output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Colour decoder

The chrominance signal is amplified and is supplied to three detectors; the burst phase detector (ref. sign. R-Y phase), the automatic colour control (ACC) + NTSC synchronous detector (ref. sign. B-Y phase) and the PAL identification detector (ref. sign. ± R-Y phase).

The burst phase detector controls the oscillator which can operate at either 3,58 or 4,43 MHz. The internal switching selects the required crystal. The oscillator is followed by a Miller integrator to obtain the required 90^{o} phase shift and is biased to provide a sine-wave output.
Reference signals obtained from the oscillator and phase shift circuit are then used for the synchronous demodulation of the (B-Y) and (R-Y) signals. The demodulated colour difference signals then have the required amplitude ratio and are fed to the delay line circuit of the TDA8451. If the SECAM decoder TDA8490 is used, then the outputs from this device can be directly connected to the outputs of the TDA8461. The output levels have been chosen so as to give the PAL decoder priority (output level during PAL or NTSC is higher than output level during SECAM reception).

To provide the ACC voltage, the output signal from the ACC and NTSC detector is peak detected and delivered to a sample and hold circuit. The output from the PAL identification detector is also applied to a sample and hold circuit. These two circuits provide the incoming signal identification and the colour killer information.

Signal identification

The decoder scans the various systems sequentially (four fields per system).
As soon as a signal is identified, the scanning stops and the decoder remains locked to that standard until the killer indicates that the signal has disappeared. After this indication, the scanning will resume. If the TDA8461 is to be used in conjunction with the TDA8490 SECAM decoder, the TDA8461 will be forced into the PAL mode on reception of a SECAM signal. This is because the delay lines for the colour difference signals in the TDA8451 are only operative in this mode.

The scanning system does not remain active during black/white reception as this would cause switching of the filters in the TDA8452. Scanning stops when no ACC voltage is present.

Both TDA8451/2 require a reference signal of $2 \times f_o$. To provide this, the oscillator frequency is internally doubled and is available at pin 34. Depending upon the incoming signal (PAL or NTSC), the DC voltage level on this pin is subject to change. This level change is detected by the TDA8451 so that the delayed signal can be switched OFF for NTSC (3,58 MHz and 4,43 MHz).

When an NTSC signal is identified the hue control circuit is switched-on. Hue control is provided by combining the two quadrature colour reference signals.

Control circuit

The luminance signal is derived from the TDA8452. The control circuit has inputs for luminance and colour difference signals, plus RGB inputs with fast switching. The required luminance signal amplitude is 0,45 V (p-p). After amplification, this signal is supplied to the R, G and B matrix where the colour difference signals are controlled on saturation. The (G-Y) signal is generated after control. The ratio of the colour difference signals which are fed to the RGB matrix is different for both PAL and NTSC signals:

For PAL the normal matrix is followed i.e. (G-Y) = −0,51 (R-Y) −0,19 (B-Y).
For NTSC a new (R-Y) signal is generated consisting of:

$$1{,}57(R\text{-}Y) - 0{,}41(B\text{-}Y).$$

Furthermore, the (G-Y) matrix is changed to −0,43(R-Y) −0,11(B-Y).

The (B-Y) factor remains unchanged, this is to obtain the preferred phase angle and amplitude ratio as normally used for NTSC.

After matrixing, the R, G and B signals are supplied to a switch circuit on which external RGB signals can be chosen. After amplification the RGB signals are controlled for contrast and brightness. The signals are fed to the output via white point adjustment. Typical output signal amplitudes are 4 V black to white (nominal controls). The black level of the three output signals is controlled by a black current stabilization circuit. The black current of the picture tube is obtained in the usual way (see TDA3566).

The TDA8461 has a peak-white limiting circuit. Because the black level at the outputs is dependent upon the black current feedback, the peak-white limiting circuit is adjustable via the I²C bus. Peak white reduces the signal amplitude via contrast. The device has a separate input for average beam current which reduces the signal amplitude via contrast and/or brightness, this is also adjustable via the I²C bus.

DEVELOPMENT DATA

I²C BUS SPECIFICATION

Write

The TDA8461 is controlled via the 2-line I²C bus as specified in the user manual "Single-chip 8-bit microcontrollers". In order to set up the TDA8461, a control message comprising a slave address, a R/W bit, a subaddress byte and one or more data bytes must be written to the device. The control word format is shown in Fig. 3, where AO (pin 9) is a pin programmable slave address bit.

If more than one data byte follows the subaddress, these bytes are stored in the successive registers by the automatic subaddress increment feature.

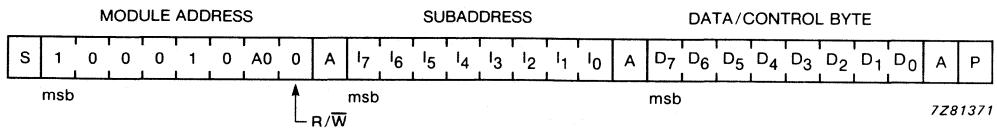


Fig. 3 Control word format for slave receiver.

Note: An acknowledge is only generated when a valid address is received.

I²C BUS SPECIFICATION (continued)

Control

Table 1 shows the bit arrangement and function of each data byte used in the control word.

Table 1 Control data

function	sub-address	data byte							
		D7	D6	D5	D4	D3	D2	D1	D0
brightness	00	X	X	A05	A04	A03	A02	A01	A00
saturation	01	X	X	A15	A14	A13	A12	A11	A10
contrast	02	X	X	A25	A24	A23	A22	A21	A20
hue	03	X	X	A35	A34	A33	A32	A31	A30
decoder control	04	MTRX	CDM2	CDM1	CDM0	CVBSS	RGBS	OFFN	SWOFF
universal DAC, I/O control	08	OUTP	X	A85	A84	A83	A82	A81	A80
peak white limit	09	BLM1	BLM0	A95	A94	A93	A92	A91	A90
red output gain	0A	X	X	AA5	AA4	AA3	AA2	AA1	AA0
green output gain	0B	X	X	AB5	AB4	AB3	AB2	AB1	AB0
blue output gain	0C	X	X	AC5	AC4	AC3	AC2	AC1	AC0

Control bit definition

MTRX control bit:

1	YUV/RGB matrix in PAL mode
0	YUV/RGB matrix in NTSC mode

If colour decoder mode control bits are set to non-forced mode, the YUV/RGB matrix will follow the "own intelligence" PAL or NTSC mode setting.

CDM2 - CDM0: Colour decoder mode bits

CDM2	CDM1	CDM0	function
0	0	0	not forced mode, own intelligence
0	0	1	forced NTSC, 3,58 MHz if a 3,58 MHz crystal is connected to pin 3
0	1	0	forced PAL –B, G, N or M if the correct crystal is connected to pin 5
0	1	1	forced SECAM*
1	0	0	forced NTSC 4,43 MHz mode*
1	0	1	forced PAL –B, G, N or M if the correct crystal is connected to pin 3
1	1	0	no function, reserved
1	1	1	no function, reserved

* If a 4,43 MHz crystal is connected to pin 5.

CVBSS control bit:

0	CVBS output LOW (CVBS1 selected)
1	CVBS output HIGH (CVBS2 selected)

RGBS source select control bit:

0	internal RGB selected
1	external RGB source selected (e.g. from TXT)

OFFN RGB output control bit:

0	RGB outputs are switched off, dark screen
1	RGB outputs are not switched off

SWOFF switch-off phase detector and killer bit:

0	phase detector and killer not switched off
1	phase detector and killer switched off*

DEVELOPMENT DATA

OUTP output control bit:

0	output = LOW
1	output = HIGH; input mode

BLM0/BLM1 beam limiting control bits:

BLM1	BLM0	mode
0	0	inactive
0	1	active on contrast
1	0	active on brightness
1	1	active on contrast and brightness

Read

The status of TDA8461 can also be read. Figure 4 illustrates status read format for the TDA8461 in the slave transmitter mode.
Note: change in direction of read/write bit.

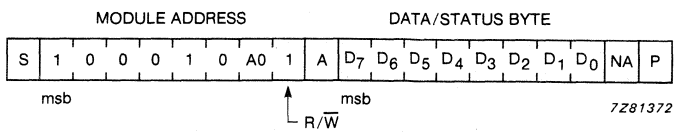


Fig. 4 Status read format slave transmitter.

* Only allowable in forced colour decoding mode.

I²C BUS SPECIFICATION (continued)

The general format of the data byte is shown in Fig. 5.

MSB LSB

PONRES	DECM2	DECM1	DECM0	0	0	0	INP

Fig. 5 Format of data byte.

Bit definition

PONRES power-on reset bit:

A power failure or a power-on reset will set this bit. A succesfull read of the data byte will reset this bit.

DECM2/DECM1/DECM0 colour decoder mode bits:

DECM2	DECM1	DECM0	function
0	0	0	no colour standard identified
0	0	1	NTSC 3,58 MHz
0	1	0	PAL –B, G, N or M*
0	1	0	SECAM
1	0	0	NTSC 4,43 MHz
1	0	1	PAL –B, G, N or M**
1	1	0	unused
1	1	1	unused

INP input function status bit:

0	Input LOW	operates only as input if bit OUTP is logic 1
1	Input HIGH	

Unused status bits are transmitted as logic 0

* Depending upon the crystal connected to pin 5.
** Depending upon the crystal connected to pin 3.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27)	V_P	–	13,2	V
Total power dissipation (encapsulation)	P_{tot}	–	2,5	W
Storage temperature range	T_{stg}	−25	+ 150	°C
Operating ambient temperature range	T_{amb}	−25	+ 70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\,j\text{-}a}$ = 40 K/W

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{27-35} = 12$ V; $T_{amb} = 25$ °C; all voltages referenced to ground unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Chrominance amplifier (pin 32)						
Input signal amplitude (peak-to-peak value)	note 1		–	465	–	mV
Input signal amplitude	preclipping		–	–	1100	mV
Input resistance (pin 32)		R_I	–	12	–	kΩ
Input capacitance (pin 32)		C_I	–	–	4,0	pF
ACC control range			30	–	–	dB
Min. burst amplitude within control range (peak-to-peak value)			30	–	–	mV
Reference section						
Phase locked loop catching range	note 2	Δf	± 500	–	–	Hz
Phase shift for ± 400 Hz deviation of f_{osc}	note 2	$\Delta\varphi$	–	–	5	deg
Oscillator						
Temperature coefficient of oscillator frequency	note 3	TC_{osc}	–	–2	–	Hz/K
Frequency deviation for a supply voltage change from 10 to 13,2 V		Δf_{osc}	–	40	–	Hz
Input resistance (pin 3)		R_I	–	1500	–	Ω
(pin 5)		R_I	–	650	–	Ω
Input capacitance (pins 3 and 5)		C_I	–	–	6,0	pF
ACC generation/identification	note 4					
Voltage at the PAL identification output (pin 6)						
nominal input signal for PAL		V_6	–	5,0	–	V
nominal input signal for NTSC		V_6	–	3,1	–	V
without burst input		V_6	–	3,1	–	V

DEVELOPMENT DATA

parameter	condition	symbol	min.	typ.	max.	unit
Colour-OFF voltage		V_6	–	3,3	–	V
Colour-ON voltage		V_6	–	3,5	–	V
Voltage identification for flip-flop reset		V_6	–	2,8	–	V
Voltage at NTSC identification output (pin 8)						
nominal input signal for PAL		V_8	–	5,3	–	V
nominal input signal for NTSC		V_8	–	5,3	–	V
without burst input		V_8	–	3,1	–	V
Colour-OFF voltage		V_8	–	3,6	–	V
Colour-ON voltage		V_8	–	3,8	–	V
Peak detector voltage (pin 33)						
nominal input signal		V_{33}	–	5,8	–	V
without nominal input signal		V_{33}	–	2,7	–	V
Demodulators						
Output voltage during PAL (R-Y) output (pin 30) (peak-to-peak value)		$V_{30(p-p)}$	0,50	0,62	0,74	V
(B-Y) output (pin 31) (peak-to-peak value)		$V_{31(p-p)}$	0,64	0,80	0,96	V
Output voltage during NTSC (R-Y) output (pin 30) (peak-to-peak value)		$V_{30(p-p)}$	1,00	1,24	1,48	V
(B-Y) output (pin 31) (peak-to-peak value)		$V_{31(p-p)}$	1,28	1,60	1,92	V
Amplification ratio of demodulated signals (B-Y)/(R-Y)		$V_{31,30}$	1,60	1,78	1,96	
Spread of PAL/NTSC signal amplitude ratio	(R-Y) channel		−1	–	1	dB
Frequency response	0 to 1 MHz		–	−3	–	dB
Colour difference output impedance		Z_O	–	100	–	Ω

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Demodulators (continued)						
DC output voltage after signal identification		$V_{31,30}$	–	8,3	–	V
DC output voltage during colour killing		$V_{31,30}$	–	1,3	–	V
Unwanted signals at (R-Y)/(B-Y) outputs	note 5		–	–	*	dB
Residual carrier (peak-to-peak value)						
(R-Y)	4,4 MHz	$V_{30(p-p)}$	–	–	*	mV
(R-Y)	8,8 MHz + harmonics	$V_{30(p-p)}$	–	–	*	mV
(B-Y)	4,4 MHz	$V_{31(p-p)}$	–	–	*	mV
(B-Y)	8,8 MHz + harmonics	$V_{31(p-p)}$	–	–	*	mV
H/2 ripple voltage at (R-Y) outputs without input signal; (peak-to-peak value)		$V_{30(p-p)}$	–	–	50	mV
Change in colour difference amplitudes with temperature		$\Delta V/\Delta T$	–	0,1	–	%/K
with supply voltage; (10%)		$\Delta V/\Delta V$	–	–	0,1	dB
Hue control	via I^2C bus					
Phase shift variation		φ	–	0±50	–	deg
		$\Delta\varphi$	–	–	5	deg
Hue control curve	see Fig. 6					
Sandcastle pulse 1 (pin 7)						
Detection level for:						
vertical blanking		V_7	1,0	1,5	2,0	V
horizontal blanking		V_7	3,0	3,5	4,0	V
burst key pulse		V_7	6,5	7,0	2,0	V
Input current (pin 7)						
0,5 to 1,5 V		V_7	–	–	–0,5	mA
1,5 to 7,0 V		V_7	–	–16,0	–	μA
7,0 to 12,0 V		V_7	–	–0,1	–	μA

* Value to be fixed.

parameter	condition	symbol	min.	typ.	max.	unit
Frequency doubler output (pin 34)						
Output signal voltage; (peak-to-peak value)	PAL/NTSC	$V_{34(p-p)}$	–	350	–	mV
Output impedance		Z_O	–	50	–	Ω
DC output level						
PAL		V_{34}	–	4,9	–	V
NTSC		V_{34}	–	7,0	–	V
NTSC information (pin 1)						
Output voltage level:						
on identification of NTSC 3,58 MHz		V_1	–	8,0	–	V
other modes		V_1	–	2,0	–	V
Output impedance		Z_O	–	–	500	Ω
ACC reference (pin 38)						
DC level		V_{38}	–	7,3	–	V
Scan switch output (pin 40)	open collector					
Clamp scan level		V_{40}	–	0,1	–	V
Input leakage current at signal identification		I_{LI}	–	5,0	–	μA
Luminance input (pin 29)						
Input voltage (peak-to-peak value)	note 6	$V_{29(p-p)}$	–	0,45	–	V
Pre-clipping input voltage		V_{29}	–	–	0,9	V
Input current		I_{29}	–	0,1	1,0	μA
Frequency response of total luminance and amplifier circuits	0 to 12 MHz		–	–3	–	dB
Colour difference input signals						
Input signal amplitude						
(R-Y) (pin 25)		V_{25}	–	0,62	–	V
(B-Y) (pin 26)		V_{26}	–	0,8	–	V
Colour difference input currents (pins 25 and 26)		$I_{25,26}$	–	0,1	1,0	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
RGB inputs (pins 19, 22 and 23)						
Input signal amplitude (peak-to-peak value)	note 7	$V_{19,22,23(p-p)}$	–	0,7	–	V
Δ Black level	note 8	$\Delta V_{19,22,23}$	–	–	*	V
Frequency response of RGB/Teletext amplifier	0 to 12 MHz		–	–2	–	dB
Delay difference	3 channels	t_d	–	0	–	ns
Input current		$I_{19,22,23}$	–	–	10	μA
Video switching (pin 13)						
Input voltage	no signal insertion	V_{13}	–	–	0,3	V
Input voltage	signal insertion note 9	V_{13}	0,9	–	3,0	V
Delay of switching		t_d	–	–	50	ns
Input resistance		R_{13}	–	10	–	kΩ
Suppression of internal RGB signal	when $V_{13} > 0{,}9$ V, 0 - 5 MHz		46	–	–	dB
Suppression of external RGB signals	when $V_{13} < 0{,}3$ V, 0 - 5 MHz		*	–	–	dB
Sandcastle pulse 2 (pin 12)						
Detection level for:						
vertical blanking		V_{12}	1,0	1,5	2,0	V
horizontal blanking		V_{12}	3,0	3,5	4,0	V
upper part of pulse		V_{12}	6,5	7,0	7,5	V

* Value to be fixed.

DEVELOPMENT DATA

parameter	condition	symbol	min.	typ.	max.	unit
Input current						
0 to 1,5 V		I_{12}	–	–	–0,5	mA
1,5 to 3,5 V		I_{12}	–	–16,0	–	μA
3,5 to 7,0 V		I_{12}	–	–5,0	–	μA
7,0 to 12,0 V		I_{12}	–	–0,1	–	μA
Saturation control	via I²C bus					
Saturation control range		G	50	–	–	dB
Saturation control curve	see Fig. 7					
Contrast control	via I²C bus					
Contrast control range	note 10	G	–	20	–	dB
Tracking of contrast control range between three channels	over 10 dB range		–	–	0,5	dB
Contrast control curve	see Fig. 8					
Brightness control	via I²C bus					
Brightness control voltage	note 14; at nominal white point adjustment		–	2,0	–	V
Brightness control curve	see Fig. 9					
White point adjustment (WPA)	via I²C bus					
Control range		CR	–	8	–	dB
		ΔCR	–	–	1	dB
Peak white limiting (PWL)	via I²C bus					
Control range	nominal WPA		5,0	–	10	V
Colour difference matrices						
PAL mode	(R-Y), (B-Y) not affected					
(G-Y)/(R-Y)			–	–0,51	–	
(G-Y)/(B-Y)			–	–0,19	–	
NTSC mode	(B-Y) not affected					
(R-Y)'/(R-Y)			–	+ 1,57	–	
(R-Y)'/(B-Y)			–	–0,41	–	
(G-Y)/(R-Y)			–	–0,43	–	
(G-Y)/(B-Y)			–	–0,11	–	

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
RGB amplifiers						
Output signal amplitude (peak-to-peak value)	note 11	$V_{18,20,21\ (p\text{-}p)}$	–	4,0	–	V
Output signal amplitude for blue channel (peak-to-peak value)	note 12	$V_{20(p\text{-}p)}$	–	5,4	–	V
Maximum peak white level		$V_{18,20,21\ (p\text{-}p)}$	–	10,5	–	V
Available output current		$I_{18,20,21}$	10	–	–	mA
Difference in black level between three channels	note 13; at nominal brightness and nominal WPA	$\Delta V_{18,20,21}$	–	–	10	mV
Delay between leading edges of sandcastle upper part and black level clamping pulse		t_d	–	*	–	μs
Control range of black current stabilization	V_{black} = 3 V; nominal brightness and nominal WPA		–	–	± 2	V
Black level shift with picture content			–	–	40	mV
Output voltage during the 4L pulse after switch-on		$V_{18,20,21}$	7,5	–	–	V
Variation of black level with temperature		$\Delta V/\Delta T$	–	0	–	mV/K
with contrast control	+3 to −17 dB note 14; at nominal saturation and WPA	ΔV	–	–	*	mV

* Value to be fixed.

DEVELOPMENT DATA

parameter	condition	symbol	min.	typ.	max.	unit
Relative spread between the R, G and B output signals			–	–	10	%
Relative black level variation between the three channels during variation of supply voltage (± 10%) at nominal controls	note 14		–	0	*	mV
contrast	(20 dB) at nominal saturation and WPA		–	–	*	mV
saturation	(50 dB) at nominal contrast and WPA		–	–	*	mV
brightness	(± 1 V) at nominal controls		–	–	*	mV
Differential drift of the black level	over range of 40 K; note 14		–	0	20	mV
Blanking level at the RGB outputs			–	1,0	–	V
Difference in blanking level of the three channels			–	0	10	mV
Differential drift of the blanking levels	over range of 40 K		–	0	10	mV
Tracking of output black levels with supply voltage		$\frac{\Delta V_{bl} \times V_p}{V_{bl} \times \Delta V_p}$	0,9	1,0	1,1	
Signal to noise ratio of output signals	note 5	S/N	*	–	–	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)			–	–	*	mV
Residual 8,8 MHz signal at RGB outputs (peak-to-peak value)			–	–	*	mV
Output impedance		$Z_{18,20,21}$	–	50	–	Ω
Current source of output stage			–	2,5	–	mA

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Black current stabilization						
DC bias voltage (pin 14)		V_{14}	3,5	5,0	7,0	V
Difference between input voltage for black current and leakage current		ΔV	0,35	0,5	0,65	V
Input current during:						
black current		I_{14}	–	–	1,0	μA
scan		I_{14}	–	–	10	mA
Internal limiting level (pin 14)		V_{14}	8,5	9,0	9,5	V
Switching threshold for black current control ON		V_{14}	7,6	8,0	8,4	V
Input resistance during scan (pin 14)		R_{14}	1,0	1,5	2,0	kΩ
DC input current during scan of clamping inputs (pins 24, 16 and 17)		$I_{24,16,17}$	–	–	50	nA
Maximum charge/discharge current during measuring time of clamping pulse (pins 24, 16 and 17)		$I_{c/d}$	0,5	–	–	mA
Beam current limiter (BCL) (pin 28)						
Voltage when BCL or PWL function is inactive	note 15	V_{28}	5,0	–	–	V
Trigger level for BCL or PWL function		V_{28}	–	4,2	–	V
I^2C BUS INTERFACE						
I/O interface (pin 36)	note 16					
DAC output (pin 37)						
Control range of output voltage		V_O	0,5	–	10,0	V
Output impedance		Z_O	–	100	–	Ω
Drive output for CVBS switch (pin 39)						
Output voltage LOW		V_{OL}	–	–	1	V
Output voltage HIGH		V_{OH}	10	–	–	V
Output current HIGH	note 17	I_{OH}	3	–	–	mA
Output impedance		Z_O	–	–	300	Ω

Notes to the characteristics

1. Indicated is a signal for a colour bar with 75% saturation (chroma/burst ratio of 2,2 :1).
2. All frequency variations are referred to the 3,58 MHz or 4,43 MHz carrier frequency.
3. The oscillator can run on two frequencies (i.e. when two crystals are connected to the device). Switching between the two reference frequencies is controlled internally or via the I²C bus.
4. The various modes are sequentially scanned (four field periods per mode) until a signal is identified. The voltage levels on the two detection pins in the various modes are given.
5. The ratio between wanted and unwanted signals (e.g. crosstalk, phase errors and noise) is specified as the output signal amplitude (peak-to-peak value at nominal conditions) with respect to the r.m.s. value of the unwanted signal.
6. Signal with negative going sync. Amplitude contains sync pulse amplitude.
7. For a resultant B/W output signal of 4 V, at nominal contrast and nominal white point adjustment.
8. Difference in black level between RGB signals and inserted signals.
9. For normal use, the input voltage should be 3 V maximum. (The range between 4 V and 12 V is used for testing).
10. Nominal contrast is specified as maximum contrast −3 dB. Nominal saturation as maximum saturation −6 dB; nominal white point adjustment is maximum −3 dB.
11. Nominal luminance, contrast and white point adjustment.
12. Nominal contrast, saturation control set and no (R-Y) luminance signal.
13. With respect to the measuring pulse. At nominal brightness the black level of one output is identical to the measuring level.
14. With respect to the measuring pulse.
15. Pin 28 should be externally connected to a high-resistance voltage divider. Pins 13, 19, 22 and 23 when unused, should be connected to ground via a 75 Ω (typ.) resistor.
16. See I²C bus specification.
17. Higher output currents are allowed but this will decrease V_{OH}.

DEVELOPMENT DATA

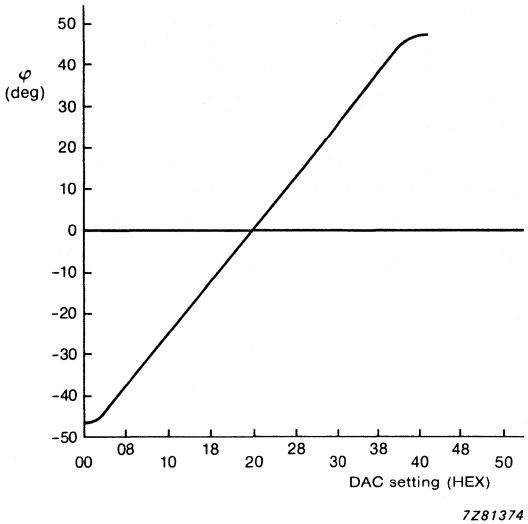


Fig. 6 Typical hue control curve.

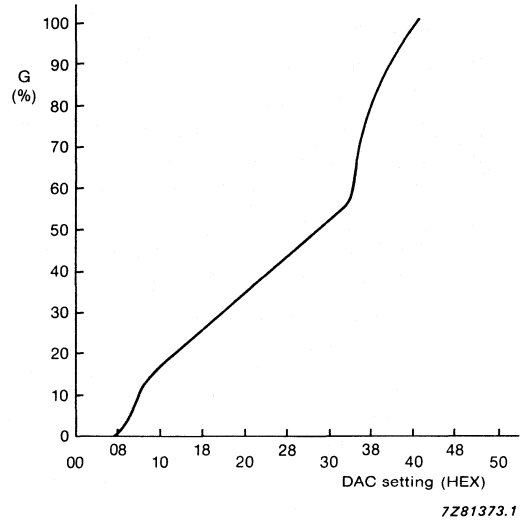


Fig. 7 Typical saturation control curve.

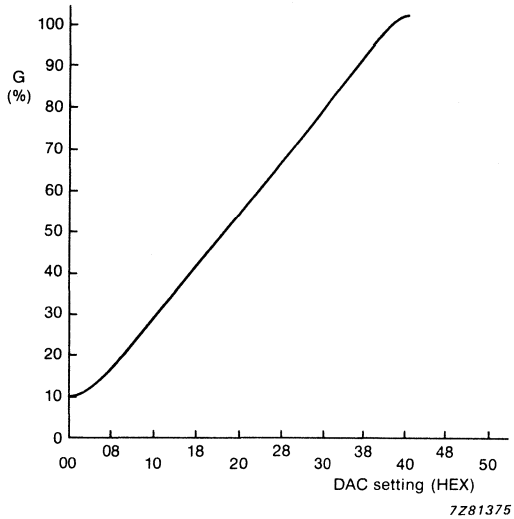


Fig. 8 Typical contrast control curve.

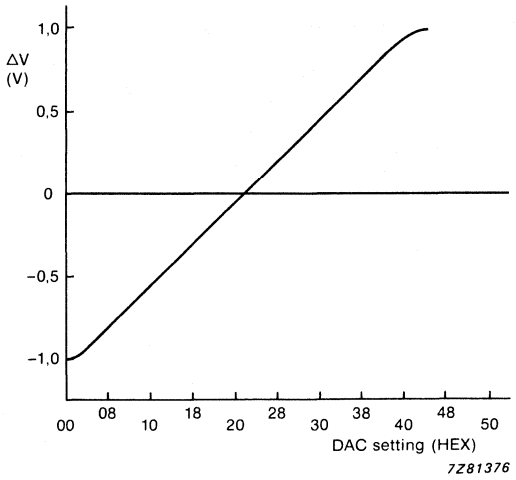


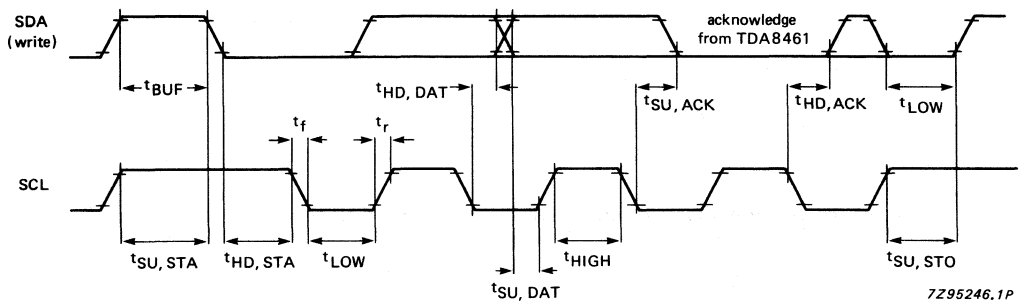
Fig. 9 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the DAC setting in hexadecimal at nominal WPA setting.

DEVELOPMENT DATA

I²C BUS TIMING (see Fig. 10)

Bus loading conditions: 4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD,STA}$	4,0	–	–	μs
LOW period SCL, SDA	t_{LOW}	4,0	–	–	μs
HIGH period SCL	t_{HIGH}	4,0	–	–	μs
Rise time SCL, SDA	t_R	–	–	1,0	μs
Fall time SCL, SDA	t_F	–	–	0,30	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from TDA8461) set-up time	$t_{SU,ACK}$	–	–	3,5	μs
Acknowledge (from TDA8461) hold time	$t_{HD,ACK}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4,0	–	–	μs



Reference levels are 10 and 90%

Fig. 10 I²C bus timing, TDA8461.

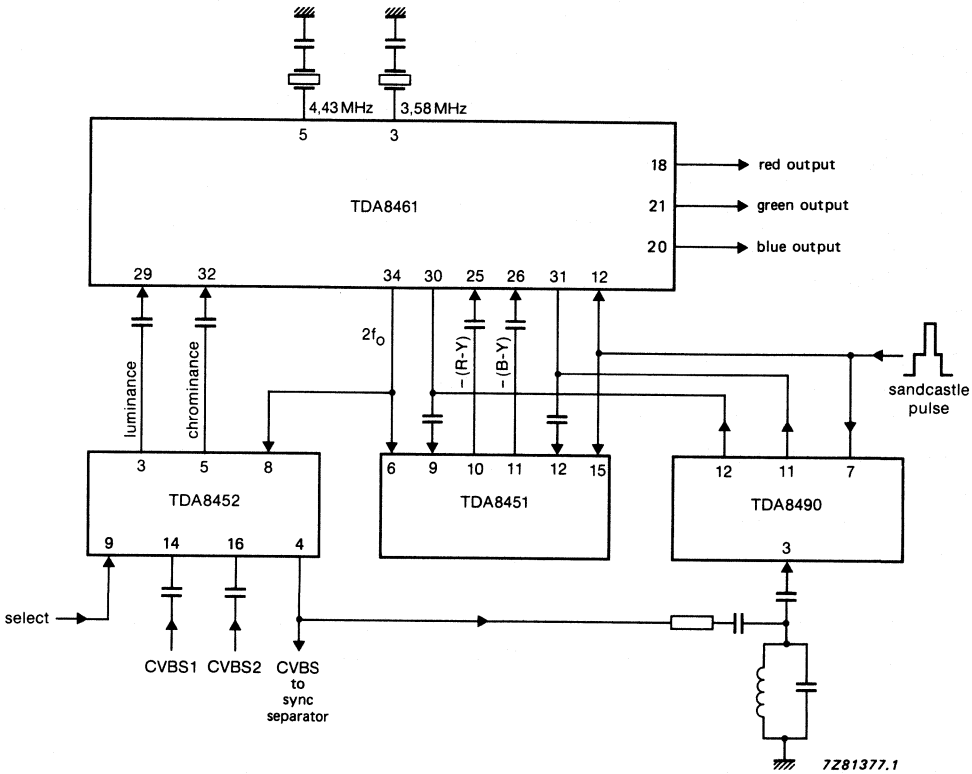


Fig. 11 Application diagram showing the complete multi-standard decoder system.

FM/IF SYSTEM
AND MICROCOMPUTER-BASED TUNING INTERFACE

GENERAL DESCRIPTION

The TEA6000 is an FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes an AM/FM-IF counter and an analogue-to-digital interface. The i.f. counter generates AM/FM precision tuning and accurate stop information.

Features

- 3-stage IF limiter for driving a ratio detector
- 2-stage level detector with current output
- operational amplifier for active filtering (e.g. multipath detector)
- high resolution frequency counter for FM and AM IF-signals
- time base reference from crystal oscillator or external source (SAA1057)
- serial two wire bidirectional computer interface (I^2C-bus)
- multiplexed 3 bit A/D converter for two input signals
- software controlled sensitivity for both ADC inputs

QUICK REFERENCE DATA

Supply voltages (V_{P1} and V_{P2})	V_P	typ.	8,4 V
Supply current; ($I_{P1} + I_{P2}$)	I_P	typ.	36 mA
FM/IF sensitivity			
at −3 dB before limiting	V_i	typ.	150 μV
Signal to noise ratio for V_i = 10 mV	S/N	typ.	80 dB
Audio output voltage			
Δf = 22,5 kHz; V_i = 1 mV	V_O	typ.	170 mV
Δf = 75 kHz; V_i = 1 mV	V_O	typ.	520 mV
AM suppression at V_i = 10 mV	AMS	typ.	58 dB
Frequency counter sensitivity			
AM (pin 18)	$V_{i(am)}$	typ.	60 μV
FM (pin 16)	$V_{i(fm)}$	typ.	80 μV
Resolution frequency counter			
AM	$f_{s(am)}$	typ.	250 Hz
FM	$f_{s(fm)}$	typ.	6,4 kHz
Power dissipation	P_{tot}	max.	1300 mW
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−30 to + 85	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

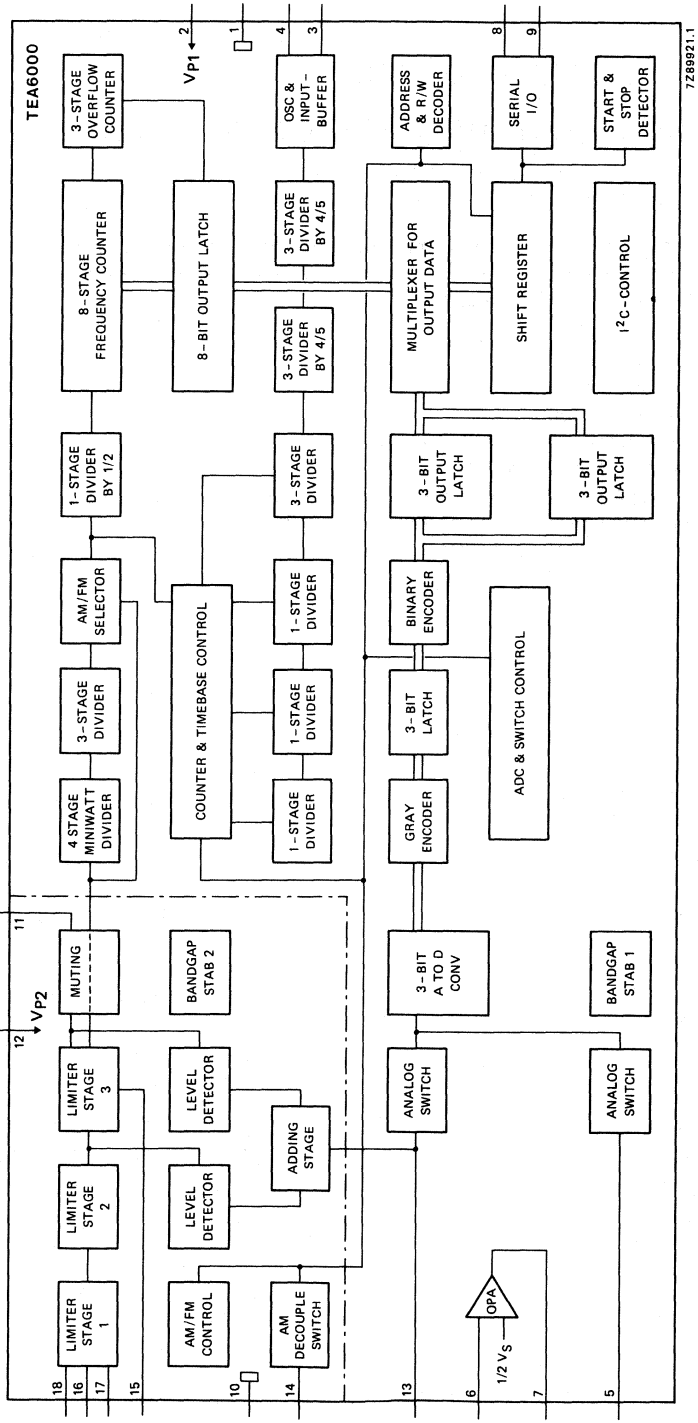


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The IF SECTION consists of three balanced differential stages with separated FM and AM inputs, directly coupled by emitter followers. The last stage also has separated outputs, which are intended for driving a ratio detector and the frequency measuring system respectively.

The last two stages are coupled via low-value capacitors to two LEVEL DETECTORS which generate a signal-dependent d.c. current for controlling channel separation and frequency response of a stereo decoder, multipath detector circuitry, AGC and the internal ADC.

The IF MUTING circuit has been incorporated to decrease the interstation noise by about 15 dB.

The 3-bit A/D CONVERTER has two inputs, which are selected via two multiplexed analogue switches. One of these switches is internally connected to the level detector output but can also serve as an external input, as the level detector output can be switched off. The outputs of the ADC are converted to a Gray code, latched and reconverted to a binary code to obtain glitch-free output data. The sensitivity of both inputs can be selected independently via software on two levels.

The reference for the ADC is derived from a BAND-GAP STABILIZER circuit. Multipath distortion on FM will generate an AM modulation on the d.c. voltage from the level detectors. This AM modulation can be filtered and rectified to obtain a multipath-dependent d.c. voltage. This voltage can be applied to the other input of the ADC.

To facilitate filtering an OPERATIONAL AMPLIFIER (OPA) is incorporated on the chip. The typical circuit diagram for a multipath filter is given in Fig. 4.

The FREQUENCY COUNTER is preceded by a 7-stage prescaler for FM, and FM/AM selector stage and a divider by 1 or 2. The actual counter is a presetable and resetable 8-stage counter with a 3-stage data disable overflow counter, which can be switched off. The eight significant output bits are situated symmetrically around 10,7 MHz and 460 kHz, when the external timebase source is used (e.g. SAA1057). See Table 1.

The reference for the TIMEBASE is primarily thought to be the SAA1057. This circuit generates from its 4 MHz crystal oscillator a 32 or 40 kHz signal. This signal is buffered and applied to the timebase circuitry (mode I). The circuit diagram for this mode I is given in Fig. 5a.
In the timebase, the selection is made for reference frequency (32 to 40 kHz), FM or AM mode and the width of the measuring window, all under software control. Accuracy ± ½ bit when the window is set to wide (see Fig. 2) and ± 1 bit when set to narrow. A special feature is the synchronization of the measuring cycle with the input DATA of the I^2C-bus, meaning the measuring cycle starts immediately after a "WRITE" instruction via the I^2C-bus.

For those who do not use the SAA1057 as reference, a 2^{15} Hz crystal (32 768 Hz) can be connected to the reference inputs directly, obtaining a quartz-oscillator reference. See Fig. 5b for the circuit diagram for this mode II.

When the circuit is used in mode II a correction has to be made to the values of window width and resolution as the cheap watch crystals differ by about 2,4% from the frequency generated by the SAA1057 (32 768 and 32 000 kHz respectively) See Table 2.

Communication between MUSTI and the microcomputer is accomplished via the two-wire bidirectional I^2C-bus (slave transceiver version); the SDA (serial data) and SCL (serial clock).

To prevent crosstalk between the digital and analogue parts of the circuit the power supply lines are fully isolated.

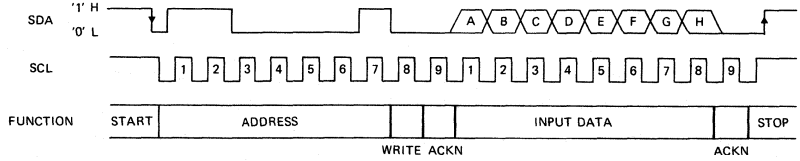


Fig. 2 Input data format waveforms.

Input bits

bit	function	"0"	"1"	reference to Fig. 2
1	reference frequency	32 kHz	40 kHz	A
2	sensitivity ADC2	LOW	HIGH	B
3	sensitivity ADC1	LOW	HIGH	C
4	level detector output	off	on	D
5	AM/FM	AM	FM	E
6	overflow counter	off	on	F
7	measuring window	narrow	wide	G
8	test mode	off	on	H

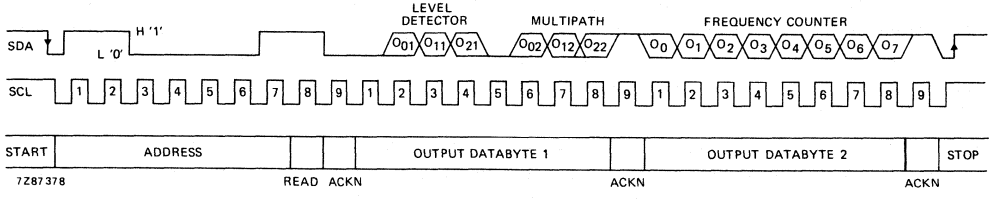


Fig. 3 Output data format waveforms.

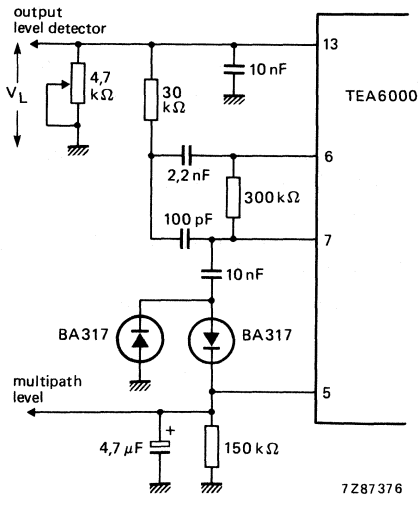


Fig. 4 Multipath detector circuit.

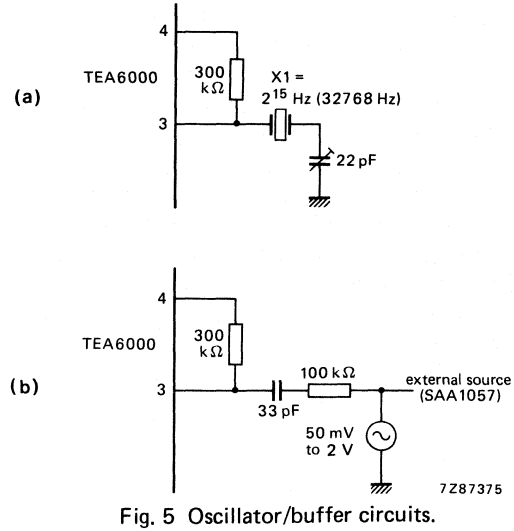


Fig. 5 Oscillator/buffer circuits.
X1 = 2^{15} Hz (32 768 Hz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
pin 2	V_{P1}	max.	13,2 V
pin 12	V_{P2}	max.	13,2 V
Power dissipation	P_{tot}	max.	1300 mW
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−30 to + 85	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c\text{-}a}$	=	50 K/W

D.C. CHARACTERISTICS

$V_{P1} = V_{P2} = 8{,}4$ V; $T_{amb} = 25$ °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
(pin 2)	V_{P1}	7,6	8,4	9,2	V
(pin 12)	V_{P2}	7,6	8,4	9,2	V
Supply current AM mode					
pin 2	I_{P1}	–	18,5	–	mA
pin 12	I_{P2}	–	17,4	–	mA
Supply current FM mode					
pin 2	I_{P1}	–	19,2	–	mA
pin 12	I_{P2}	–	16,4	–	mA
Power dissipation	P_{tot}	–	350	–	mW

A.C. CHARACTERISTICS (see Fig. 6)

$V_{P1} = V_{P2} = 8{,}4$ V; $V_{16\text{-}10} = 1$ mV; f = 10,7 MHz; $\Delta f = 22{,}5$ kHz; $f_m = 1$ kHz; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity					
at −3 dB before limiting	$V_{I(FM)}$	–	150	–	μV
Signal-to-noise ratio, FM input					
V_i = 20 μV	S/N	40	46	–	dB
V_i = 150 μV	S/N	–	64	–	dB
V_i = 1 mV	S/N	–	76	–	dB
V_i = 10 mV	S/N	–	80	–	dB
Noise output voltage					
V_i = 0 V; with muting, switch S1 on	V_{no}	–	55	–	μV
V_i = 0 V; without muting, S1 off	V_{no}	–	420	–	μV
Audio output voltage					
Δf = 22,5 kHz	V_O	–	170	–	mV
Δf = 75 kHz	V_O	–	520	–	mV

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
AM suppression					
ratio of the AM output signal referred to the FM signal (m = 0,3)					
V_i = 150 μV	AMS	–	46	–	dB
V_i = 1 mV	AMS	–	62	–	dB
V_i = 10 mV	AMS	–	58	–	dB
V_i = 100 mV	AMS	–	60	–	dB
Level detector output voltage (Fig. 4)					
$R_{13\text{-}10}$ = 4,7 kΩ; V_i = 10 mV, FM mode	V_L	–	6,2	–	V
Level detector output voltage slope					
$R_{13\text{-}10}$ adjusted in FM mode for V_L = 5,5 V at V_i = 10 mV; f = 10,7 MHz					
V_i = 0 V (pin 16)	$V_{L(FM)}$	–	130	–	mV
V_i = 140 μV	$V_{L(FM)}$	–	1,3	–	V
V_i = 1 mV	$V_{L(FM)}$	–	2,7	–	V
V_i = 3 mV	$V_{L(FM)}$	–	4,4	–	V
$R_{13\text{-}10}$ adjusted in FM mode (see above)					
V_i = 0 V, f = 460 kHz (pin 18)	$V_{L(AM)}$	–	200	–	mV
V_i = 1 mV, f = 460 kHz (pin 18)	$V_{L(AM)}$	–	1,4	–	V
V_i = 10 mV, f = 460 kHz (pin 18)	$V_{L(AM)}$	–	2,7	–	V
Frequency counter sensitivity					
AM input voltage (pin 18)	$V_{I(AM)}$	–	60	–	μV
FM input voltage (pin 16)	$V_{I(FM)}$	–	80	–	μV
AM input impedance	R_i	–	30	–	kΩ
BUS inputs					
SDA and SCL (pins 9 and 8)					
input voltage HIGH	V_{IH}	3,0	–	V_{P1}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	10	μA
input current LOW	I_{IL}	–	–	10	μA
acknowledge sink current	I_{ack}	–	–	2	mA
maximum input frequency	$f_{i\ max}$	100	–	–	kHz
Output voltage SDA					
HIGH; 4 kΩ to 8,4 V	V_{OH}	8,0	–	–	V
LOW; I = 2 mA	V_{OL}	–	–	0,4	V

parameter	symbol	min.	typ.	max.	unit
A/D converter (pin 5 and 13)					
input resistance	R_i		t.b.f.		kΩ
input capacitance	C_i		t.b.f.		pF
Trip levels, sensitivity bit HIGH					
level 1	V_T	–	0,6	–	V
level 2	V_T	–	1,06	–	V
level 3	V_T	–	1,38	–	V
level 4	V_T	–	1,84	–	V
level 5	V_T	–	2,14	–	V
level 6	V_T	–	2,55	–	V
level 7	V_T	–	2,97	–	V
Trip levels, sensitivity bit LOW					
level 1	V_T	–	0,96	–	V
level 2	V_T	–	1,78	–	V
level 3	V_T	–	2,44	–	V
level 4	V_T	–	3,26	–	V
level 5	V_T	–	3,92	–	V
level 6	V_T	–	4,63	–	V
level 7	V_T	–	5,38	–	V
Crystal oscillator (see Fig. 5)					
reference frequency	f_{ref}	32	32,768	40	kHz
temperature coefficient	TC		t.b.f.		10^{-6}
input resistance	R_i		t.b.f.		kΩ
input capacitance	C_i		t.b.f.		pF
Operational amplifier (pins 6 and 7)					
voltage gain	G_V	–	10^4	–	
input bias current	I_{bias}	–	30	100	nA
output sink current at V_O = 1 V	I_O	–	0,2	–	mA
output source current at V_O = 7,4 V	I_O	5,5	10	–	mA
output voltage swing	$V_{7(p-p)}$	–	5,5	–	V
Frequency measuring system (see pages 8 and 9)					
measuring windows; f_{ref} = 32 or 40 kHz					
AM					
window "0" (LOW)	t_{gate}	–	4	–	ms
window "1" (HIGH)	t_{gate}	–	8	–	ms
FM					
window "0" (LOW)	t_{gate}	–	20	–	ms
window "1" (HIGH)	t_{gate}	–	40	–	ms
resolution frequency counter					
AM	$f_{s(am)}$	–	250	–	Hz
FM	$f_{s(fm)}$	–	6,4	–	kHz

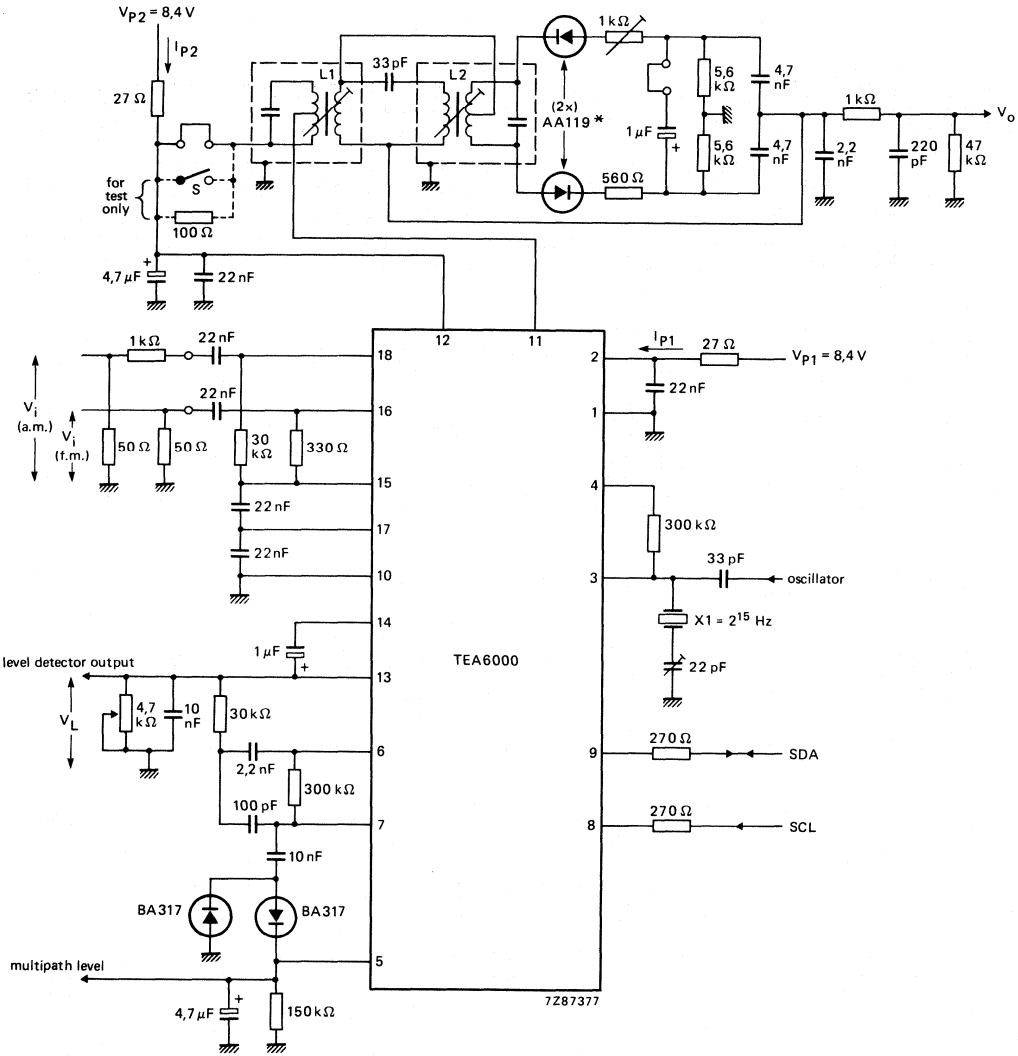
t_{gate} has to be multiplied by 32 000/32 768 for a f_{ref} of 2^{15} Hz.
f_s has to be multiplied by 32 768/32 000 for a f_{ref} of 2^{15} Hz.

TABLE 1 REFERENCE FREQUENCY 32 000 Hz (SAA1057)

AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)
428.25	'00'	9.888	441.00	'33'	10.214	453.75	'66'	10.541	466.50	'99'	10.867	479.25	'CC'	11.194
428.50	'01'	9.894	441.25	'34'	10.221	454.00	'67'	10.547	466.75	'9A'	10.874	479.50	'CD'	11.200
428.75	'02'	9.901	441.50	'35'	10.227	454.25	'68'	10.554	467.00	'9B'	10.880	479.75	'CE'	11.206
429.00	'03'	9.907	441.75	'36'	10.234	454.50	'69'	10.560	467.25	'9C'	10.886	480.00	'CF'	11.213
429.25	'04'	9.914	442.00	'37'	10.240	454.75	'6A'	10.566	467.50	'9D'	10.893	480.25	'D0'	11.219
429.50	'05'	9.920	442.25	'38'	10.246	455.00	'6B'	10.573	467.75	'9E'	10.899	480.50	'D1'	11.226
429.75	'06'	9.926	442.50	'39'	10.253	455.25	'6C'	10.579	468.00	'9F'	10.906	480.75	'D2'	11.232
430.00	'07'	9.933	442.75	'3A'	10.259	455.50	'6D'	10.586	468.25	'A0'	10.912	481.00	'D3'	11.238
430.25	'08'	9.939	443.00	'3B'	10.266	455.75	'6E'	10.592	468.50	'A1'	10.918	481.25	'D4'	11.245
430.50	'09'	9.946	443.25	'3C'	10.272	456.00	'6F'	10.598	468.75	'A2'	10.925	481.50	'D5'	11.251
430.75	'0A'	9.952	443.50	'3D'	10.278	456.25	'70'	10.605	469.00	'A3'	10.931	481.75	'D6'	11.258
431.00	'0B'	9.958	443.75	'3E'	10.285	456.50	'71'	10.611	469.25	'A4'	10.938	482.00	'D7'	11.264
431.25	'0C'	9.965	444.00	'3F'	10.291	456.75	'72'	10.618	469.50	'A5'	10.944	482.25	'D8'	11.270
431.50	'0D'	9.971	444.25	'40'	10.298	457.00	'73'	10.624	469.75	'A6'	10.950	482.50	'D9'	11.277
431.75	'0E'	9.978	444.50	'41'	10.304	457.25	'74'	10.630	470.00	'A7'	10.957	482.75	'DA'	11.283
432.00	'0F'	9.984	444.75	'42'	10.310	457.50	'75'	10.637	470.25	'A8'	10.963	483.00	'DB'	11.290
432.25	'10'	9.990	445.00	'43'	10.317	457.75	'76'	10.643	470.50	'A9'	10.970	483.25	'DC'	11.296
432.50	'11'	9.997	445.25	'44'	10.323	458.00	'77'	10.650	470.75	'AA'	10.976	483.50	'DD'	11.302
432.75	'12'	10.003	445.50	'45'	10.330	458.25	'78'	10.656	471.00	'AB'	10.982	483.75	'DE'	11.309
433.00	'13'	10.010	445.75	'46'	10.336	458.50	'79'	10.662	471.25	'AC'	10.989	484.00	'DF'	11.315
433.25	'14'	10.016	446.00	'47'	10.342	458.75	'7A'	10.669	471.50	'AD'	10.995	484.25	'E0'	11.322
433.50	'15'	10.022	446.25	'48'	10.349	459.00	'7B'	10.675	471.75	'AE'	11.002	484.50	'E1'	11.328
433.75	'16'	10.029	446.50	'49'	10.355	459.25	'7C'	10.682	472.00	'AF'	11.008	484.75	'E2'	11.334
434.00	'17'	10.035	446.75	'4A'	10.362	459.50	'7D'	10.688	472.25	'B0'	11.014	485.00	'E3'	11.341
434.25	'18'	10.042	447.00	'4B'	10.368	459.75	'7E'	10.694	472.50	'B1'	11.021	485.25	'E4'	11.347
434.50	'19'	10.048	447.25	'4C'	10.374	460.00	'7F'	10.701	472.75	'B2'	11.027	485.50	'E5'	11.354
434.75	'1A'	10.054	447.50	'4D'	10.381	460.25	'80'	10.707	473.00	'B3'	11.034	485.75	'E6'	11.360
435.00	'1B'	10.061	447.75	'4E'	10.387	460.50	'81'	10.714	473.25	'B4'	11.040	486.00	'E7'	11.366
435.25	'1C'	10.067	448.00	'4F'	10.394	460.75	'82'	10.720	473.50	'B5'	11.046	486.25	'E8'	11.373
435.50	'1D'	10.074	448.25	'50'	10.400	461.00	'83'	10.726	473.75	'B6'	11.053	486.50	'E9'	11.379
435.75	'1E'	10.080	448.50	'51'	10.406	461.25	'84'	10.733	474.00	'B7'	11.059	486.75	'EA'	11.386
436.00	'1F'	10.086	448.75	'52'	10.413	461.50	'85'	10.739	474.25	'B8'	11.066	487.00	'EB'	11.392
436.25	'20'	10.093	449.00	'53'	10.419	461.75	'86'	10.746	474.50	'B9'	11.072	487.25	'EC'	11.398
436.50	'21'	10.099	449.25	'54'	10.426	462.00	'87'	10.752	474.75	'BA'	11.078	487.50	'ED'	11.405
436.75	'22'	10.106	449.50	'55'	10.432	462.25	'88'	10.758	475.00	'BB'	11.085	487.75	'EE'	11.411
437.00	'23'	10.112	449.75	'56'	10.438	462.50	'89'	10.765	475.25	'BC'	11.091	488.00	'EF'	11.418
437.25	'24'	10.118	450.00	'57'	10.445	462.75	'8A'	10.771	475.50	'BD'	11.098	488.25	'F0'	11.424
437.50	'25'	10.125	450.25	'58'	10.451	463.00	'8B'	10.778	475.75	'BE'	11.104	488.50	'F1'	11.430
437.75	'26'	10.131	450.50	'59'	10.458	463.25	'8C'	10.784	476.00	'BF'	11.110	488.75	'F2'	11.437
438.00	'27'	10.138	450.75	'5A'	10.464	463.50	'8D'	10.790	476.25	'C0'	11.117	489.00	'F3'	11.443
438.25	'28'	10.144	451.00	'5B'	10.470	463.75	'8E'	10.797	476.50	'C1'	11.123	489.25	'F4'	11.450
438.50	'29'	10.150	451.25	'5C'	10.477	464.00	'8F'	10.803	476.75	'C2'	11.130	489.50	'F5'	11.456
438.75	'2A'	10.157	451.50	'5D'	10.483	464.25	'90'	10.810	477.00	'C3'	11.136	489.75	'F6'	11.462
439.00	'2B'	10.163	451.75	'5E'	10.490	464.50	'91'	10.816	477.25	'C4'	11.142	490.00	'F7'	11.469
439.25	'2C'	10.170	452.00	'5F'	10.496	464.75	'92'	10.822	477.50	'C5'	11.149	490.25	'F8'	11.475
439.50	'2D'	10.176	452.25	'60'	10.502	465.00	'93'	10.829	477.75	'C6'	11.155	490.50	'F9'	11.482
439.75	'2E'	10.182	452.50	'61'	10.509	465.25	'94'	10.835	478.00	'C7'	11.162	490.75	'FA'	11.488
440.00	'2F'	10.189	452.75	'62'	10.515	465.50	'95'	10.842	478.25	'C8'	11.168	491.00	'FB'	11.494
440.25	'30'	10.195	453.00	'63'	10.522	465.75	'96'	10.848	478.50	'C9'	11.174	491.25	'FC'	11.501
440.50	'31'	10.202	453.25	'64'	10.528	466.00	'97'	10.854	478.75	'CA'	11.181	491.50	'FD'	11.507
440.75	'32'	10.208	453.50	'65'	10.534	466.25	'98'	10.861	479.00	'CB'	11.187	491.75	'FE'	11.514

TABLE 2 REFERENCE FREQUENCY 32 768 Hz (2^{15} Hz)

AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (HMz)	AM (kHz)	READ OUT	FM (MHz)
438.53	'00'	10.125	451.58	'33'	10.460	464.64	'66'	10.794	477.70	'99'	11.128	490.75	'CC'	11.462
438.78	'01'	10.132	451.84	'34'	10.466	464.90	'67'	10.800	477.95	'9A'	11.135	491.01	'CD'	11.469
439.04	'02'	10.138	452.10	'35'	10.473	465.15	'68'	10.807	478.21	'9B'	11.141	491.26	'CE'	11.475
439.30	'03'	10.145	452.35	'36'	10.479	465.41	'69'	10.813	478.46	'9C'	11.148	491.52	'CF'	11.482
439.55	'04'	10.152	452.61	'37'	10.486	465.66	'6A'	10.820	478.72	'9D'	11.154	491.78	'D0'	11.488
439.81	'05'	10.158	452.86	'38'	10.492	465.92	'6B'	10.827	478.98	'9E'	11.161	492.03	'D1'	11.495
440.06	'06'	10.165	453.12	'39'	10.499	466.18	'6C'	10.833	479.23	'9F'	11.167	492.29	'D2'	11.502
440.32	'07'	10.171	453.38	'3A'	10.505	466.43	'6D'	10.840	479.49	'A0'	11.174	492.54	'D3'	11.508
440.58	'08'	10.178	453.63	'3B'	10.512	466.69	'6E'	10.846	479.74	'A1'	11.180	492.80	'D4'	11.515
440.83	'09'	10.184	453.89	'3C'	10.519	466.94	'6F'	10.853	480.00	'A2'	11.187	493.06	'D5'	11.521
441.09	'0A'	10.191	454.14	'3D'	10.525	467.20	'70'	10.859	480.26	'A3'	11.194	493.31	'D6'	11.528
441.34	'0B'	10.197	454.40	'3E'	10.532	467.46	'71'	10.866	480.51	'A4'	11.200	493.57	'D7'	11.534
441.60	'0C'	10.204	454.66	'3F'	10.538	467.71	'72'	10.872	480.77	'A5'	11.207	493.82	'D8'	11.541
441.86	'0D'	10.211	454.91	'40'	10.545	467.97	'73'	10.879	481.02	'A6'	11.213	494.08	'D9'	11.547
442.11	'0E'	10.217	455.17	'41'	10.551	468.22	'74'	10.886	481.28	'A7'	11.220	494.34	'DA'	11.554
442.37	'0F'	10.224	455.42	'42'	10.558	468.48	'75'	10.892	481.54	'A8'	11.226	494.59	'DB'	11.561
442.62	'10'	10.230	455.68	'43'	10.564	468.74	'76'	10.899	481.79	'A9'	11.233	494.85	'DC'	11.567
442.88	'11'	10.237	455.94	'44'	10.571	468.99	'77'	10.905	482.05	'AA'	11.239	495.10	'DD'	11.574
443.14	'12'	10.243	456.19	'45'	10.578	469.25	'78'	10.912	482.30	'AB'	11.246	495.36	'DE'	11.580
443.39	'13'	10.250	456.45	'46'	10.584	469.50	'79'	10.918	482.56	'AC'	11.253	495.62	'DF'	11.587
443.65	'14'	10.256	456.70	'47'	10.591	469.76	'7A'	10.925	482.82	'AD'	11.259	495.87	'E0'	11.593
443.90	'15'	10.263	456.96	'48'	10.597	470.02	'7B'	10.931	483.07	'AE'	11.266	496.13	'E1'	11.600
444.16	'16'	10.269	457.22	'49'	10.604	470.27	'7C'	10.938	483.33	'AF'	11.272	496.38	'E2'	11.606
444.42	'17'	10.276	457.47	'4A'	10.610	470.53	'7D'	10.945	483.58	'B0'	11.279	496.64	'E3'	11.613
444.67	'18'	10.283	457.73	'4B'	10.617	470.78	'7E'	10.951	483.84	'B1'	11.285	496.90	'E4'	11.620
444.93	'19'	10.289	457.98	'4C'	10.623	471.04	'7F'	10.958	484.10	'B2'	11.292	497.15	'E5'	11.626
445.18	'1A'	10.296	458.24	'4D'	10.630	471.30	'80'	10.964	484.35	'B3'	11.298	497.41	'E6'	11.633
445.44	'1B'	10.302	458.50	'4E'	10.636	471.55	'81'	10.971	484.61	'B4'	11.305	497.66	'E7'	11.639
445.70	'1C'	10.309	458.75	'4F'	10.643	471.81	'82'	10.977	484.86	'B5'	11.312	497.92	'E8'	11.646
445.95	'1D'	10.315	459.01	'50'	10.650	472.06	'83'	10.984	485.12	'B6'	11.318	498.18	'E9'	11.652
446.21	'1E'	10.322	459.26	'51'	10.656	472.32	'84'	10.990	485.38	'B7'	11.325	498.43	'EA'	11.659
446.46	'1F'	10.328	459.52	'52'	10.663	472.58	'85'	10.997	485.63	'B8'	11.331	498.69	'EB'	11.665
446.72	'20'	10.335	459.78	'53'	10.669	472.83	'86'	11.003	485.89	'B9'	11.338	498.94	'EC'	11.672
446.98	'21'	10.342	460.03	'54'	10.676	473.09	'87'	11.010	486.14	'BA'	11.344	499.20	'ED'	11.679
447.23	'22'	10.348	460.29	'55'	10.682	473.34	'88'	11.017	486.40	'BB'	11.351	499.46	'EE'	11.685
447.49	'23'	10.355	460.54	'56'	10.689	473.60	'89'	11.023	486.66	'BC'	11.357	499.71	'EF'	11.692
447.74	'24'	10.361	460.80	'57'	10.695	473.86	'8A'	11.030	486.91	'BD'	11.364	499.97	'F0'	11.698
448.00	'25'	10.368	461.06	'58'	10.702	474.11	'8B'	11.036	487.17	'BE'	11.370	500.22	'F1'	11.705
448.26	'26'	10.374	461.31	'59'	10.709	474.37	'8C'	11.043	487.42	'BF'	11.377	500.48	'F2'	11.711
448.51	'27'	10.381	461.57	'5A'	10.715	474.62	'8D'	11.049	487.68	'C0'	11.384	500.74	'F3'	11.718
448.77	'28'	10.387	461.82	'5B'	10.722	474.88	'8E'	11.056	487.94	'C1'	11.390	500.99	'F4'	11.724
449.02	'29'	10.394	462.08	'5C'	10.728	475.14	'8F'	11.062	488.19	'C2'	11.397	501.25	'F5'	11.731
449.28	'2A'	10.401	462.34	'5D'	10.735	475.39	'90'	11.069	488.45	'C3'	11.403	501.50	'F6'	11.737
449.54	'2B'	10.407	462.59	'5E'	10.741	475.65	'91'	11.076	488.70	'C4'	11.410	501.76	'F7'	11.744
449.79	'2C'	10.414	462.85	'5F'	10.748	475.90	'92'	11.082	488.96	'C5'	11.416	502.02	'F8'	11.751
450.05	'2D'	10.420	463.10	'60'	10.754	476.16	'93'	11.089	489.22	'C6'	11.423	502.27	'F9'	11.757
450.30	'2E'	10.427	463.36	'61'	10.761	476.42	'94'	11.095	489.47	'C7'	11.429	502.53	'FA'	11.764
450.56	'2F'	10.433	463.62	'62'	10.768	476.67	'95'	11.102	489.73	'C8'	11.436	502.78	'FB'	11.770
450.82	'30'	10.440	463.87	'63'	10.774	476.93	'96'	11.108	489.98	'C9'	11.443	503.04	'FC'	11.777
451.07	'31'	10.446	464.13	'64'	10.781	477.18	'97'	11.115	490.24	'CA'	11.449	503.30	'FD'	11.783
451.33	'32'	10.453	464.38	'65'	10.787	477.44	'98'	11.121	490.50	'CB'	11.456	503.55	'FE'	11.790



L1 = 3122 138 2021/TOKO 85 ACS-4238 A
L2 = 3122 138 2022/TOKO 85 ACS-4260 SEJ

Fig. 6 MUSTI test and application circuit.
Germanium diodes AA119 are required in the test circuit only.
In a complete FM channel (inclusive FM front end) the silicon diodes BA281 are recommended.

S open = without muting
S closed = with muting
} for measuring purpose only.

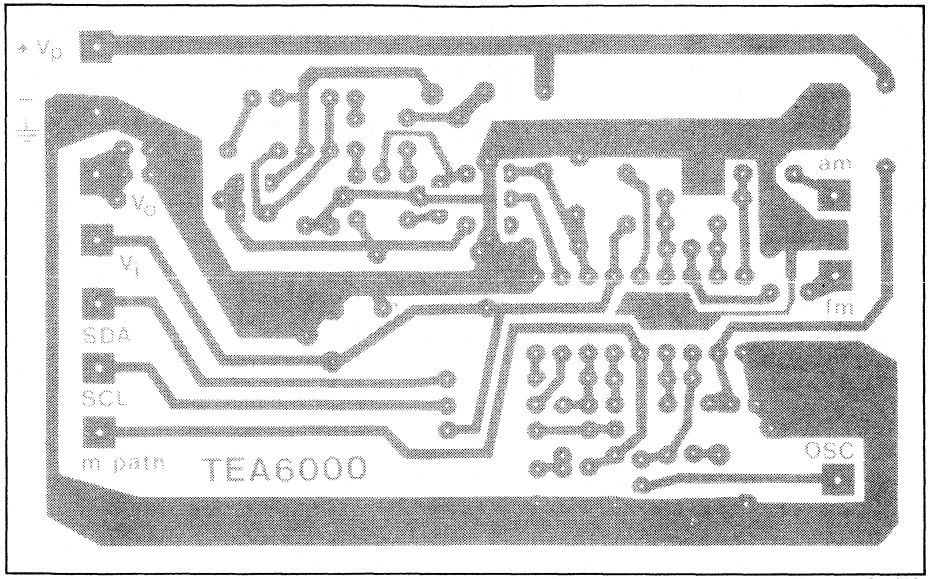


Fig. 7 Track side of printed-circuit board.

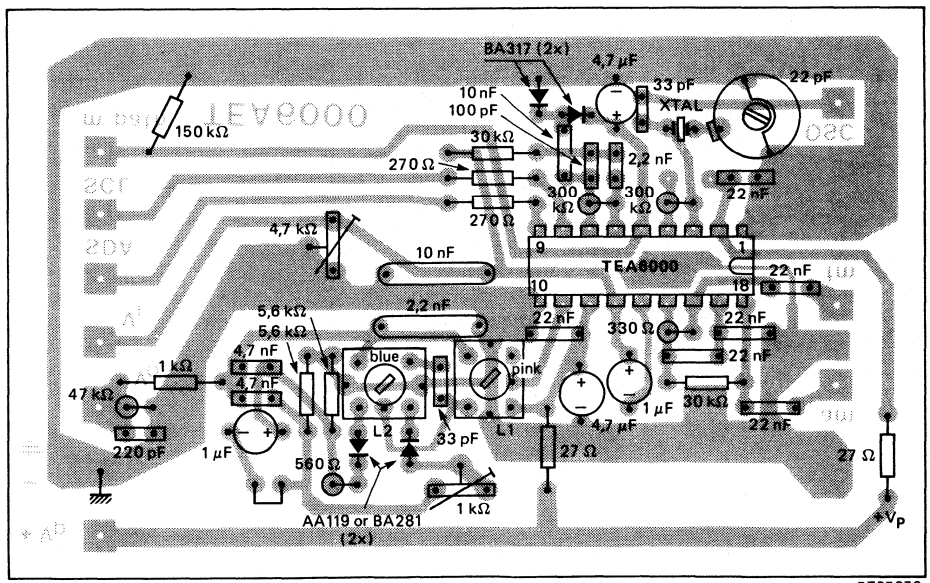


Fig. 8 Component side of printed-circuit board.

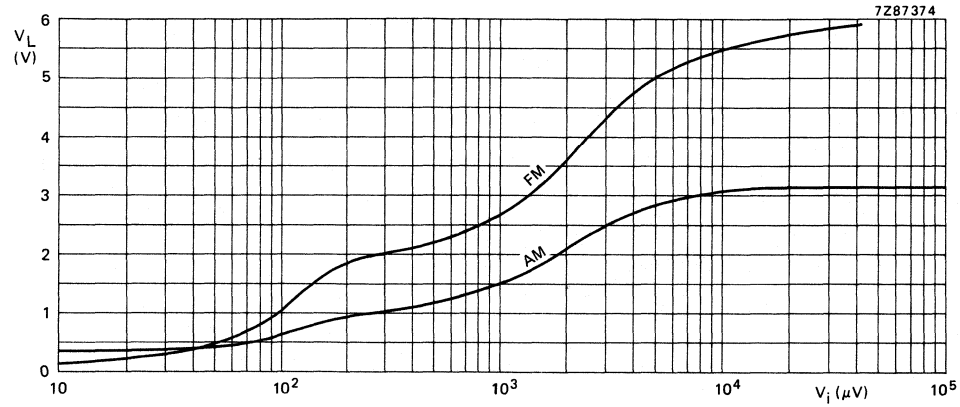


Fig. 9 Level detector output as a function of input voltage.

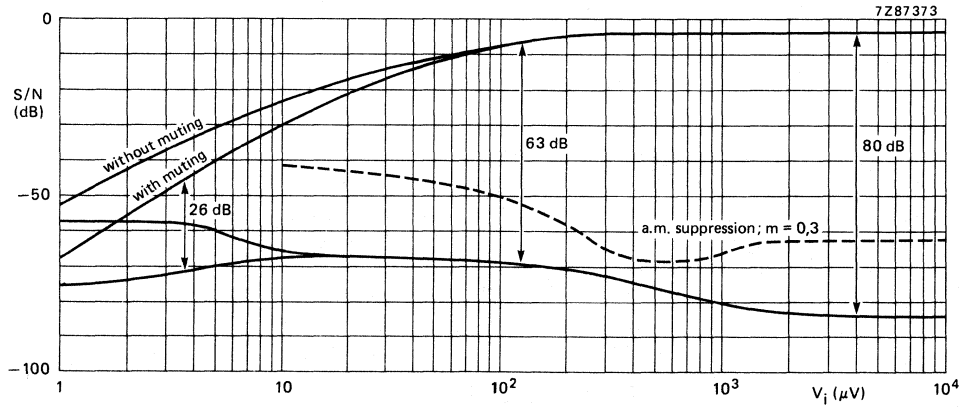


Fig. 10 Signal-to-noise ratio as a function of FM input voltage.
f_i = 10,7 MHz; Δf = 22,5 kHz; f_{mod} = 1 kHz; 0 dB = 245 mV.

FM/IF SYSTEM AND MICROCOMPUTER-BASED TUNING INTERFACE

GENERAL DESCRIPTION

The TEA6100 is a FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes highly sensitive analogue circuitry. The digital circuitry, including an I^2C bus, controls the analogue circuitry and the AM/FM tuning and stop information for the microcomputer.

Features

- 4-stage symmetrical IF limiting amplifier
- Software selectable AM or FM input
- Symmetrical quadrature demodulator
- Single-ended LF output stage
- D.C. output level determined by the input signal
- Semi-adjustable AM and FM level voltage
- Multi-path detector/rectifier/amplifier circuitry
- 3-bit level information and 3-bit multi-path information
- Signal dependent 'soft' muting circuit; externally adjustable
- Reference voltage output (FM mode only)
- 8-bit AM/FM frequency counter with selectable counter resolution
- Possibility to measure the AM IF frequency at 460 kHz (250 Hz resolution) and 10,7 MHz (500 Hz resolution)
- Reference frequency can be directly connected to the reference frequency output of a frequency synthesizer (TSA6057, 40 kHz)

PACKAGE OUTLINE

20-lead DIL; plastic (SOT-146).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{P1}, V_{P2}	–	8,5	–	V
Supply current		$I_{P1} + I_{P2}$	–	35	–	mA
FM/IF sensitivity	–3 dB before limiting	V_i	–	15	–	μV
Signal plus noise to noise ratio	Δf = 75 kHz; V_I = 10 mV	(S + N)/N	–	85	–	dB
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	–	200	–	mV
AM suppression	V_{IFM} = 600 μV to 600 mV; m = 0,3	AMS	–	60	–	dB
Frequency counter sensitivity						
AM	pin 19, f = 10,7 MHz	$V_{i(AM)}$	–	45	–	μV
	f = 460 kHz	$V_{i(AM)}$	–	20	–	μV
FM	pin 18, f = 10,7 MHz	$V_{i(FM)}$	–	45	–	μV
Resolution of the frequency counter	reference frequency of 40 kHz;					
AM	IF = 460 kHz	f_s (AM)	–	250	–	Hz
	IF = 10,7 MHz	f_s (AM)	–	500	–	Hz
FM		f_s (FM)	–	6,4	–	kHz

DEVELOPMENT DATA

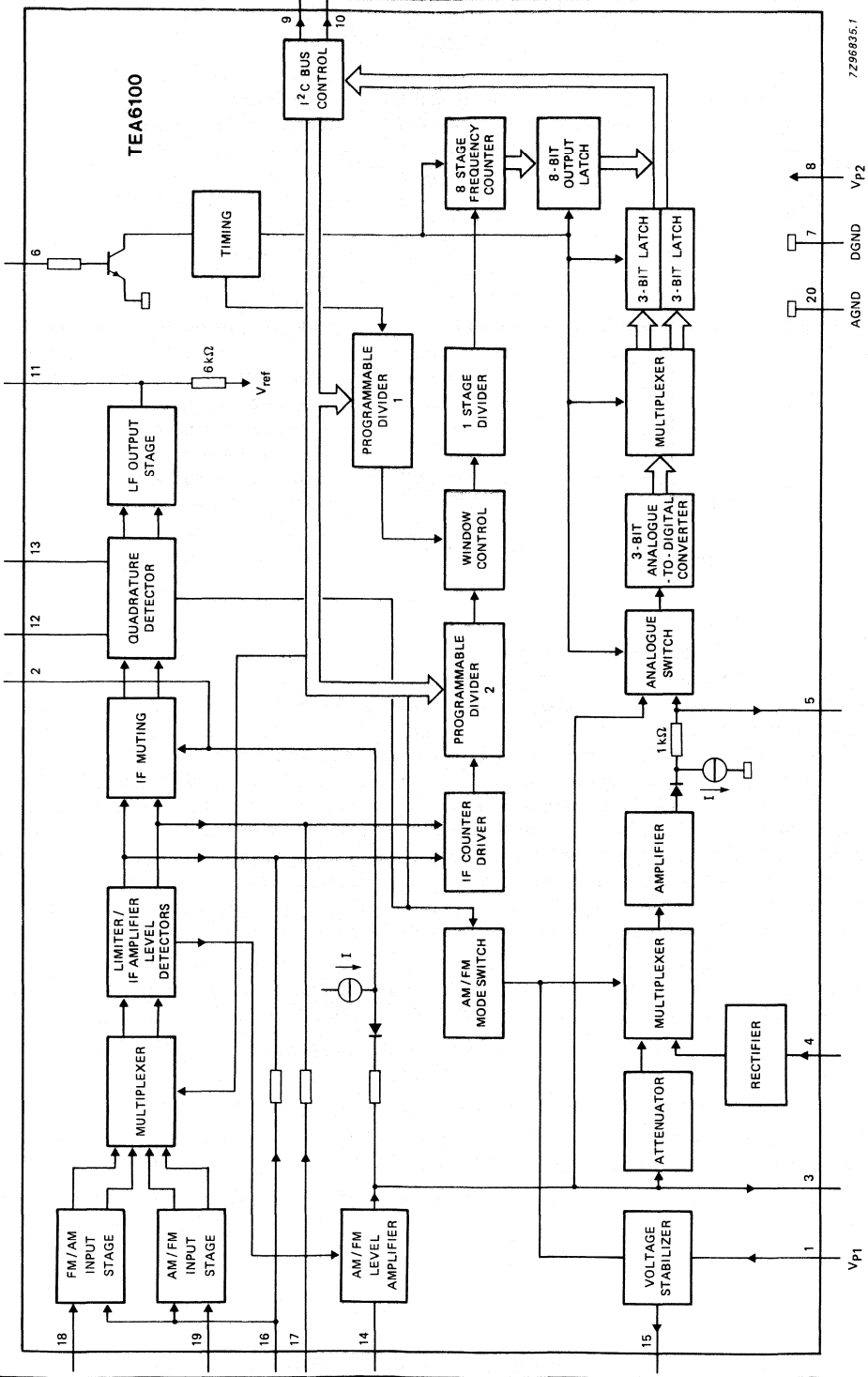


Fig. 1 Block diagram.

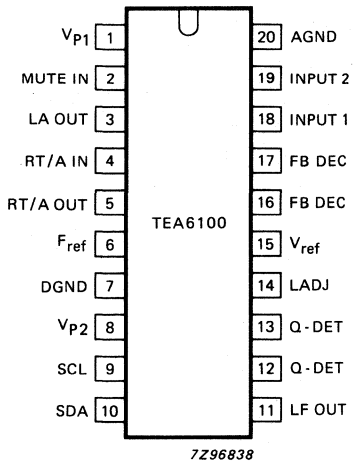


Fig. 2 Pinning diagram.

PINNING

1	V_{P1}	analogue supply voltage
2	MUTE IN	mute input
3	LA OUT	level amplifier output
4	RT/A IN	rectifier/amplifier input
5	RT/A OUT	rectifier/amplifier output
6	F_{ref}	reference frequency input
7	DGND	digital ground
8	V_{P2}	digital supply voltage
9	SCL	serial clock line (I^2C bus)
10	SDA	serial data line (I^2C bus)
11	LF OUT	audio output signal
12	Q-DET	phase shift for quadrature detector
13	Q-DET	phase shift for quadrature detector
14	LADJ	level amplifier adjustment
15	V_{ref}	reference voltage
16	FB DEC	decoupled feedback
17	FB DEC	decoupled feedback
18	INPUT 1	FM/AM IF input
19	INPUT 2	AM/FM IF input
20	AGND	analogue ground

FUNCTIONAL DESCRIPTION (see Figs 1 and 13)

The IF amplifier consists of four balanced limiting amplifier stages, two separate inputs (AM and FM) and one output. Software programming (see Table 2; Figs 4 and 5) allows the input signals (AM/FM) to be inserted on either input (pin 18 or 19). The output drives the frequency counter and via the mute stage, drives the quadrature detector. The output of the quadrature detector is applied to an audio stage (which has a single-ended output). The AM/FM level amplifier, which is driven by 5 IF level detectors, generates a signal dependent d.c. voltage. The level output voltage is used internally to control the mute stage and, if required, the signal can be used externally to control the stereo channel separation and frequency response of a stereo decoder. The signal is also feed to the analogue-to-digital converter (ADC). Due to the front-end spread in the amplification, the level voltage is made adjustable (LADJ, pin 14). The level voltage amplifier controls the mute stage and this insures the −3 dB limiting point remains constant, independent of the front-end spread. AM and FM mode have different front-end circuitry, therefore LADJ must be adjustable for both inputs.

The output voltage of the level amplifier is dependent upon the field strength of the input signal. The multi-path of the FM signal exists in the AM modulation of the input signal. The following method is used to determine the level information and the amount of multi-path (as a DC voltage):

- the IF level detector detects the multi-path and feds the signal, via the level amplifiers, to the external bandpass filter (pin 3) and ADC1
- the signal is then fed to an internal rectifier
- the rectified signal is then fed to an amplifier, so at pin 5 the DC level information is externally available and internally used by ADC2

In the FM mode, the DC information concerning the multi-path is available at pin 5 and the level information is available at pin 3.

In the AM mode, the level information at pin 3 cannot be directly used owing to AM modulation on the output signal of the level amplifier. This signal requires filtering, which is achieved by the following method:

- the multiplexer is switched to a position which causes the signal to be applied to the attenuator
- after attenuation the signal is fed to an amplifier (the resultant gain of attenuator and amplifier is unity), after amplification the signal is filtered by an internal resistor and external capacitor
- after filtering the signal is applied to ADC2 and is externally available

In AM mode pin 5 contains the level information.

The voltages on pin 3 and 5 are converted into two 3-bit digital words by the ADC, which can then be read out by the I^2C bus. The meaning of the 3-bit words is shown in Table 1.

Table 1 3-bit words

word	position	
	FM	AM
1	multipath	level without modulation
2	level	level with modulation

The FM modulated signal is converted into an audio signal by the symmetrical quadrature detector. The main advantage of such a detector is that it requires few external components.

An FM signal requires good AM suppression, and as a result, the IF amplifiers must act as limiters. To achieve good suppression on small input signals the IF amplifiers must have a high gain and thus a high sensitivity. High sensitivity is an undesirable property when used in car radio applications, this problem is solved by having an externally adjustable mute stage to control the overall sensitivity of the device.

The IF mute stage is controlled by the level amplifier (soft muting) and is only active in FM mode. If the input falls below a predetermined level, the mute stage becomes active. To avoid the 'ON/OFF' effect of the audio signal due to fluctuations of the input signal, the mute stage is activated rapidly but de-activated slowly. The mute stage is de-activated slowly, via a current source and an external capacitor at pin 2, to avoid aggressive behaviour of the audio signal. It is possible to adjust the '−3 dB limiting point' of the audio output via the level voltage due to the level signal being externally adjustable. If hard muting is required then pin 2 must be switched to ground.

The 8-bit counter allows accurate stop information to be obtained, because exact tuning is achieved when the measured frequency is equal to the centre frequency of the IF filter.

To measure the input frequency, the number of pulses which occur in a defined time must be counted. This defined time is refered to as 'window'. A wide window indicates a long measuring time and therefore a high accuracy. The counter resolution is defined as Hertz per count. Due to the TEA6100 having to measure the IF frequencies of AM and FM, the counter resolution must be adjustable (different channel spacing). The counter resolution depends on the setting of dividers 1 (N1), divider 2 (N2) and the reference frequency (F_{ref}). The divider ratios of N1 and N2 are controlled by software (see section PROGRAMMING INFORMATION). In Table 3 the window and counter resolution has been calculated for a reference frequency of 40 kHz. The accuracy is controlled by bit 7 of the input word. Although the resolution is the same for bit 7 = logic 0 and bit 7 = logic 1, the width of the window doubles when bit 7 = logic 1.

- bit 7 = 0, accuracy = ± counter resolution
- bit 7 = 1, accuracy = ± $\frac{1}{2}$ counter resolution

Communication between TEA6100 and the microcomputer is via a two wire bidirectional I^2C bus. The power supply lines are fully isolated to avoid cross talk between the digital and analogue parts of the circuit.

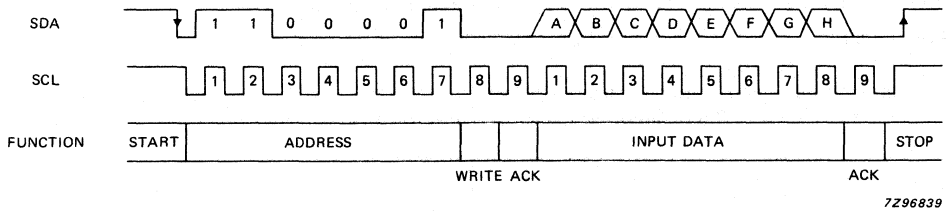


Fig. 3 Input data format waveforms.

Table 2 Input bits

bit	function	logic 0	logic 1	see Figs. 5 and 6
1	reference frequency	32 kHz	40 kHz	A
2	IF mode	AM	FM	B
3	IF input	pin 19	pin 18	C
4	counter input	460 kHz	10,7 MHz	D
5	counter mode	AM	FM	E
6	resolution	divide by 8	divide by 1	F
7	accuracy	LOW	HIGH	G
8	test mode	OFF	ON	H

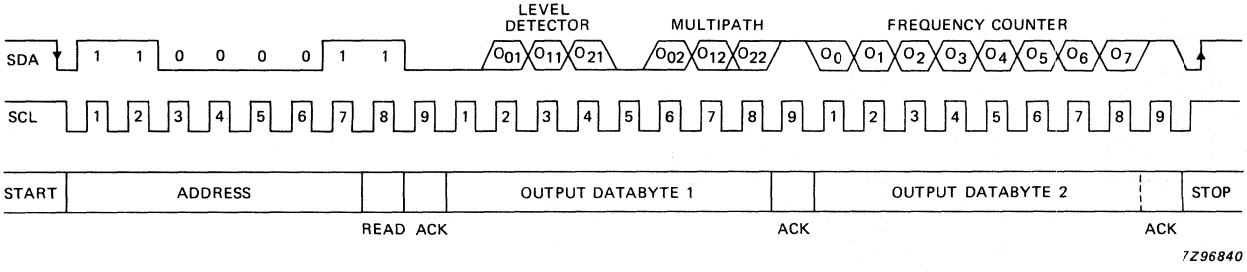


Fig. 4 Output data format waveforms.

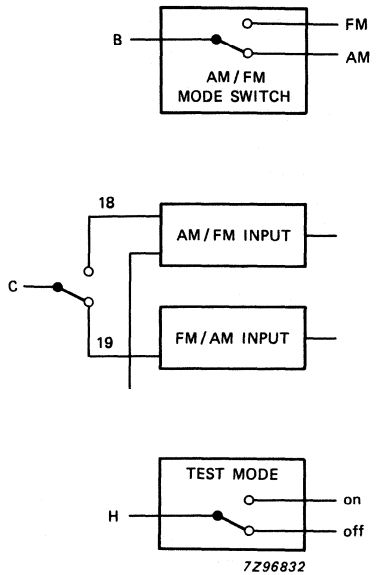


Fig. 5 Switch positions, analogue part (switches drawn in logic 0 state).

DEVELOPMENT DATA

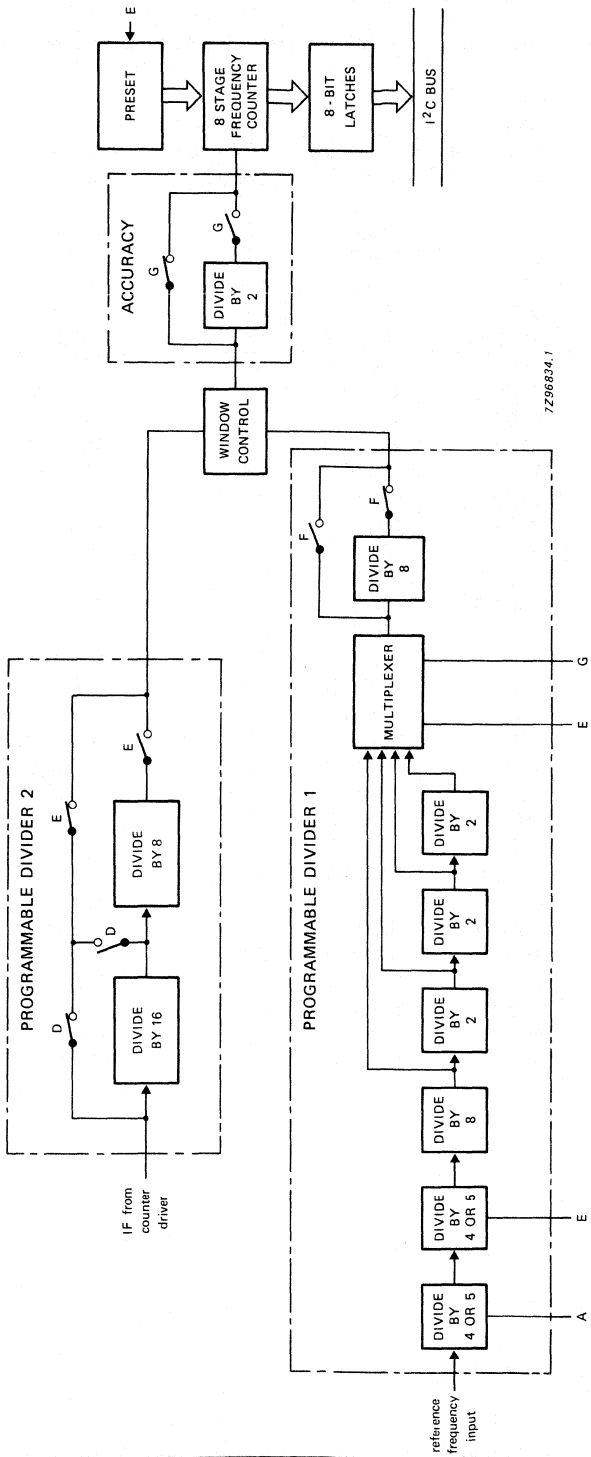


Fig. 6 Switch positions, digital part (switches drawn in logic 0 state, see Tables 2 and 3).

Table 3 Possible window settings and counter resolutions with a 40 kHz reference frequency (see Figs. 5 and 6)

position of switch ADEFG	window (ms)	counter resolution Hz/count	IF frequency (kHz)	read out by IF frequency (hex)	range (kHz)	
					min.	max.
00000	25,6	39,1	460,0	4F	456,914	466,875
10000	32,0	31,3	460,0	CF	453,531	461,500
00001	51,2	39,1	460,0	4F	456,914	466,875
10001	64,0	31,3	460,0	CF	453,531	461,500
00100	128,0	1000,0	460,0	C3	265,000	520,000
10100	160,0	800,0	460,0	36	416,800	620,800
00101	256,0	1000,0	460,0	C3	256,000	520,000
10101	320,0	800,0	460,0	36	416,800	620,800
00010	3,2	312,5	460,0	0F	455,312	535,000
10010	4,0	250,0	460,0	7F	428,250	492,000
00011	6,1	312,5	460,0	0F	455,312	535,000
10011	8,0	250,0	460,0	7F	428,250	492,000
00110	16,0	8000,0	460,0	30	76,000	2116,000
10110	20,0	6400,0	460,0	3F	56,800	1688,800
00111	32,0	8000,0	460,0	30	76,800	2116,000
10111	40,0	6400,0	460,0	3F	56,800	1688,800
01000	25,6	625,0	10700,0	2F	10670,625	10830,000
11000	32,0	500,0	10700,0	E7	10584,500	10712,000
01001	51,2	625,0	10700,0	2F	10670,625	10830,000
11001	64,0	500,0	10700,0	E7	10584,000	10712,000
01100	128,0	1000,0	10700,0	C3	10505,000	10760,000
11100	160,0	800,0	10700,0	36	10656,800	10860,800
01101	256,0	1000,0	10700,0	C3	10505,000	10760,000
11101	320,0	800,0	10700,0	36	10656,800	10860,000
01010	3,2	5000,0	10700,0	AB	9845,000	11120,000
11010	4,0	4000,0	10700,0	C2	9924,000	10944,000
01011	6,4	5000,0	10700,0	AB	9845,000	11120,000
11011	8,0	4000,0	10700,0	C2	9924,000	10944,000
01110	16,0	8000,0	10700,0	30	10316,000	12356,000
11110	20,0	6400,0	10700,0	7F	9887,200	11519,200
01111	32,0	8000,0	10700,0	30	10316,000	12356,000
11111	40,0	6400,0	10700,0	7F	9887,200	11519,200

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	0	13,2	V
Total power dissipation		P_{tot}	see Fig. 7		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+85	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 70 K/W

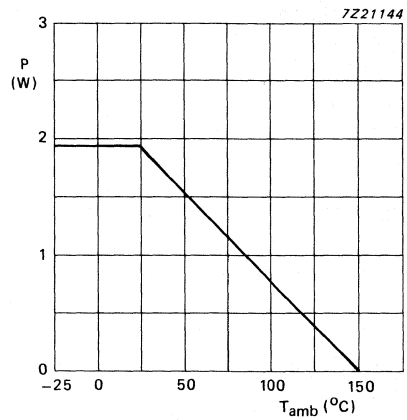


Fig. 7 Power derating curve.

DC CHARACTERISTICS (note)

$V_{P1} = V_{P2} = 8{,}5$ V; $T_{amb} = 25$ °C; all currents positive into the IC; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	7,5	8,5	12	V
Supply current						
FM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	19	25	mA
AM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	15	25	mA
digital part		I_{P2}	–	16	23	mA
Power dissipation		P_d	–	280	–	mW

DEVELOPMENT DATA

AC CHARACTERISTICS (note 1)

V_P = 8,5 V; $V_{i(FM)}$ = 1 mV; f = 10,7 MHz; Δf = 22,5 kHz; f_m = 1 kHz; FM mode; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
IF amplifier, quadrature detector and LF amplifier output	pin 11					
Sensitivity	−3 dB before limiting; inactive mute	$V_{i(FM)}$	–	15	30	μV
Sensitivity	S/N = 26 dB; inactive mute	$V_{i(FM)}$	–	12	–	μV
Signal plus noise to noise ratio	$V_{i(FM)}$ = 10 mV; bandwith = 0,3 to 15 kHz; Δf = 75 kHz	(S + N)/N	–	85	–	dB
IF input range	AM suppression > 40 dB	$V_{i(FM)}$	–	0,09 to 1000	–	mV
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	160	200	240	mV
Total harmonic distortion for single tuned circuit	Δf = 75 kHz	THD	–	0,65	–	%
AM suppression	note 2; see Fig. 8; $V_{i(AM)}$ range = 200 μV to 600 mV	AMS	–	60	–	dB
	$V_{i(AM)}$ range = 200 μV to 600 μV	AMS	–	55	–	dB
Supply voltage ripple rejection	200 Hz; 20 log (V_i/V_o)	SVRR	38	40	–	dB
IF counter inputs						
Frequency counter sensitivity	minimum input voltage for a readout ± 1 bit;					
FM mode	10,7 MHz	$V_{i(FM)}$	–	–	60	μV
AM mode	10,7 MHz	$V_{i(AM)}$	–	–	60	μV
AM mode	460 kHz	$V_{i(AM)}$	–	–	45	μV
Maximum input voltage		V_i	–	–	1	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
FM level performance	see Fig. 9					
Output voltage adjustment range	$V_{i(FM)}$ = 0 V; pins 3 and 14	V_{LFM}	–	0,1 to 4,6	–	V
Maximum output voltage	pins 3 and 14	V_{LFM}	V_P–1,5	–	–	V
Adjustable gain	$V_{i(FM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(FM)}$	1,4	1,6	1,8	V/dec *
Output impedance of level amplifier	$V_{LFM} > 1$ V	$\lvert Z_o \rvert$	–	100	–	Ω
AM level performance	see Fig. 10					
Output voltage adjustment range	$V_{i(AM)}$ = 0 V; pins 5 and 14	V_{LFM}	–	0,1 to 4,6	–	V
	$V_{i(AM)}$ = 10 mV; pins 5 and 14	V_{LAM}	6	–	–	V
Adjustable gain	$V_{i(AM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(AM)}$	1,3	1,5	1,7	V/dec *
IF soft muting	V_{LFM}; pin 3; see Fig. 11					
Mute operating range		V_{LFM}	–	0,1 to 2,5	–	V
Mute voltage	–3 dB output attenuation	V_{LFM}	1,20	1,45	1,75	V
Maximum muting	V_{LFM} = 0,1 V	V_{MUTE}	–	19	–	dB
IF hard muting	V_{MUTE}; pin 2					
Mute voltage	–60 dB output attenuation	V_{MUTE}	–	460	–	mV
Mute discharge current	V_{MUTE} = 1 V; V_{LEVEL} = 0 V; mute ON; pin 2	$+I_2$	–	270	–	μA
Mute charging current	V_{MUTE} = 0 V; mute OFF	$-I_2$	–	1,5	–	μA

* V/dec = voltage per decade.

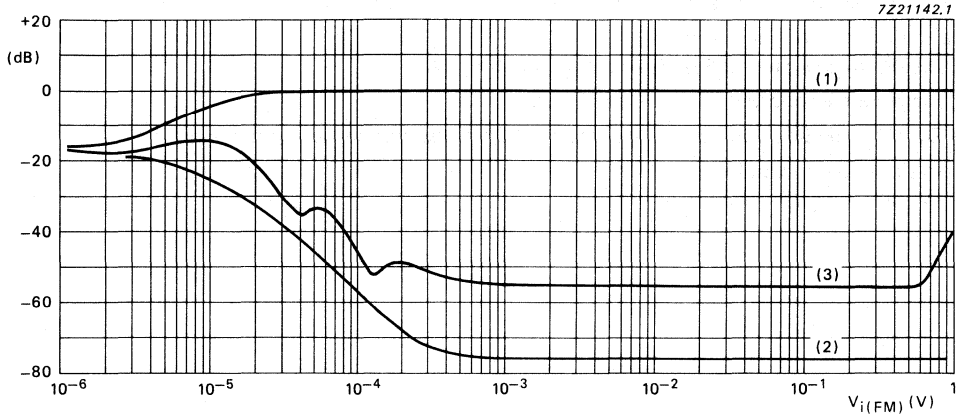
AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Rectifier/amplifier						
Input impedance	pin 4	$\|Z_i\|$	7	10	13	kΩ
Conversion gain AC to DC	pins 4 and 5; bandwith = 100 Hz to 120 kHz; 20 log $V_{O(MP)}$ (d.c.)/ $V_{i(MP)}$ (a.c.)	G_A	–	30	–	dB
DC output voltage range		$V_{O(MP)}$	–	0,2 to 6	–	V
Output characteristics	see Fig. 13; note 3					
Discharge current		I_o	–	200	–	μA
Output ripple in AM mode (peak-to-peak value)	f_m = 200 Hz; m = 0,8; $V_{i(AM)}$ range = 100 μV to 30 mV	V_{ripple}	–	300	400	mV
Multi-path output	see Fig. 12; note 4					
Reference voltage output	pin 15, FM only					
Output voltage		V_{ref}	–	4,4	–	V
Output sink current		$+I_{15}$	–	–	1,5	mA
Output impedance		$\|Z_O\|$	–	–	10	Ω
Output charge current		$-I_{15}$	5	–	–	mA
Output voltage	AM mode	V_{ref}	–	0	–	V
Output impedance	AM mode	$\|Z_O\|$	–	14	–	kΩ
I^2C bus data format	see Figs 3 and 4; Table 2					
3-bit ADC	multi-path and level information, note 5					
Trip level LOW		V_{TL}	1,20	1,45	1,75	V
Trip level HIGH		V_{TH}	4,25	4,50	4,75	V
Reference frequency input	pin 6					
Reference range		F_{ref}	–	–	40	kHz
Input voltage LOW		V_{IL}	–	–	0,4	V
Input current HIGH		I_{IH}	5	–	–	μA

Notes to the characteristics

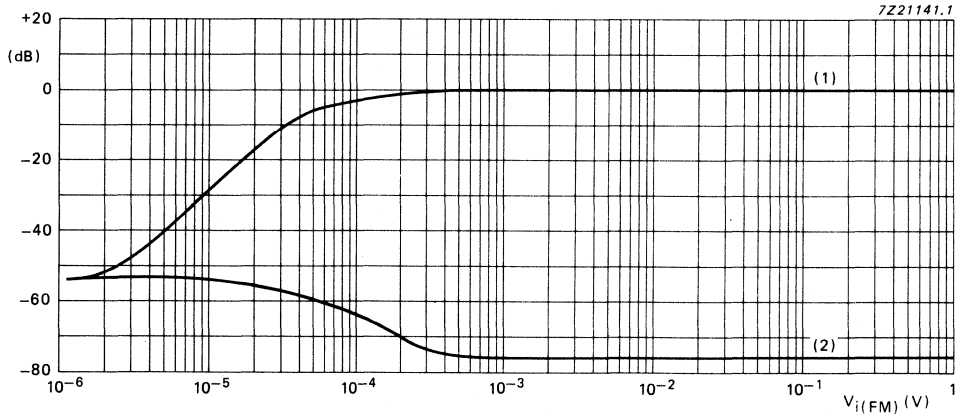
1. All characteristics are measured from the circuit shown in Fig. 13.
2. Conditions for this parameter are:
   20 log $V_{o(FM)}$; m = 0,3 or 20 log $V_{o(AM)}$; m = 0,3.
3. Voltage source followed by diode and resistor.
4. A DC shift can be achieved by connecting a 1,8 MΩ resistor between pin 4 and pin 15.
5. Step size between trip levels:
   $(V_{TH} - V_{TL})/6 \pm 0{,}07$ V.

DEVELOPMENT DATA



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.
(2) Noise (with dBA filter) for V_{ADJ} = 0 V.
(3) AM suppression (m = 0,3 and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.

Fig. 8(a) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 2,4 V.
(2) Noise (with dBA filter) for V_{ADJ} = 2,4 V.

Fig. 8(b) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.

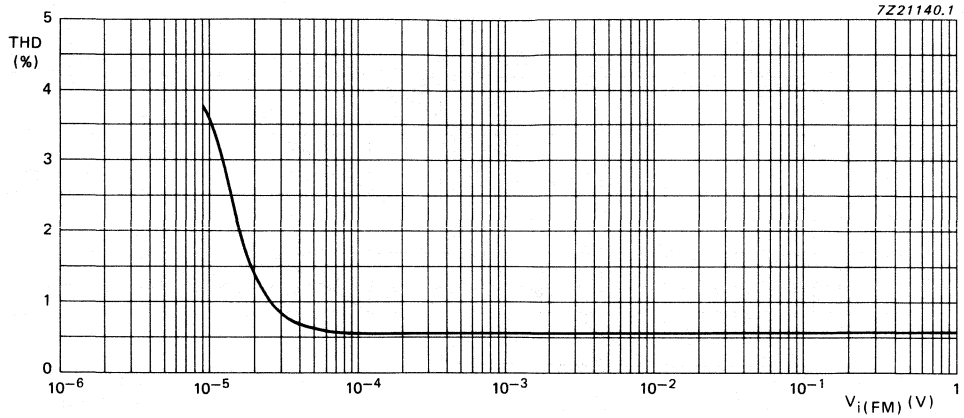
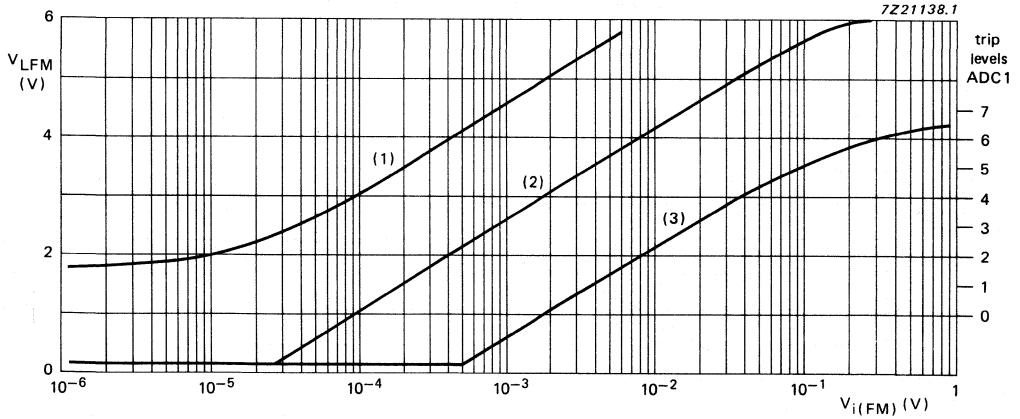


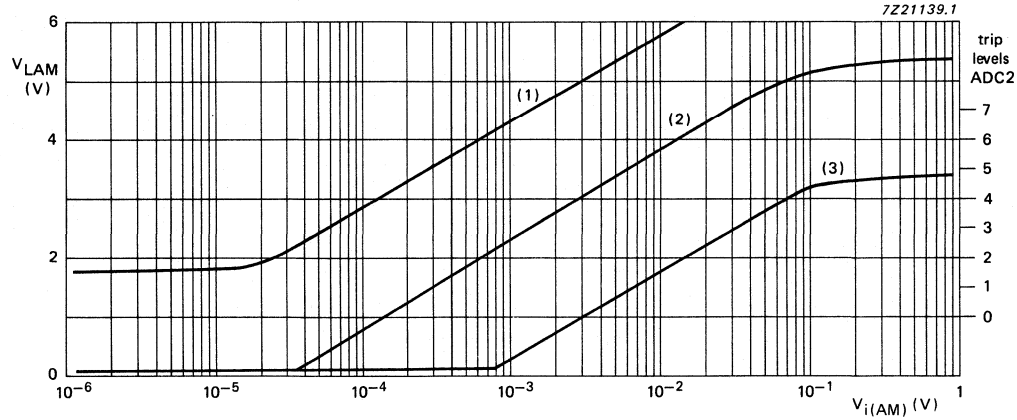
Fig. 8(c) Total harmonic distortion; Δf = 75 kHz, f_{mod} = 1 kHz and V_{ADJ} = 0 V.

DEVELOPMENT DATA



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 9 Level voltage output (V_{LFM}) plotted against IF input signal, $V_{i(FM)}$; IF = 10,7 MHz.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 10 Level voltage output (V_{LAM}) plotted against IF input signal, $V_{i(AM)}$; IF = 10,7 MHz or 460 kHz.

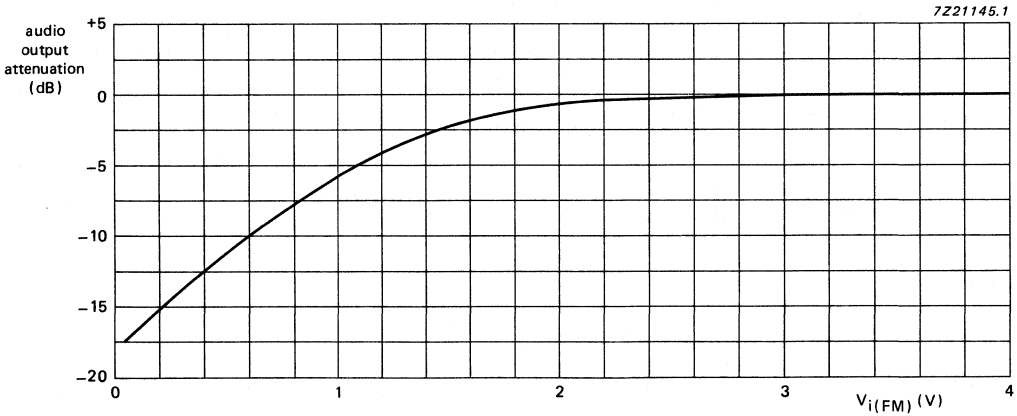
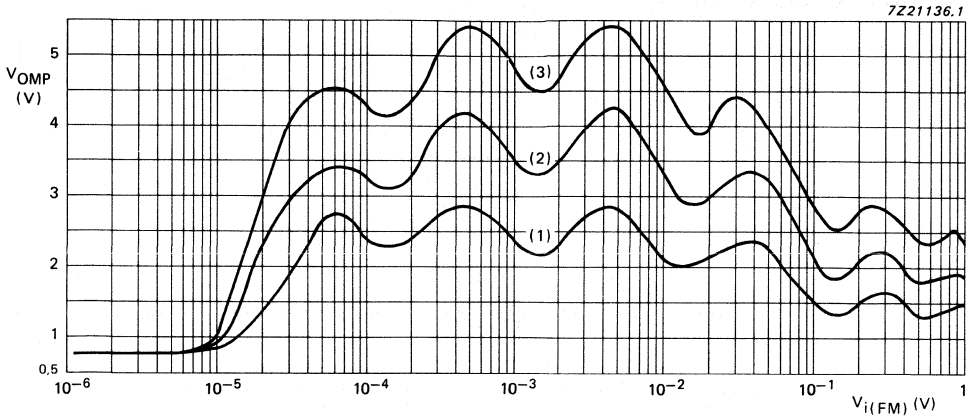


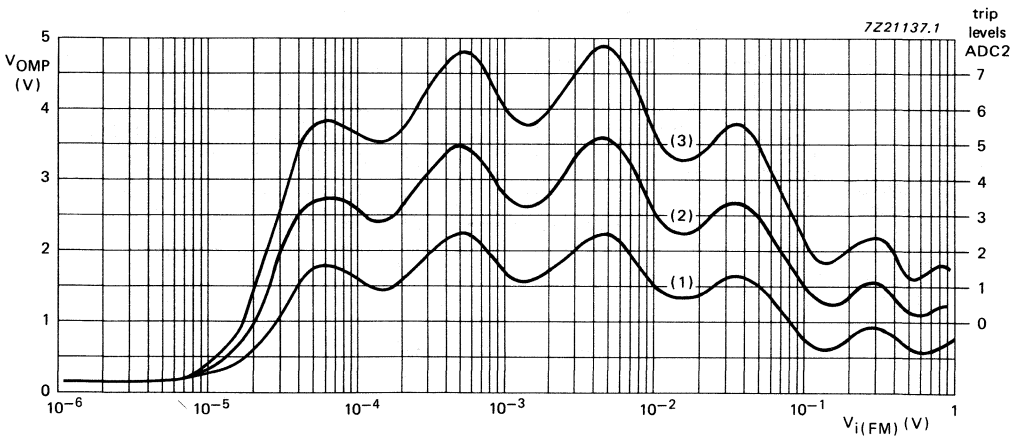
Fig. 11 Soft muting plotted against level output voltage; $V_{i(FM)}$ = 1 mV and Δf = 22,5 kHz.



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(a) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V and 1,8 MΩ resistor connected between pin 4 and pin 15.

DEVELOPMENT DATA



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(b) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V.

APPLICATION INFORMATION

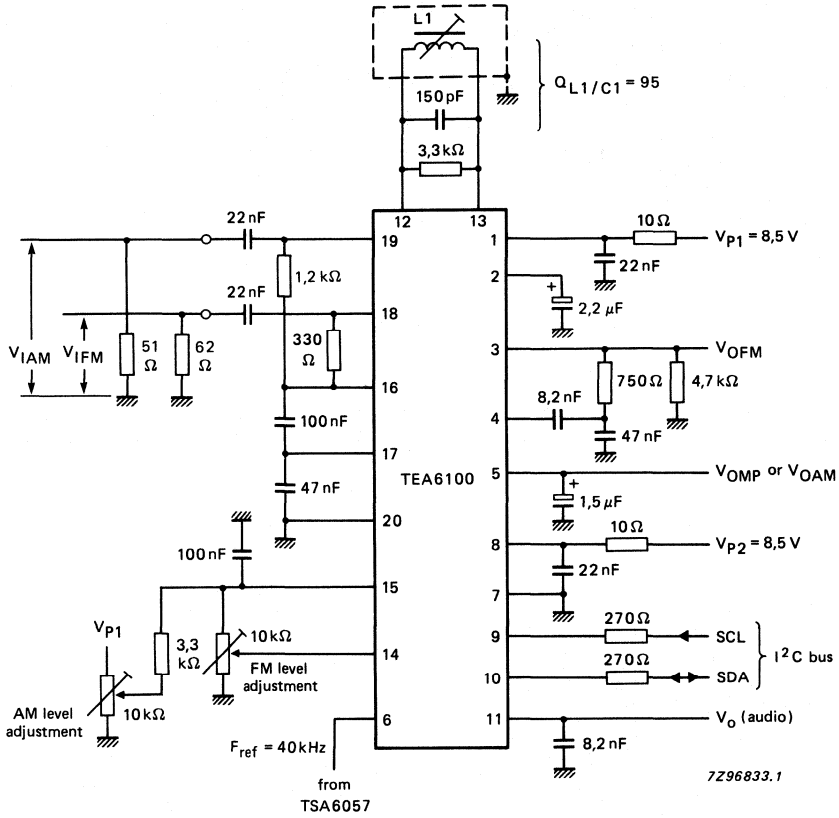


Fig. 13 Application diagram.

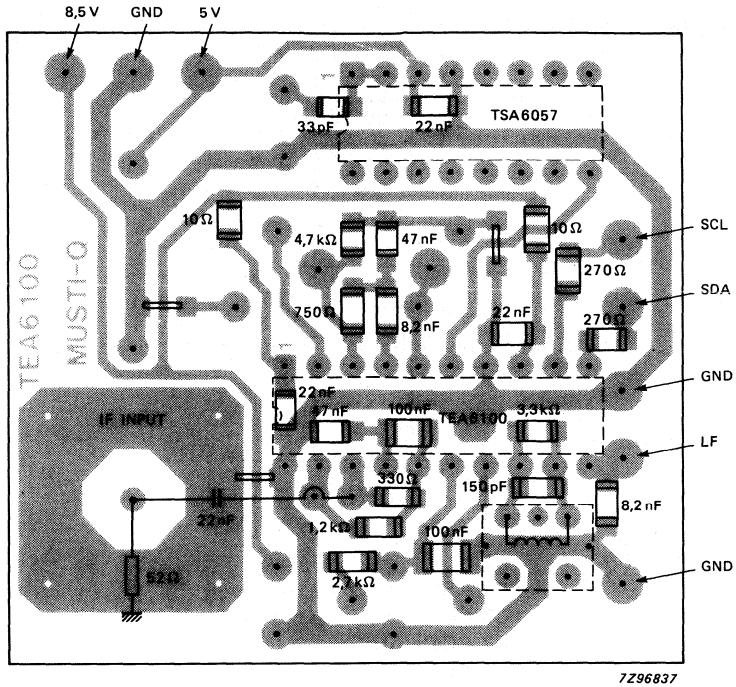


Fig. 14 Track side of printed circuit board.

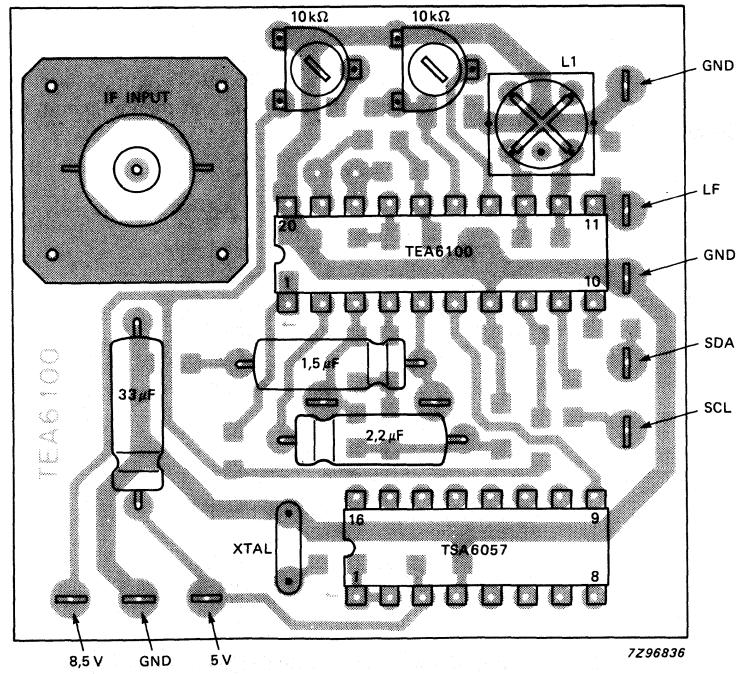
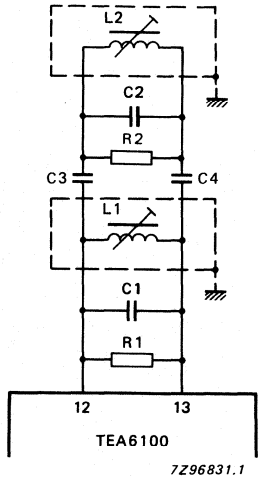


Fig. 15 Component side of printed circuit board.

Double tuned circuit



R1 = 5,1 kΩ, R2 = 1,5 kΩ
C1 = C2 = 150 pF (n = 220)
C3 = C4 = 10 pF
L1 = L2 = 1,6 μH

Fig. 16 Double tuned demodulator circuit.

Alignment of the circuit is obtained with an IF input signal > 200 μV. Tuning the circuit is performed by, detuning L2, adjusting L1 to obtain a minimum distortion level and then adjusting L2 to obtain a minimum distortion level.

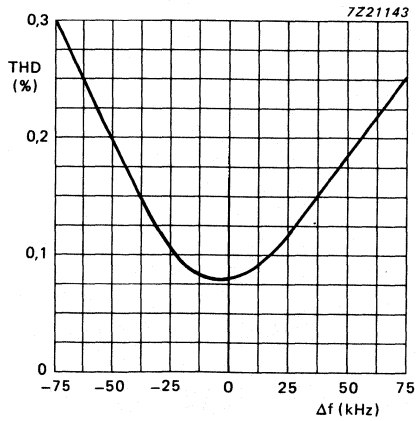


Fig. 17 Total harmonic distortion plotted against IF detuning; for $\Delta f = \pm 75$ kHz, $f_{mod} = 1$ kHz and $V_O = 500$ mV.

PROGRAMMING INFORMATION

Converting the read out of the counters into frequency

The counter resolution at the input is defined as:

- resolution = divider ratio of N2/window

For every increment of the counter the counted frequency increases relative to the resolution in Hertz, as shown in example:

- window = 20 ms; N2 = 128; IF frequency = 10,7 MHz; resolution = 128/0,02 = 6,4 kHz per count

The counter consists of 8 bits. Therefore, the maximum frequency range that can be counted is 256 x resolution = 1,6384 MHz. In the example the frequency to be counted is 10,7 MHz, therefore, the counter will overflow (in the example above, 7 times). The real measured frequency is:

- f_{real} = (read out + overflow x 256) x resolution

The overflow indicates the off-set on the frequency scale which must be added to the read out. Due to the bandwidth of the IF filter, the frequencies at the input to the TEA6100 are known, for example:

- IF filter for FM has a center frequency of 10,7 MHz and −3 dB bandwidth of 300 kHz. Only the frequencies of 10,7 MHz ± 150 kHz occur at the input of the TEA6100. For this reason it is not necessary to count the overflow.

The read out of the counter has to be translated into frequency. This translation depends upon the counter resolution. The preferred way to calculate the input frequency is to:

- calculate the read out of the target IF frequency. Compare this value with that of the measured read out and multiply the difference by the resolution.

The formulae for calculating the target IF read out and the resolution are as follows (A, D, E, F and G refer to the bits of the I^2C bus input data as shown in Figs 3 and 4 and to the counter/timer block diagram shown in Fig. 6. An, Dn, En, Fn and Gn are inverted values of the variables A, D, E, F and G. Table 3 shows the following formulae calculated for a reference frequency of 40 kHz):

- N1 = (An x 4 + A x 5) x (En x 4 + E x 5) x 8 x $(2^{[E \times 2 + G \times 1]})$ x (F x 1 + Fn x 8)
- Window (T) = $N1/F_{ref}$
- N2 = (E x 16 x 8 + En x [Dn x 1 + D x 16]) x (G x 2 + Gn x 1)
- Target decimal read out (TDEC) = T x (TIFF/N2 + (E x 247 + En x 79). TIFF is the symbol for target IF frequency
- Target read out hexadecimal (THEX), convert the target decimal read out to hexadecimal and use the 2 least significant digits (Do not use overflow value). The symbol for measured hexadecimal is MHEX
- Resolution (R) = N2/T
- Measured frequency (F_I) = (TIFF) + R x (MHEX − THEX)

Note

Care should be taken if TIFF + $\frac{1}{2}$ filter bandwidth is greater than the frequency for the read out of hexadecimal value FF, or if TIFF − $\frac{1}{2}$ filter bandwith is less than the frequency at read out for hexadecimal value 00.

- Counter accuracy (AW and AN), with bit 7 (G) the accuracy can be chosen with the same resolution. If bit 7 is logic 1 the accuracy is HIGH and if bit 7 is logic 0 then the accuracy is LOW.

  bit 7 = 0, AN = ± (N2/T)
  bit 7 = 1, AW = ± ($\frac{1}{2}$ x N2/T)

DEVELOPMENT DATA

Example

The example uses the following values:

TIFF = 10,7 MHz; accuracy = LOW (G = 0); F_{ref} = 40 kHz (A = 1); IF frequency = 10, 7 MHz (D = 1); resolution = N1 (F = 1) and counter mode = FM (E = 1)

N1 = (0 x 4 + 1 x 5) x (0 x 4 + 1 x 5) x 8 x ($2^{[1 \times 2 + 0 \times 1]}$) x (1 x 1 + 0 x 8) = 800

T = 800/40 = 20 ms

N2 = (1 x 16 x 8 + 0 x [1 x 1 + 0 x 16]) x (0 x 2 + 1 x 1) = 128

TDEC = 20 x 10,7/128 + (1 x 247 + 0 x 79) = 1919

THEX; 1919 is hexadecimal 77F and the least significant 2 digits are 7F, so THEX = 7 F

R = 128/20 = 6400 Hz/count

Assume the readout is '6E', the measured frequency will be:

- F_I = 10,7 + (6E − 7F) x 6400 = 10,59 MHz

Assume the readout is '83', the measured frequency will be:

- F_I = 10,7 + (83 − 7F) x 6400 = 10,726

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled preamplifier for car radios.

Features

- Source selector for three stereo inputs
- Inputs and outputs for noise reduction circuits
- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from + 15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control from 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for DOLBY* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINES

28-lead dual in-line; plastic (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

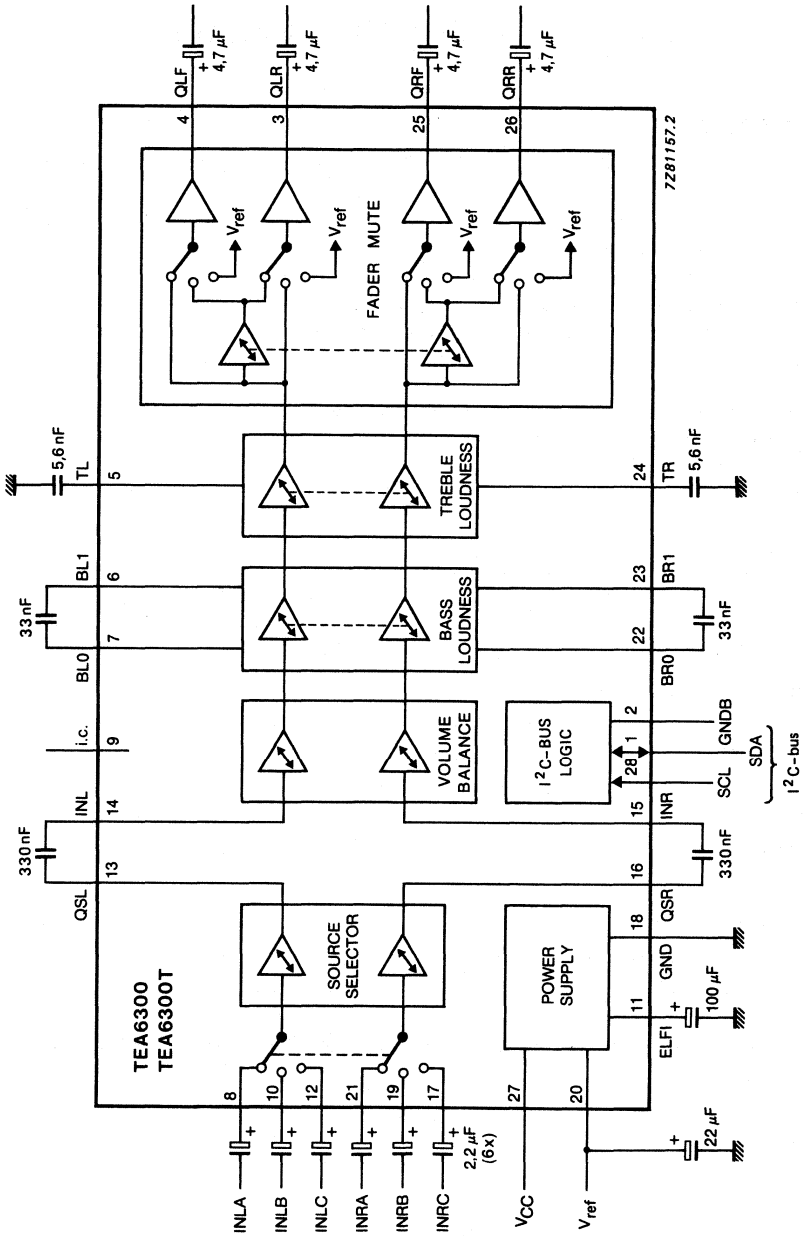


Fig. 1 Block diagram.

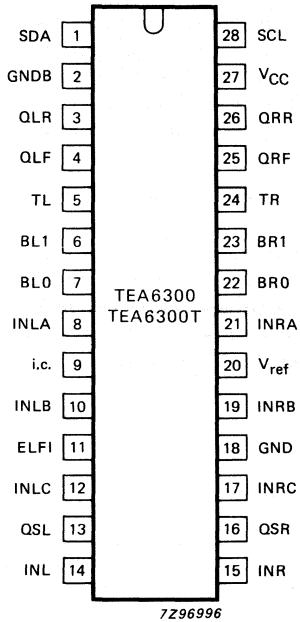


Fig. 2 Pinning diagram.

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	INLA	input left source A
9	i.c.	internally connected
10	INLB	input left source B
11	ELFI	electronic filtering for supply
12	INLC	input left source C
13	QSL	output source selector left
14	INL	input left control part
15	INR	input right control part
16	QSR	output source selector right
17	INRC	input right source C
18	GND	ground
19	INRB	input right source B
20	V_{ref}	reference voltage (1/2 V_{CC})
21	INRA	input right source A
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The source selector selects three stereo channels – RF part (AM/FM), recorder and compact disc. As the outputs of the source selector and the inputs of the main control part are available, additional circuits such as compander and equalizer systems may be inserted into the signal path. The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6300 has four outputs a low-level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the microcomputer and the TEA6300 is required.

The on-chip power-on-reset sets the TEA6300 to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	–55	+ 150	°C
Operating ambient temperature range	T_{amb}	–40	+ 85	°C

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	30	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V
Internal reference voltage (pin 20) $V_{ref} = 0,5\ V_{CC}$	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage	$V_{o(rms)}$	–	500	–	mV
for start of clipping	$V_{o(rms)}$	–	1000	–	mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency −1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = −10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)} < 200$ mV; G_v = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal plus noise-to-noise ratio bass and treble linear; notes 1 and 2 CCIR 468-2 weighted; quasi peak					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	(S + N)/N	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	(S + N)/N	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	70	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	78	–	dB
V_i = 50 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	70	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	85	–	dB
Noise output power mute position, only contribution of TEA6300; power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_V = 0 dB; bass and treble linear	α_B	–	110	–	dB
Source selector					
Input impedance	Z_i	20	30	40	kΩ
Output impedance	Z_o	–	–	100	Ω
Output load resistance	R_L	10	–	–	kΩ
Output load capacity	C_L	0	–	200	pF
Input isolation not selected source; frequency range 40 Hz to 12,5 kHz	α_S	–	80	–	dB
Voltage gain $R_L \geqslant 10$ kΩ	G_v	–	0	–	dB
Internal bias voltage ratio	$V_{b\,int}/V_{ref}$	–	1	–	
Maximum input voltage level (RMS value) THD < 0,5% THD < 0,5%; V_{CC} = 7,5 V	 $V_{i(rms)}$ $V_{i(rms)}$	 – –	 1,65 1,5	 – –	 V V
Total harmonic distortion V_i = 500 mV; R_L = 10 kΩ	THD	–	–	0,1	%
Noise output voltage weighted CCIR 468-2, quasi peak	V_{no}	–	9	20	μV
DC offset voltage between any inputs	V_o	–	–	10	mV
Control part					
Source selector disconnected, source resistance 600 Ω					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Maximum input voltage THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	76	90	–	dB
DC step offset					
Between any adjoining step and any step to mute					
G_v = 0 to −66 dB		–	0,2	10	mV
G_v = 20 to 0 dB		–	2	15	mV
In any treble and fader position G_v = 0 to −66 dB		–	–	10	mV
In any bass position G_v = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Fader control					
Continuous attenuation					
fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current					
HIGH	I_{IH}	−10	–	+ 10	μA
LOW	I_{IL}	−10	–	+ 10	μA
Output voltage LOW					
I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I^2C-bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I^2C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage					
start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 1000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	SCC	SCB	SCA

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
SCA to SCC	source selector control
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

DEVELOPMENT DATA

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

DEVELOPMENT DATA

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting		DATA					
front dB	rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting		DATA					
front dB	rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Selected inputs

selected inputs	DATA		
	SCC	SCB	SCA
data not allowed	1	1	1
data not allowed	1	1	0
data not allowed	1	0	1
INLC, INRC	1	0	0
data not allowed	0	1	1
INLB, INRB	0	1	0
INLA, INRA	0	0	1
data not allowed	0	0	0

Table 8 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

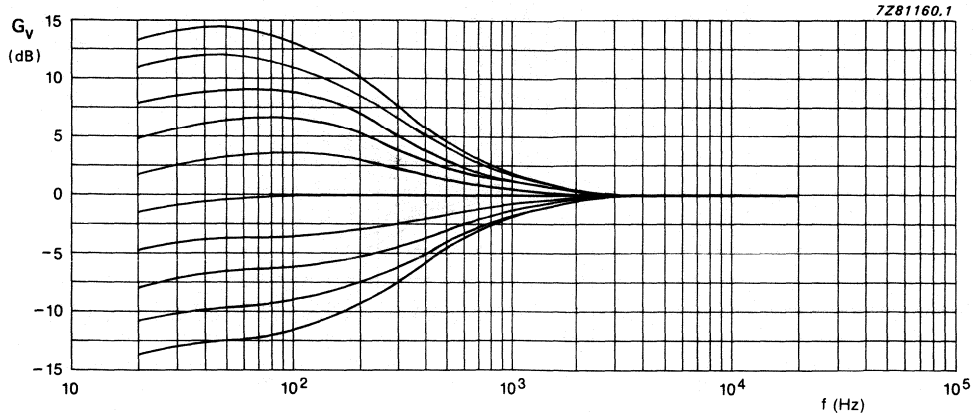


Fig. 3 Bass control without T-pass filter.

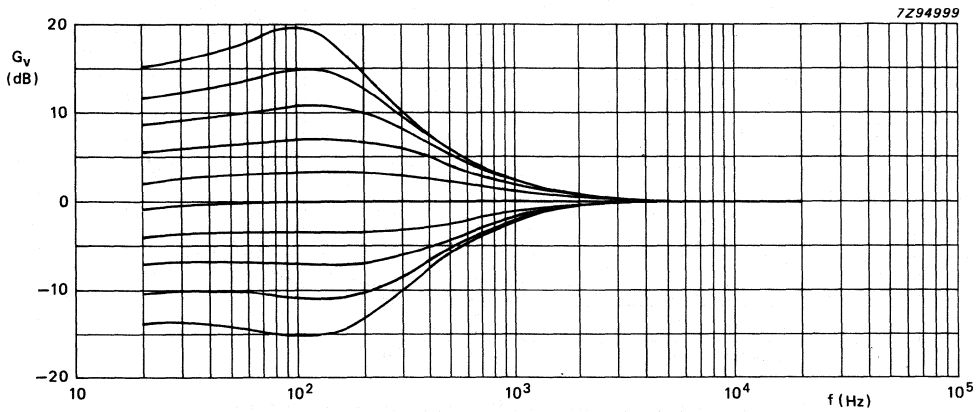
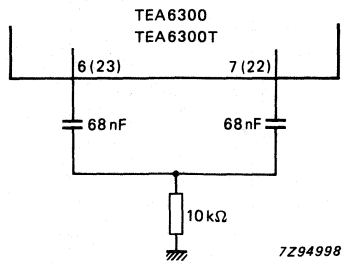


Fig. 4 Bass control with T-pass filter.



Pin numbers in parenthases refer to the bass control, right channel.

Fig. 5 T-pass filter.

DEVELOPMENT DATA

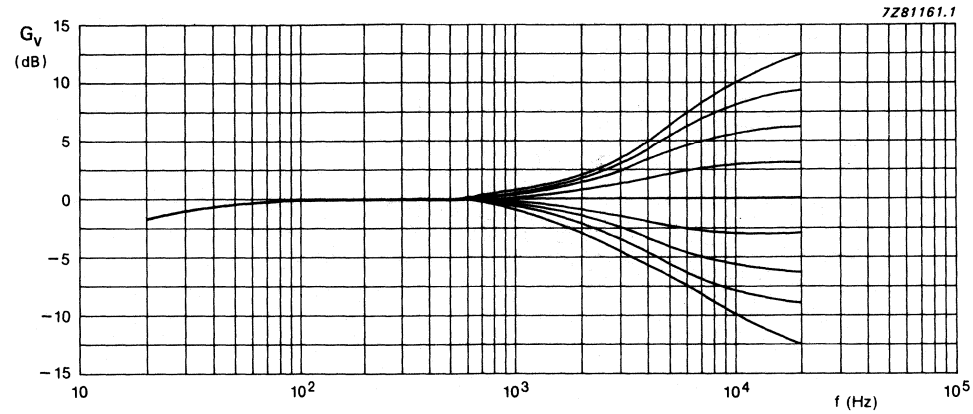


Fig. 6 Treble control.

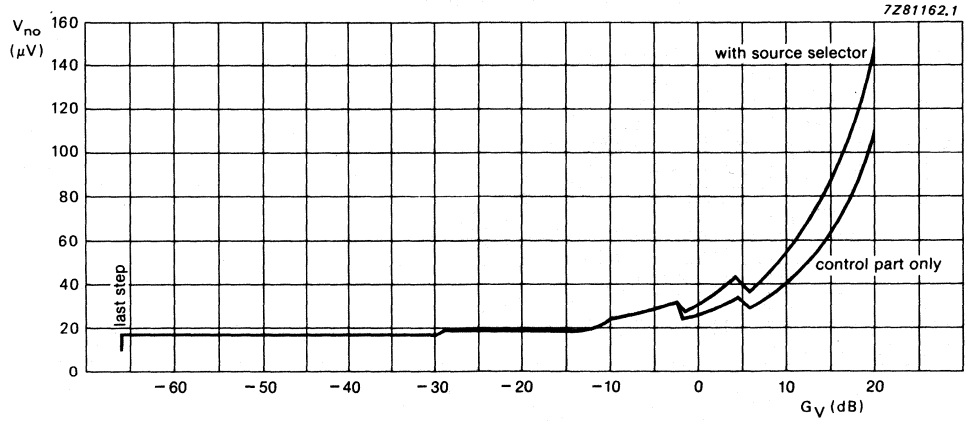


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

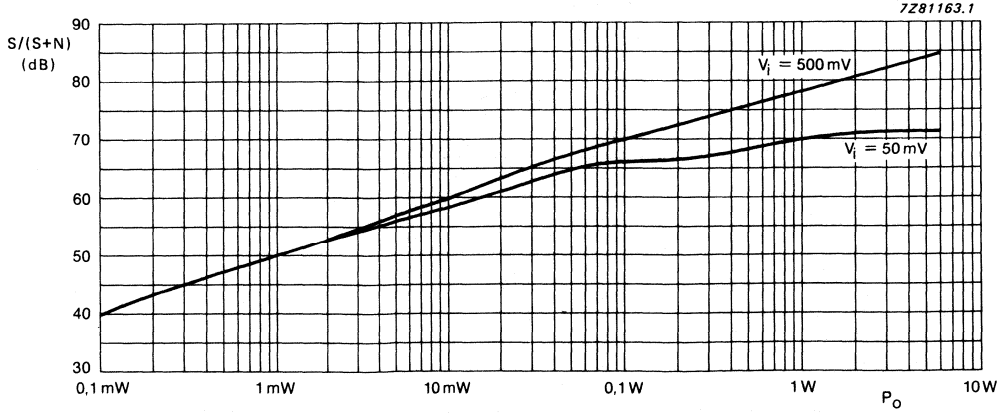


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

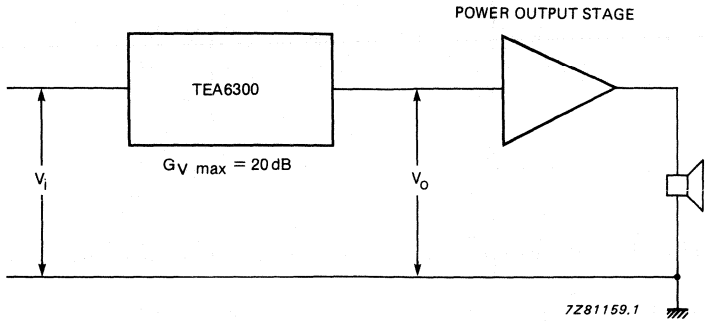


Fig. 9 Recommended level diagram; $V_{i\ min}$ = 50 mV, V_o = 500 mV for P_{max}.

DEVELOPMENT DATA

APPLICATION INFORMATION

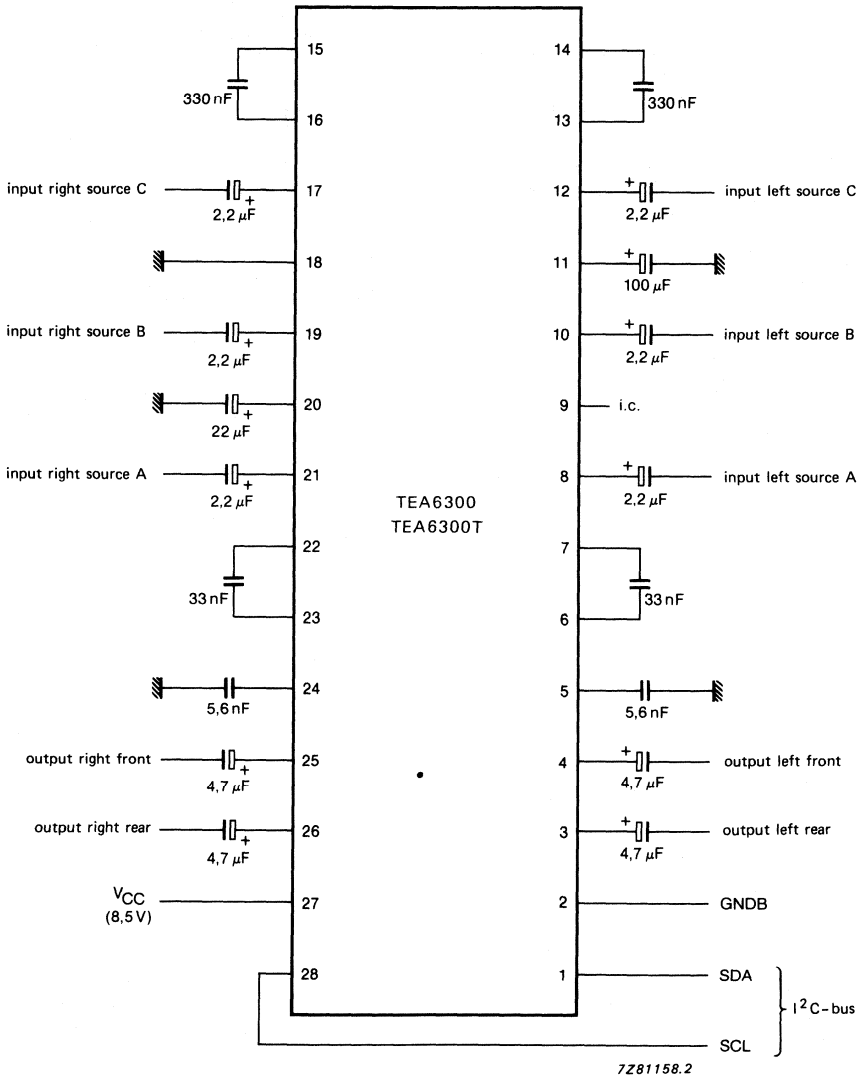


Fig. 10 Test and application circuit.

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled tone and volume control circuit for car radios.

Features

- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from +15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control form 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for Dolby* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	96	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

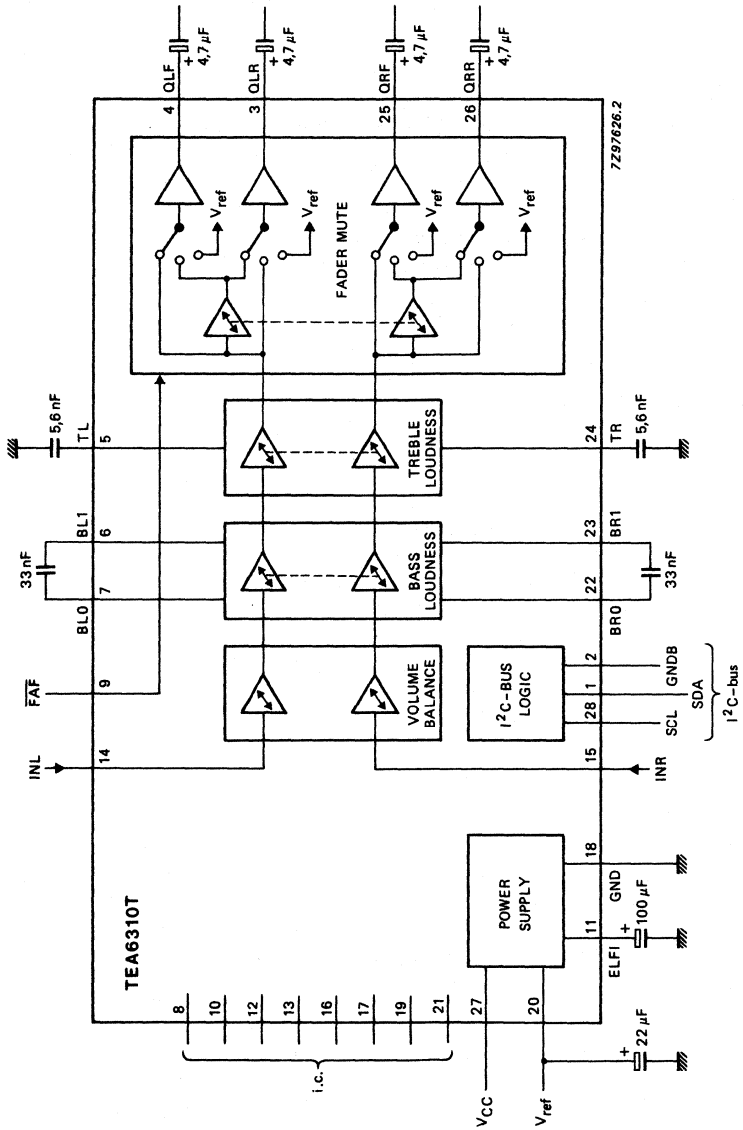


Fig. 1 Block diagram.

DEVELOPMENT DATA

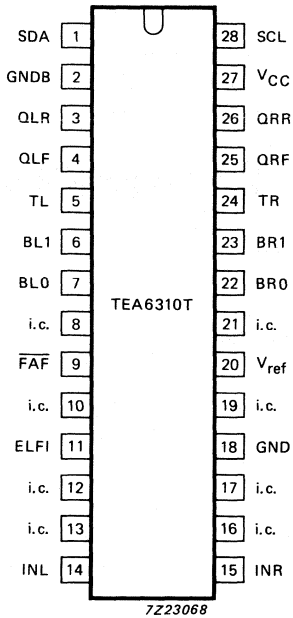


Fig. 2 Pinning diagram

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	i.c.	internally connected
9	$\overline{FAF}$	fader off control input
10	i.c.	internally connected
11	ELFI	electronic filtering for supply
12	i.c.	internally connected
13	i.c.	internally connected
14	INL	input left control part
15	INR	input right control part
16	i.c.	internally connected
17	i.c.	internally connected
18	GND	ground
19	i.c.	internally connected
20	V_{ref}	reference voltage (1/2 V_{CC})
21	i.c.	internally connected
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)

FUNCTIONAL DESCRIPTION

The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6310T has four outputs a low level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. The Fader function can be disabled by an input signal at $\overline{FAF}$ (pin 9).
An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the microcomputer and the TEA6310T is required.

The on-chip power-on-reset sets the TEA6310T to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	30	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage	$V_{o(rms)}$	–	500	–	mV
for start of clipping	$V_{o(rms)}$	–	1000	–	mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency −1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	96	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = −10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)}$ <200 mV; G_v = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal-to-noise ratio; bass and treble linear; notes 1 and 2; CCIR 468-2 weighted; quasi peak;					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	S/(S + N)	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	S/(S + N)	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	S/(S + N)	65	72	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	S/(S + N)	65	78	–	dB
V_i = 50 mV, V_o = 500 mV; P_o = 6 W	S/(S + N)	–	72	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	S/(S + N)	–	86	–	dB
Noise output power mute position, only contribution of TEA310T, power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_v = 0 dB; bass and treble linear;	α_B	–	110	–	dB
Control part					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF
Maximum input voltage; THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage; weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off;					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error; (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error; (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error; balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	76	90	–	dB

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
DC step offset					
Between any adjoining step and any step to mute					
G_v = 0 to −66 dB		–	0,2	10	mV
G_v = 20 to 0 dB		–	2	15	mV
In any treble and fader position					
G_v = 0 to −66 dB		–	–	10	mV
In any bass position					
G_v = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range;					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Fader control					
Continous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Fader enable/disable control (pin 9)					
Fader enabled					
Input voltage HIGH	$V_{9\text{-}18}$	3	–	12	V
Fader disabled					
Input voltage LOW	$V_{9\text{-}18}$	−0,3	–	1,5	V
Input current					
HIGH	I_9	−10	–	+10	μA
LOW	I_9	−10	–	+10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	1,5	V
Input current					
HIGH	I_{IH}	−10	–	+10	μA
LOW	I_{IL}	−10	–	+10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I^2C-bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I^2C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 10000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	X	X	X

Function of the bits:

VL0 to VL5 volume control left
VR0 to VR5 volume control right
BA0 to BA3 bass control
TR0 to TR3 treble control
FA0 to FA3 fader control
FCH select fader channel (front or rear)
MFN mute control of the selected fader channel (front or rear)
GMU mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X don't care bits (logic 1 during testing)

DEVELOPMENT DATA

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+ 15	1	1	1	1
+ 15	1	1	1	0
+ 15	1	1	0	1
+ 15	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+ 12	1	1	1	1
+ 12	1	1	1	0
+ 12	1	1	0	1
+ 12	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

DEVELOPMENT DATA

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting		DATA					
front dB	rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting		DATA					
front dB	rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

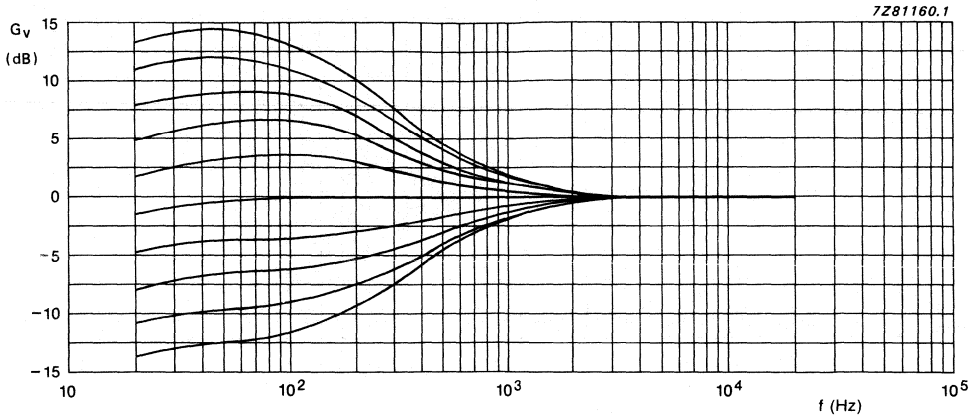


Fig. 3 Bass control without T-pass filter.

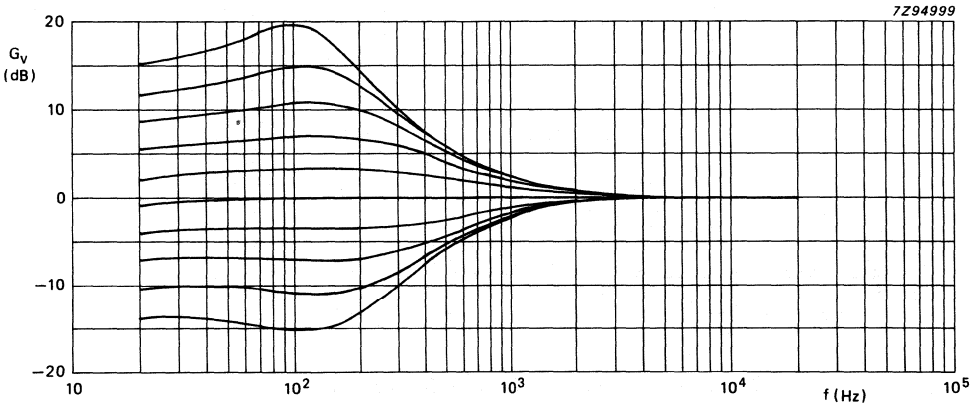
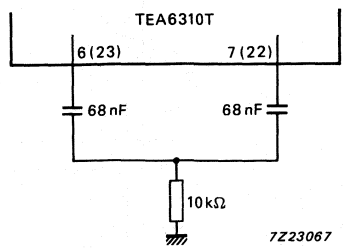


Fig. 4 Bass control with T-pass filter.



Pin numbers in parentheses refer to the bass control, right channel.

Fig. 5 T-pass filer.

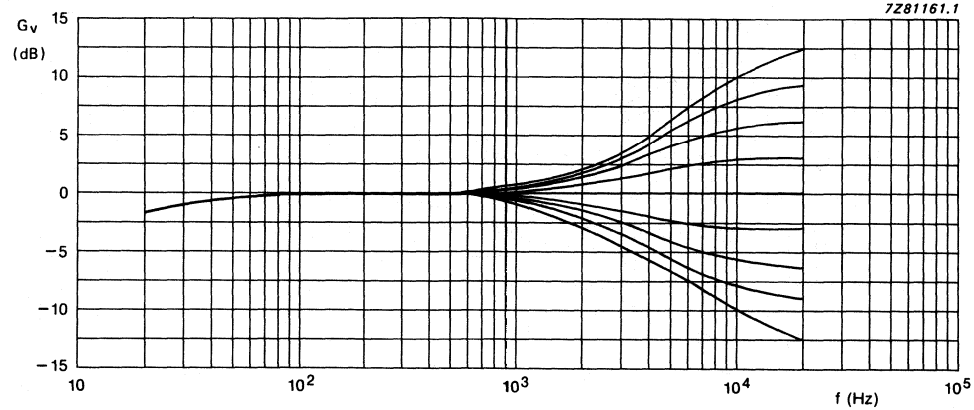


Fig. 6 Treble control.

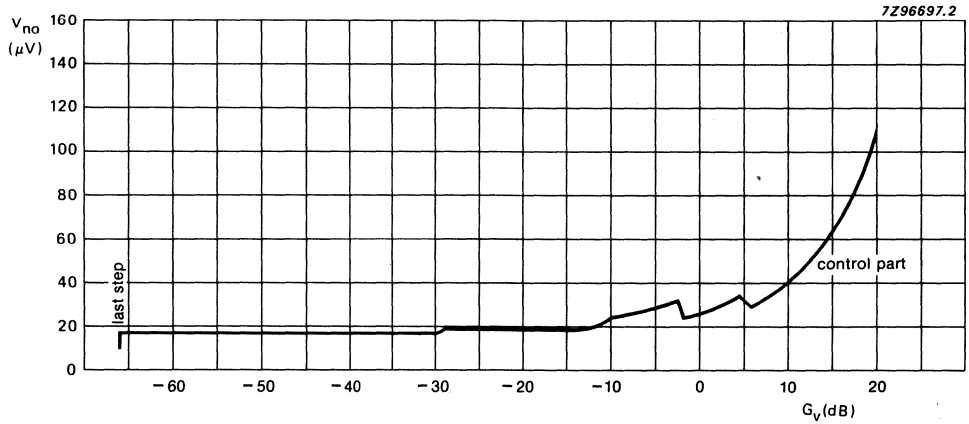


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

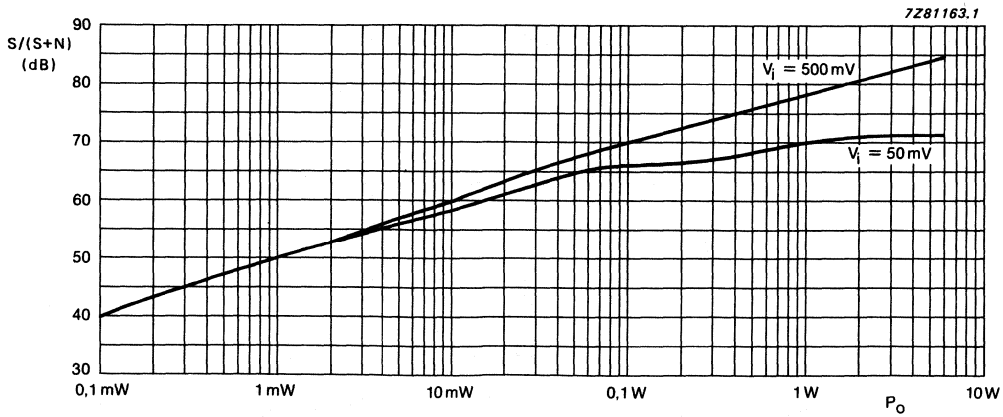


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

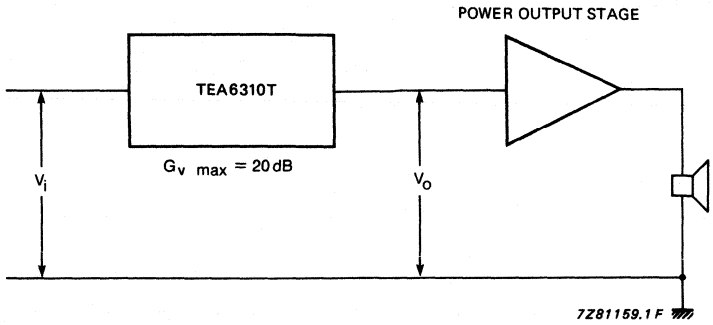


Fig. 9 Recommended level diagram; $V_{i\,min}$ = 50 mV, V_o = 500 mV for P_{max}.

DEVELOPMENT DATA

APPLICATION INFORMATION

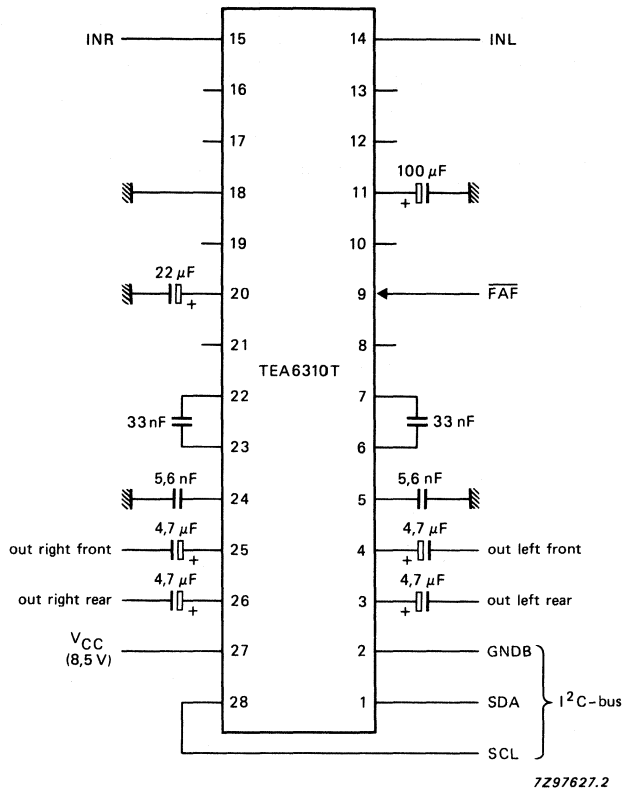


Fig. 10 Test and application circuit.

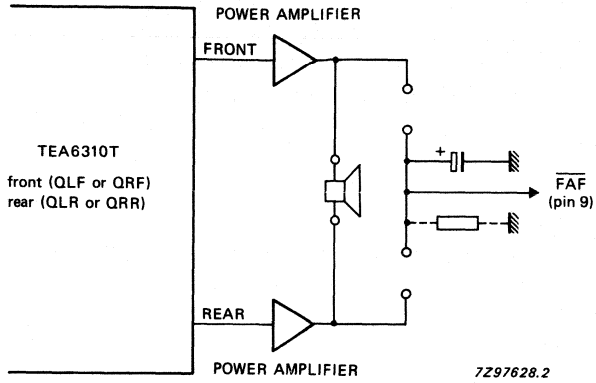


Fig. 11 Automatic FADER control; P_o = 24 W, V_{9-18} = 0 V (FADER disabled).

DEVELOPMENT DATA

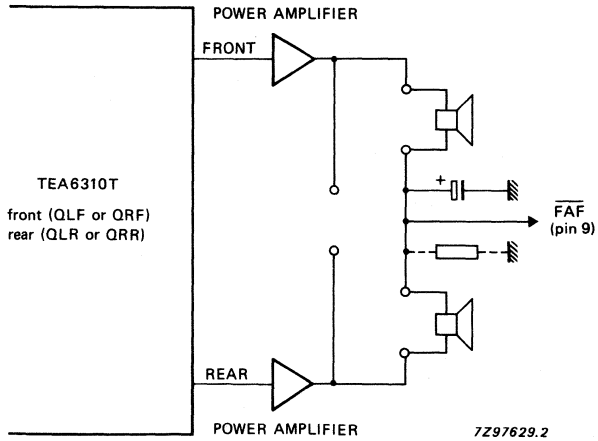


Fig. 12 Automatic FADER control; P_o = 2 x 6 W, V_{9-18} = 7 V (FADER enabled).

1.3 GHz I²C-BUS CONTROLLED FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The TSA5510 is a bipolar single-chip frequency synthesizer. It performs all the tuning functions of a phase-locked loop (PLL) television tuning system. The IC is designed for application in all types of television receivers.

Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, program the 8 output ports and set the programmable current amplifier (charge pump) current. Three of these ports can also be used as general purpose I/O ports.

Digital information concerning these ports can be read out of the TSA5510 on the serial data line (SDA), one status byte, during a READ operation.

A flag is set when the PLL is "in-lock" and read during a READ operation. The TSA5510 has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3.

The phase comparator operates at a frequency of 7.8125 kHz when a 4 MHz crystal is used.

Features

- Complete 1.3 GHz single-chip system
- Low power: 5 V at 35 mA
- I²C-bus programming
- In-lock flag
- Variable capacitor drive disable
- Low radiation
- Address selection for Picture-in Picture Controller (PIPCO), Direct Broadcast Satellite tuner (DBS), etc.
- 8 controllable outputs, 4 bidirectional
- Power-down flag

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)		V_{CC}	4.5	5.0	5.5	V
Supply current		I_{CC}	25	35	50	mA
Input frequency range		f_i	64	–	1300	MHz
Input voltage (RMS value)	f_i = 80 - 150 MHz	$V_{i(rms)}$	12/–25	–	300/2.6	mV/dBm
	f_i = 150 - 1000 MHz	$V_{i(rms)}$	9/–28	–	300/2.6	mV/dBm
	f_i = 1 - 1.3 GHz	$V_{i(rms)}$	40/–15	–	300/2.6	mV/dBm
Oscillator frequency	C_{series} = 27 pF	f_{OSC}	–	4	–	MHz
Output current						
open-collector		I_{OL}	–	–	10	mA
current limited		I_{OL}	–	1	–	mA
Operating ambient temperature range		T_{amb}	–10	–	+ 80	°C
Storage temperature range		T_{stg}	–40	0	+ 125	°C
Thermal resistance		$R_{th\ j\text{-}a}$	–	70	80	K/W

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

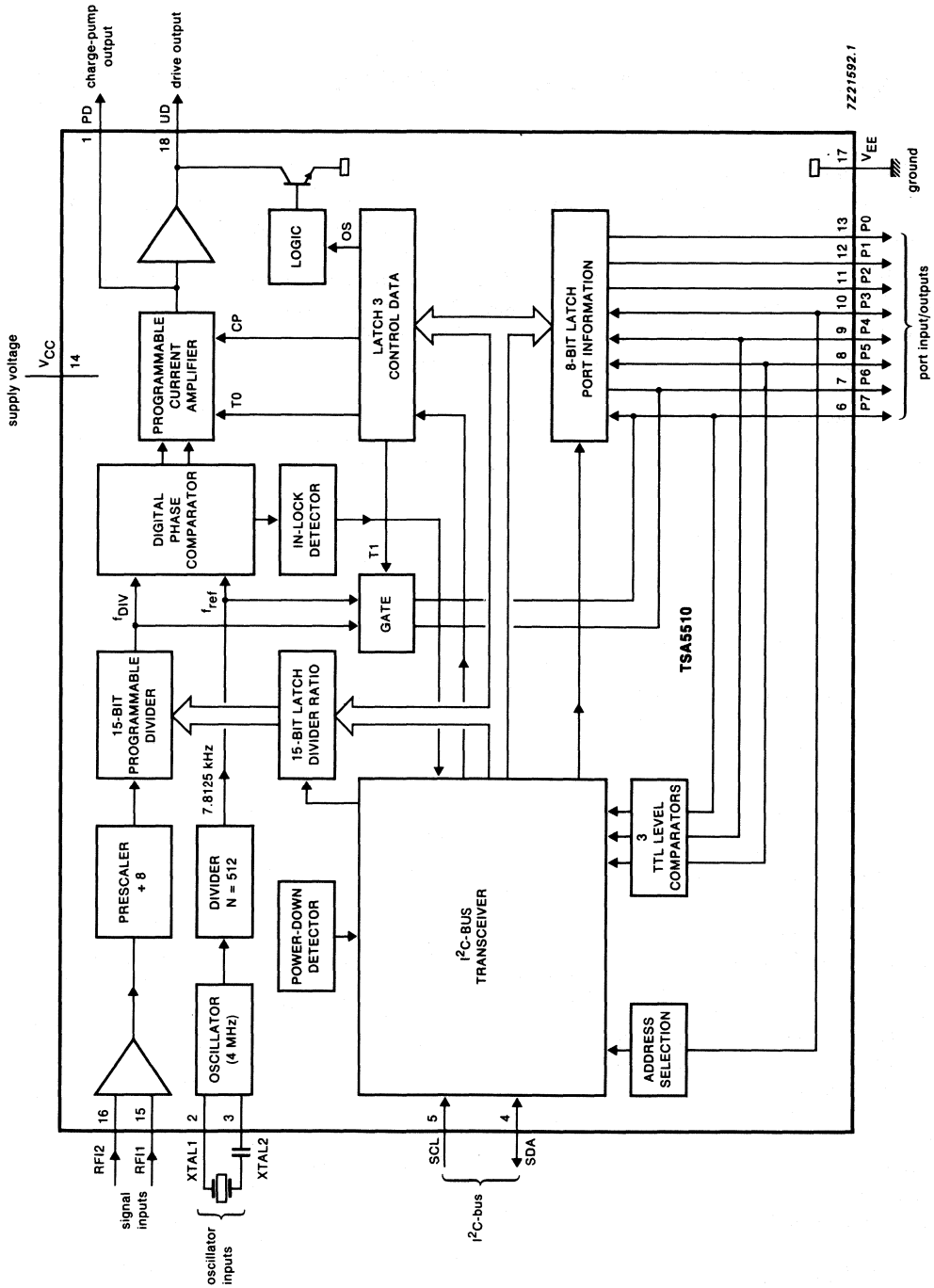


Fig. 1 Block diagram.

PINNING

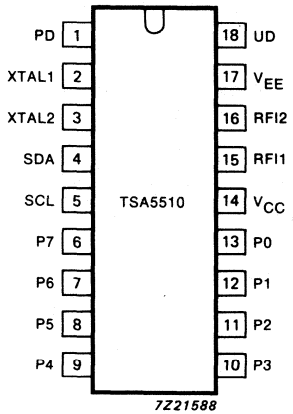


Fig. 2 Pinning diagram.

1	PD	charge-pump output	
2	XTAL1	crystal oscillator input 1	
3	XTAL2	crystal oscillator input 2	
4	SDA	serial data input/output	I²C-bus
5	SCL	serial clock input	I²C-bus
6	P7	port 7 I/O (general purpose)	
7	P6	port 6 output	
8	P5	port 5 I/O (general purpose)	
9	P4	port 4 I/O (general purpose)	
10	P3	port 3 I/O for address selection	
11	P2	port 2 output	
12	P1	port 1 output	
13	P0	port 0 output	
14	V_{CC}	positive supply voltage	
15	RFI1	UHF/VHF signal input 1	
16	RFI2	UHF/VHF signal input 2	
17	V_{EE}	ground	
18	UD	operational amplifier drive output	

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TSA5510 is controlled via the 2-wire I²C-bus. For programming there is one 7-bit module address and a R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode: R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are required to fully program the TSA5510. The bus transceiver has an auto-increment facility which permits the programming of the TSA5510 within one single transmission (address + 4 data bytes).

The TSA5510 can also be partially programmed at the condition that the first data byte following address is byte 2 or byte 4. The meaning of the bits in the data byte is explained in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge-pump and ports information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on ports are set to a high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz oscillator by 512. As the input of the UHF/VHF signal is first divided by 8 the minimum step is 62.5 kHz.

FUNCTIONAL DESCRIPTION (continued)

READ mode: R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5510 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5510 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.

A second data byte can be read out of the TSA5510 if the processor generates an acknowledge on the SDA line. If no acknowledge is generated, end of transmission will occur. The TSA5510 will then release the data line to allow the processor to generate a STOP condition.

When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.

The power-on reset (POR) flag is set to logic 1 when V_{CC} drops below 3 V and at power-on. It is reset when an end of data is detected by the TSA5510 (end of READ sequence).

A control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked.

Bits I0, I1 and I2 represent the status of the I/O ports P4, P5 and P7 respectively. A logic 0 indicates a low level and a logic 1 indicates a high level (TTL levels).

Address selection (see Table 3)

The module address contains programmable address bits (MA0 and MA1) which offer together with the I/O port P3 the possibility of having up to 3 synthesizers in one system. The relationship between bits MA0 and MA1 and the input voltage on I/O port P3 is given in Table 4.

Table 1 Write data format

	MSB							LSB		
address	1	1	0	0	0	MA1	MA0	0*	A	byte 1
programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
I/O port control bits	P7	P6	P5	P4	P3	P2	P1	P0	A	byte 5

* R/W bit = 0 for WRITE mode;
R/W bit = 1 for READ mode.

Where

A is the acknowledge bit.
N14 to N0 are the programmable divider bits;
$N = N14 \times 2^{14} + N13 \times 2^{13} + \ldots + N1 \times 2 + N0$.
CP is the charge-pump current;
CP = 0 : 50 μA
CP = 1 : 220 μA.
P3 to P0 = 1 : limited current output is active.
P7 to P4 = 1 : open-collector output is active.
P7, P0 = 0 : outputs are in high-impedance state.
T1, T0, OS = 0, 0, 0 : normal operation.
T1 = 1, P6 = f_{ref}, P7 = f_{DIV}.
T0 = 1 : 3-state charge pump.
OS = 1 : operational amplifier output is switched off (variable capacitor drive is disabled).

Table 2 Read data format

	MSB									LSB
address	1	1	0	0	0	MA1	MA0	1*	A	byte 1
status byte	0	FL	I2	I1	I0	X	X	X	A	byte 2

Where

POR is the power-on reset flag;
POR = 1 : on power-on.
FL is the in-lock flag;
FL = 1 : loop is phase-locked.
I2, I1, I0 : digital information for I/O ports P4, P5 and P7 respectively.
X = don't care

Table 3 Address selection

MA1	MA0	voltage input on P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

* R/$\overline{W}$ bit = 0 for WRITE mode;
R/$\overline{W}$ bit = 1 for READ mode.

DEVELOPMENT DATA

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection in accordance with specification MIL-STD-883C, class A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 14)	V_{CC}	−0.3	+ 6.0	V
Charge-pump output voltage (pin 1)	V_{1-17}	−0.3	V_{CC}	V
Crystal oscillator input voltage (pin 2)	V_{2-17}	−0.3	V_{CC}	V
Serial data input/output voltage (pin 4)	V_{4-17}	−0.3	+ 6.0	V
Serial clock input voltage (pin 5)	V_{5-17}	−0.3	+ 6.0	V
Ports P7 to P3 input/output voltage (pins 6 to 10)	$V_{I/O}$	−0.3	+ 16.0	V
Ports P2 to P0 output voltage (pins 11 to 13)	V_O	−0.3	+ 16.0	V
UHF/VHF signal input voltage (pin 15)	V_{15-17}	−0.3	+ 2.5	V
UHF/VHF signal input voltage (pin 16)	V_{16-17}	−0.3	+ 2.5	V
Drive output voltage (pin 18)	V_{18-17}	−0.3	V_{CC}	V
Output current				
output ports (open collector)	I_{OL}	−1	+ 15	mA
serial data output (open collector)	I_{OL}	−1	+ 5	mA
Storage temperature range	T_{stg}	−40	+ 125	°C
Operating ambient temperature range	T_{amb}	−10	+ 80	°C
Junction temperature	T_j	–	+ 125	°C
Short-circuit time	t_{sc}	–	10	s

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a(max)}$ = 80 K/W

CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{CC}	4.5	5.0	5.5	V
Supply current		I_{CC}	25	35	50	mA
Input frequency range		f_i	64	–	1300	MHz
Programmable divider		N_n	256	–	32767	bits
Oscillator frequency	C_{series} = 27 pF	f_{OSC}	–	4	–	MHz
Prescaler						
Input sensitivity	see Fig. 3					
Input voltage	V_{CC} = 5 V ± 10%; T_{amb} = −10 to 80 °C					
(RMS value)						
	f_i = 80 to 150 MHz	$V_{i(rms)}$	12/−25	–	300/2.6	mV/dBm
	f_i = 150 to 1000 MHz	$V_{i(rms)}$	9/−28	–	300/2.6	mV/dBm
	f_i = 1 to 1.3 GHz	$V_{i(rms)}$	40/−15	–	300/2.6	mV/dBm
Input impedance	see Fig. 4					
		R_i	–	50	–	Ω
		C_i	–	2	–	pF
Output ports						
Port P3	current limited					
Leakage current		I_{LO}	–	–	10	μA
Sink current		I_{sink}	0.7	1.0	1.5	mA
Ports P4 to P7*	open-collector					
Leakage current	V_9 = 13.5 V	I_{LO}	–	–	10	μA
Output voltage LOW	I_9 = 10 mA**	V_{OL}	–	–	0.7	V

DEVELOPMENT DATA

* When the port is active, the collector voltage may not exceed 6 V.

** Measured with a single open-collector port active.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input ports						
Port P3						
Input current LOW	V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH	V_{IH} = 13.5 V	I_{IH}	–	–	10	μA
Ports P4, P5, P7						
Input voltage LOW		V_{IL}	–	–	0.8	V
Input voltage HIGH		V_{IH}	2.7	–	–	V
Input current LOW	V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH	V_{IH} = 13.5 V	I_{IH}	–	–	10	μA
Inputs						
SCL, SDA						
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	5.5	V
Input current LOW	V_{CC} = 5 V; V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH	V_{CC} = 0 V; V_{IH} = 5 V	I_{IH}	–	–	10	μA
	V_{CC} = 5 V; V_{IH} = 5 V	I_{IH}	–	–	10	μA
Outputs						
SDA	open-collector					
Leakage current	V_4 = 5.5 V	I_{LO}	–	–	10	μA
Output voltage LOW	I_4 = 3 mA	V_{OL}	–	–	0.4	V
PD						
Output current LOW	bit CP = logic 0	$\|I_{OL}\|$	22	50	75	μA
Output current HIGH	bit CP = logic 1	$\|I_{OH}\|$	90	220	300	μA
Output voltage LOW	in-lock	V_{OL}	1.5	–	2.5	V
UD (test mode)	bit T0 = logic 1					
Output current	V_6 = 0.8 V; I_1 = 90 μA	I_{16}	500	–	–	μA
Output voltage	V_1 = 0 V	V_{16}	–	–	100	mV
Output voltage when switched off	bits T0, OS = logic 1; V_1 = 2 V	V_{16}	–	–	200	mV

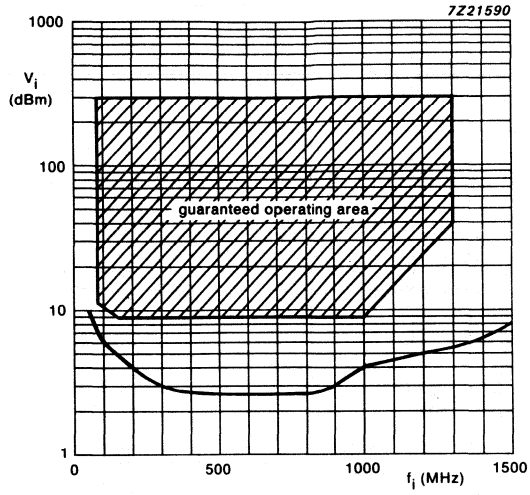


Fig. 3 Prescaler typical input sensitivity curve: V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to + 80 °C.

DEVELOPMENT DATA

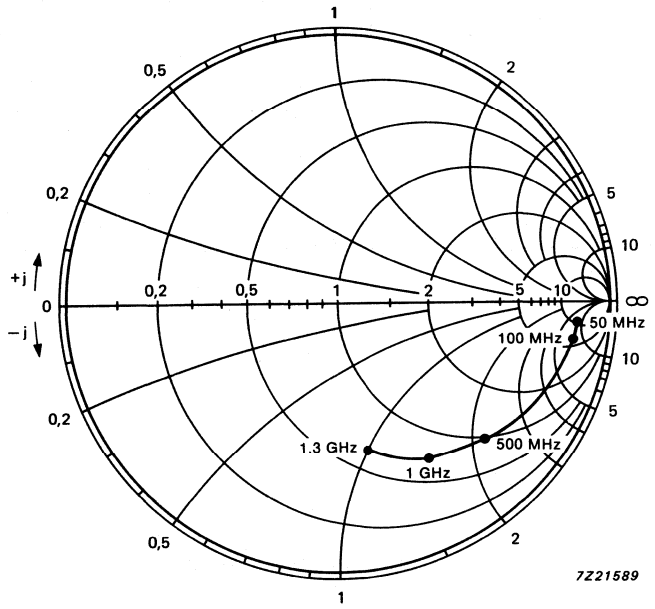


Fig. 4 Prescaler Smith chart of typical input impedance: V_{CC} = 5 V; reference value = 50 Ω.

APPLICATION INFORMATION

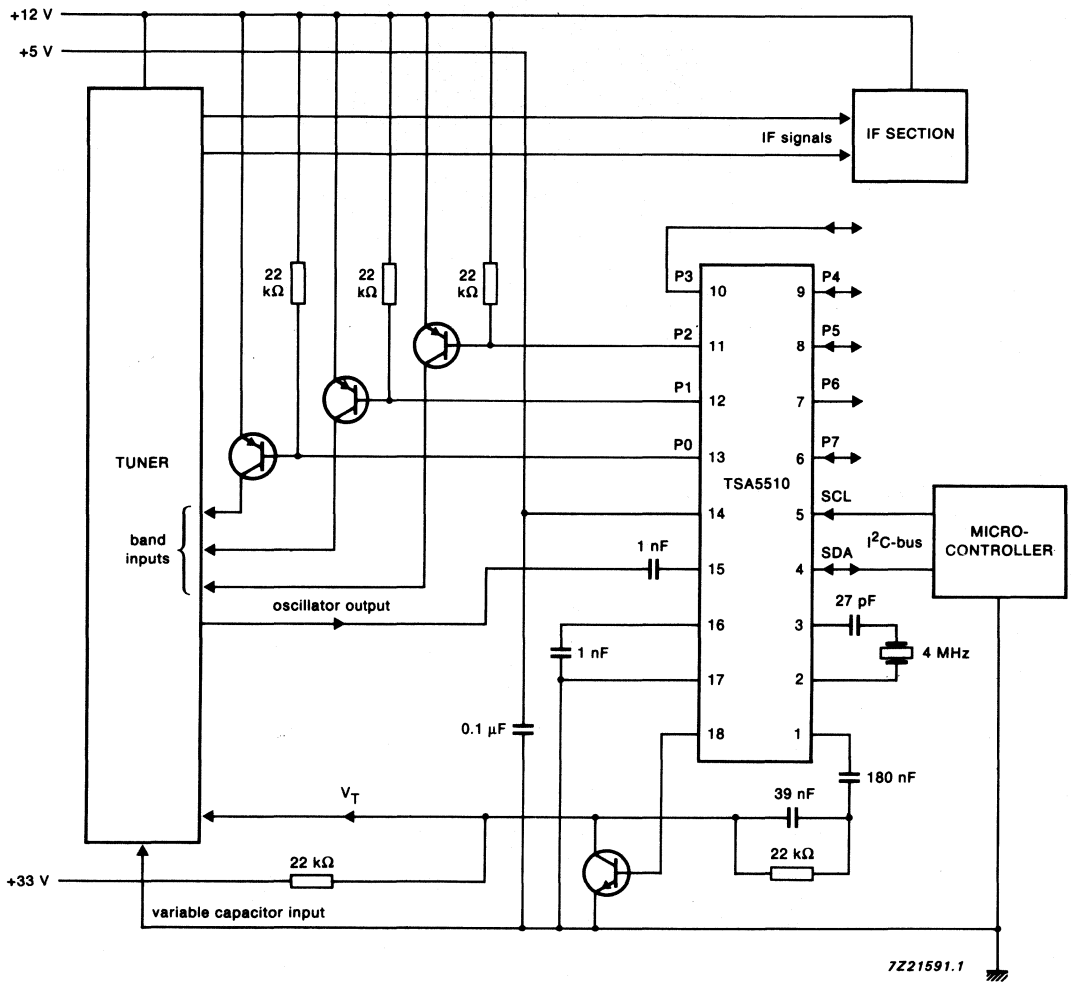


Fig. 5 Typical application diagram.

1.3 GHz I²C-BUS CONTROLLED FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The TSA5510T is a bipolar single-chip frequency synthesizer. It performs all the tuning functions of a phase-locked loop (PLL) television tuning system. The IC is designed for application in all types of television receivers.

Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, program the output ports and set the programmable current amplifier (charge pump) current. Three of these ports can also be used as general purpose I/O ports.

Digital information concerning these ports can be read from the TSA5510T on the serial data line (SDA), one status byte, during a READ operation.

A flag is set when the PLL is "in-lock" and read during a READ operation.

The TSA5510T has one fixed I²C-bus address and 3 programmable addresses, which can be programmed by applying a specific voltage to Port 3.

The phase comparator operates at a frequency of 7.8125 kHz when a 4 MHz crystal is used.

Features

- Complete 1.3 GHz single-chip system
- Low power: 5 V at 35 mA
- I²C-bus programming
- In-lock flag
- Variable capacitor drive disable
- Low radiation
- Address selection for Picture-in Picture Controller (PIPCO), Direct Broadcast Satellite tuner (DBS), etc.
- 5 controllable outputs, 4 bidirectional
- Power-down flag

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)		V_{CC}	4.5	5.0	5.5	V
Supply current		I_{CC}	25	35	50	mA
Input frequency range		f_i	64	–	1300	MHz
Input voltage (RMS value)	f_i = 80 - 150 MHz	$V_{i(rms)}$	12/–25	–	300/2.6	mV/dBm
	f_i = 150 - 1000 MHz	$V_{i(rms)}$	9/–28	–	300/2.6	mV/dBm
	f_i = 1 - 1.3 GHz	$V_{i(rms)}$	40/–15	–	300/2.6	mV/dBm
Oscillator frequency	C_{series} = 27 pF	f_{OSC}	–	4	–	MHz
Output current						
open-collector		I_{OL}	–	–	10	mA
current limited		I_{OL}	–	1	–	mA

PACKAGE OUTLINE

16-lead DIL; plastic (SO16; SOT109A)

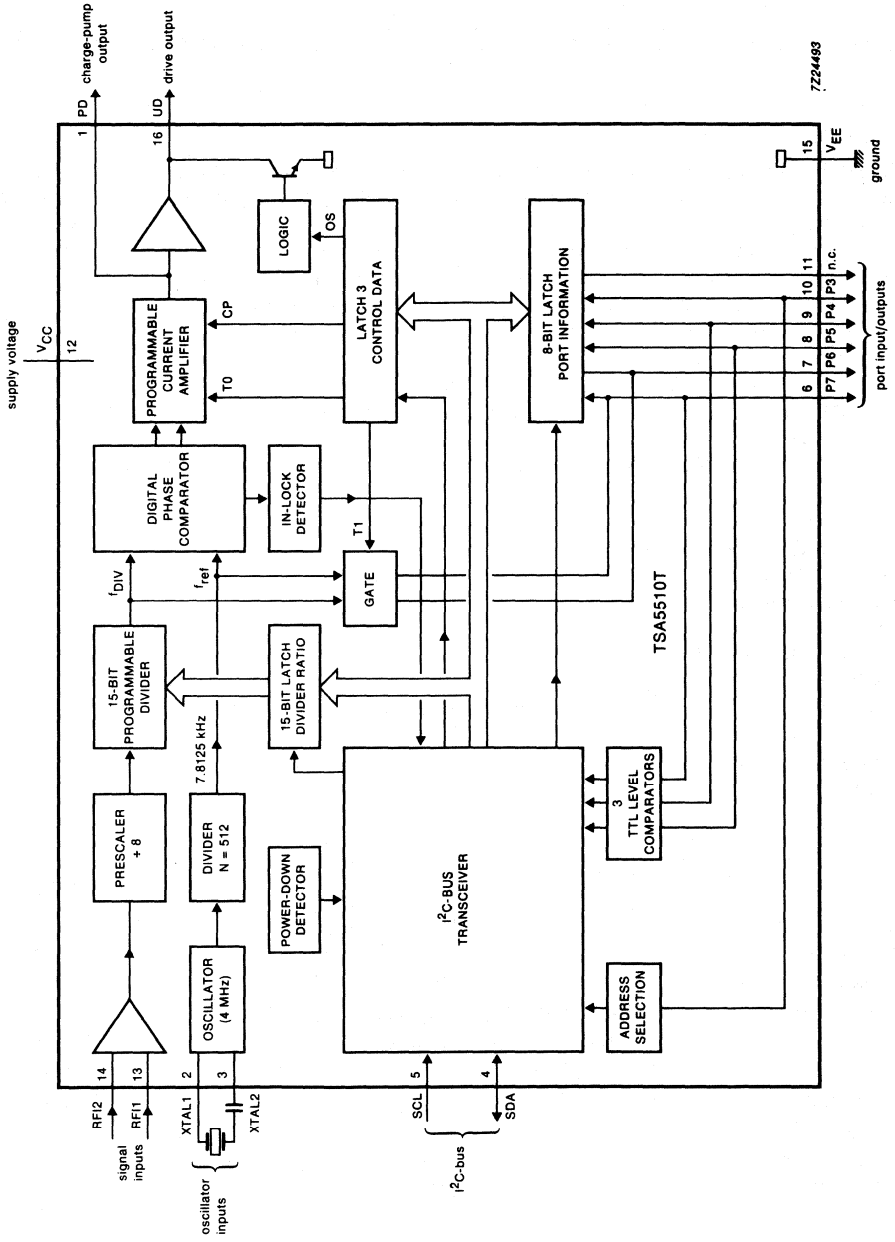


Fig.1 Block diagram.

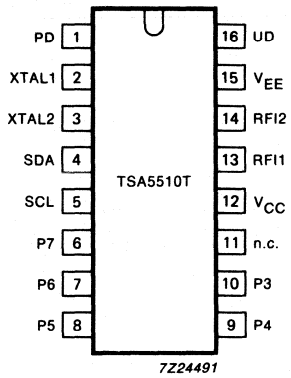


Fig.2 Pinning diagram.

PINNING

1	PD	charge-pump output	
2	XTAL1	crystal oscillator input 1	
3	XTAL2	crystal oscillator input 2	
4	SDA	serial data input/output	I²C-bus
5	SCL	serial clock input	I²C-bus
6	P7	port 7 I/O (general purpose)	
7	P6	port 6 output	
8	P5	port 5 I/O (general purpose)	
9	P4	port 4 I/O (general purpose)	
10	P3	port 3 I/O for address selection	
11	n.c.	not connected	
12	V_{CC}	positive supply voltage	
13	RFI1	UHF/VHF signal input 1	
14	RFI2	UHF/VHF signal input 2	
15	V_{EE}	ground	
16	UD	operational amplifier drive output	

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TSA5510T is controlled via the 2-wire I²C-bus. For programming there is one 7-bit module address and a R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode: R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are required to fully program the TSA5510T. The bus transceiver has an auto-increment facility which permits the programming of the TSA5510T within one single transmission (address + 4 data bytes).

The TSA5510T can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data byte is explained in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge-pump and ports information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on, ports are set to a high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz oscillator by 512. As the input of the UHF/VHF signal is first divided by 8 the minimum step is 62.5 kHz.

FUNCTIONAL DESCRIPTION= (continued)

READ mode: R/$\overline{W}$ = 1 (see Table 2)

Data can be read from the TSA5510T by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5510T generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line when the SCL clock signal is HIGH.

A second data byte can be read from the TSA5510T if the processor generates an acknowledge on the SDA line. If no acknowledge is generated, end of transmission will occur. The TSA5510T will then release the data line to allow the processor to generate a STOP condition.

When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.

The power-on reset (POR) flag is set to logic 1 when V_{CC} drops below 3 V and at power-on. It is reset when an end of data is detected by the TSA5510T (end of READ sequence).

Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked.

Bits I0, I1 and I2 represent the status of the I/O ports P4, P5 and P7 respectively. A logic 0 indicates a low level and a logic 1 indicates a high level (TTL levels).

Address selection (see Table 3)

The module address contains programmable address bits (MA0 and MA1) which offer, together with the I/O port P3, the possibility of having up to 3 synthesizers in one system. The relationship between bits MA0 and MA1 and the input voltage on I/O port P3 is given in Table 3.

Table 1 Write data format

	MSB							LSB		
address	1	1	0	0	0	MA1	MA0	0*	A	byte 1
programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
charge-pump and test bits	1	CP	T1	T0	1	1	1	0S	A	byte 4
I/O port control bits	P7	P6	P5	P4	P3	–	–	–	A	byte 5

Where

A is the acknowledge bit.
N14 to N0 are the programmable divider bits;
$N = N14 \times 2^{14} + N13 \times 2^{13} + \ldots + N1 \times 2 + N0$.
CP is the charge-pump current; CP = 0 : 50 μA; CP = 1 : 220 μA
P3 = 1 : limited current output is active.
P7 to P4 = 1 : open-collector output is active.
P7 = 0 : output is in high-impedance state.
T1, T0, 0S = 0, 0, 0 : normal operation.
T1 = 1, P6 = f_{ref}, P7 = f_{DIV}.
T0 = 1 : 3-state charge pump.
0S = 1 : operational amplifier output is switched off (variable capacitor drive is disabled).

Table 2 Read data format

	MSB								LSB	
address	1	1	0	0	0	MA1	MA0	1*	A	byte 1
status byte	0	FL	I2	I1	I0	X	X	X	A	byte 2

Where

POR is the power-on reset flag;
POR = 1 : on power-on.
FL is the in-lock flag;
FL = 1 : loop is phase-locked.
I2, I1, I0 : digital information for I/O ports P7, P5 and P4 respectively.
X = don't care.

R/$\overline{W}$ bit = 0 for WRITE mode;
R/$\overline{W}$ bit = 1 for READ mode.

Table 3 Address selection

MA1	MA0	voltage input on P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

DEVELOPMENT DATA

* Accuracy is 1/2 LSB.

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection in accordance with specification MIL-STD-883C, class A.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 12)	V_{CC}	−0.3	+6.0	V
Charge-pump output voltage (pin 1)	$V_{1\text{-}15}$	−0.3	V_{CC}	V
Crystal oscillator input voltage (pin 2)	$V_{2\text{-}15}$	−0.3	V_{CC}	V
Serial data input/output voltage (pin 4)	$V_{4\text{-}15}$	−0.3	+6.0	V
Serial clock input voltage (pin 5)	$V_{5\text{-}15}$	−0.3	+6.0	V
Ports P7 to P3 input/output voltage (pins 6 to 10)	$V_{I/O}$	−0.3	+16.0	V
UHF/VHF signal input voltage (pin 13)	$V_{13\text{-}15}$	−0.3	+2.5	V
UHF/VHF signal input voltage (pin 14)	$V_{14\text{-}15}$	−0.3	+2.5	V
Drive output voltage (pin 16)	$V_{16\text{-}15}$	−0.3	V_{CC}	V
Output current				
output ports (open collector)	I_{OL}	−1	+15	mA
serial data output (open collector)	I_{OL}	−1	+5	mA
Storage temperature range	T_{stg}	−40	+125	°C
Operating ambient temperature range	T_{amb}	−10	+80	°C
Junction temperature	T_j	−	+125	°C
Short-circuit time	t_{sc}	−	10	s

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a(max)}$ = 80 K/W

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{CC}	4.5	5.0	5.5	V
Supply current		I_{CC}	25	35	50	mA
Input frequency range		f_i	64	–	1300	MHz
Programmable divider		N_n	256	–	32767	bits
Oscillator frequency	C_{series} = 27 pF	f_{OSC}	–	4	–	MHz
Prescaler						
Input sensitivity	see Fig.3					
Input voltage	V_{CC} = 5 V ± 10%; T_{amb} = −10 to 80 °C					
(RMS value)						
	f_i = 80 to 150 MHz	$V_{i(rms)}$	12/−25	–	300/2.6	mV/dBm
	f_i = 150 to 1000 MHz	$V_{i(rms)}$	9/−28	–	300/2.6	mV/dBm
	f_i = 1 to 1.3 GHz	$V_{i(rms)}$	40/−15	–	300/2.6	mV/dBm
Input impedance	see Fig.4					
		R_i	–	50	–	Ω
		C_i	–	2	–	pF
Output ports						
Port P3	current limited					
Leakage current		I_{LO}	–	–	10	μA
Sink current		I_{sink}	0.7	1.0	1.5	mA
Ports P4 to P7*	open-collector					
Leakage current	V_9 = 13.5 V	I_{LO}	–	–	10	μA
Output voltage LOW	I_9 = 10 mA**	V_{OL}	–	–	0.7	V
Input ports						
Port P3						
Input current LOW	V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH	V_{IH} = 13.5 V	I_{IH}	–	–	10	μA
Ports P4, P5, P7						
Input voltage LOW		V_{IL}	–	–	0.8	V
Input voltage HIGH		V_{IH}	2.7	–	–	V
Input current LOW	V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH	V_{IH} = 13.5 V	I_{IH}	–	–	10	μA

* When the port is active, the collector voltage may not exceed 6 V.

** Measured with a single open-collector port active.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs						
SCL, SDA						
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	5.5	V
Input current LOW	V_{CC} = 5 V; V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH						
	V_{CC} = 0 V; V_{IH} = 5 V	I_{IH}	–	–	10	μA
	V_{CC} = 5 V; V_{IH} = 5 V	I_{IH}	–	–	10	μA
Outputs						
SDA	open-collector					
Leakage current	V_4 = 5.5 V	I_{LO}	–	–	10	μA
Output voltage LOW	I_4 = 3 mA	V_{OL}	–	–	0.4	V
PD						
Output current LOW	bit CP = logic 0	$\|I_{OL}\|$	22	50	75	μA
Output current HIGH	bit CP = logic 1	$\|I_{OH}\|$	90	220	300	μA
Output voltage LOW	in-lock	V_{OL}	1.5	–	2.5	V
UD (test mode)	bit T0 = logic 1					
Output current	V_{16} = 0.8 V; I_1 = 90 μA	I_{16}	500	–	–	μA
Output voltage	V_1 = 0 V	V_{16}	–	–	100	mV
Output voltage when switched off	bits T0, 0S = logic 1; V_1 = 2 V	V_{16}	–	–	200	mV

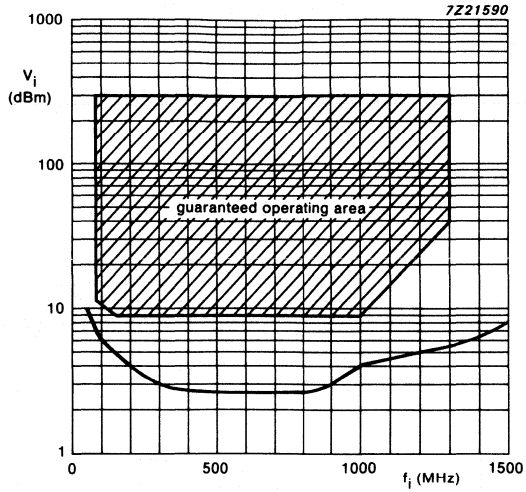


Fig. 3 Prescaler typical input sensitivity curve: V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to + 80 °C.

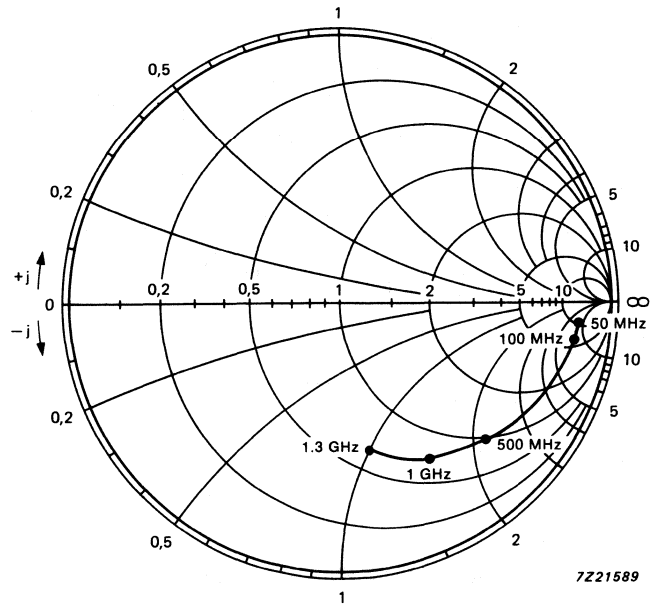


Fig. 4 Prescaler Smith chart of typical input impedance: V_{CC} = 5 V; reference value = 50 Ω.

APPLICATION INFORMATION

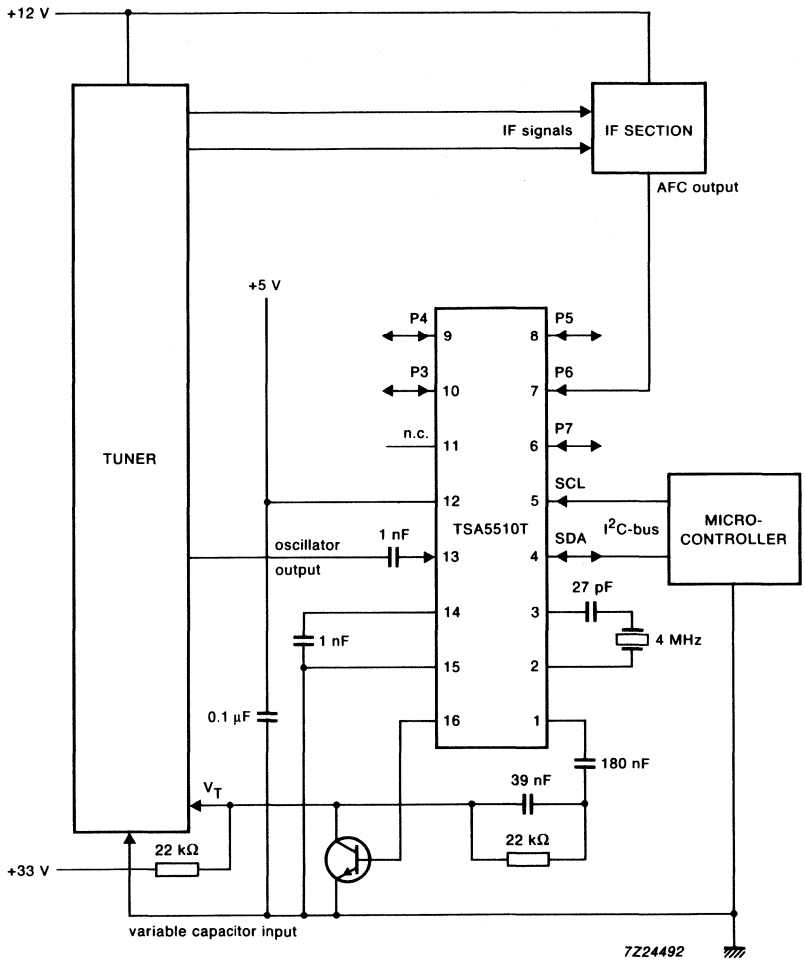


Fig.5 Typical application diagram.

RADIO TUNING PLL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The TSA6057/6057T is a bipolar single chip frequency synthesizer manufactured in SUBILO-N technology (components laterally separated by oxide). It performs all the tuning functions of a PLL radio tuning system. The IC is designed for application in all types of radio receivers.

Features

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high performance one input (two output) tuning voltage amplifier for the AM and FM loop filters
- On-chip 2-level current amplifier (charge pump) to adjust the loop gain
- Only one reference oscillator (4 MHz) for both AM and FM
- High speed tuning due to a powerful digital memory phase detector
- 40 kHz output reference frequency for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100)
- Oscillator frequency ranges of: 512 kHz to 30 MHz and 30 MHz to 150 MHz
- Three selectable reference frequencies of 1 kHz, 10 kHz or 25 kHz for both tuning ranges
- Serial 2-wire I^2C-bus interface to a microcomputer and one programmable address input
- Software controlled bandswitch output

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 3		$V_{CC1} = V_{3-4}$	4.5	5.0	5.5	V
pin 16		$V_{CC2} = V_{16-4}$	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_3	12	20	28	mA
pin 16		I_{16}	0.7	1.0	1.3	mA
Max. input frequency on AM_I		f_{iAM}	30	–	–	MHz
Min. input frequency on AM_I		f_{iAM}	–	–	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	–	–	MHz
Min. input frequency on FM_I		f_{iFM}	–	–	30	MHz
Input voltage on AM_I (RMS value)	$V_{iFM} = 0$ V	$V_{iAM(rms)}$	30	–	500	mV
Input voltage on FM_I (RMS value)	$V_{iAM} = 0$ V	$V_{iFM(rms)}$	20	–	300	mV
Total power dissipation		P_{tot}	–	0.14	–	W
Operating ambient temperature range		T_{amb}	–30	–	+ 85	°C

PACKAGE OUTLINES

TSA6057: 16-lead DIL; plastic (SOT38).
TSA6057T: 16-lead minipack; plastic (SO16L; SOT162A).

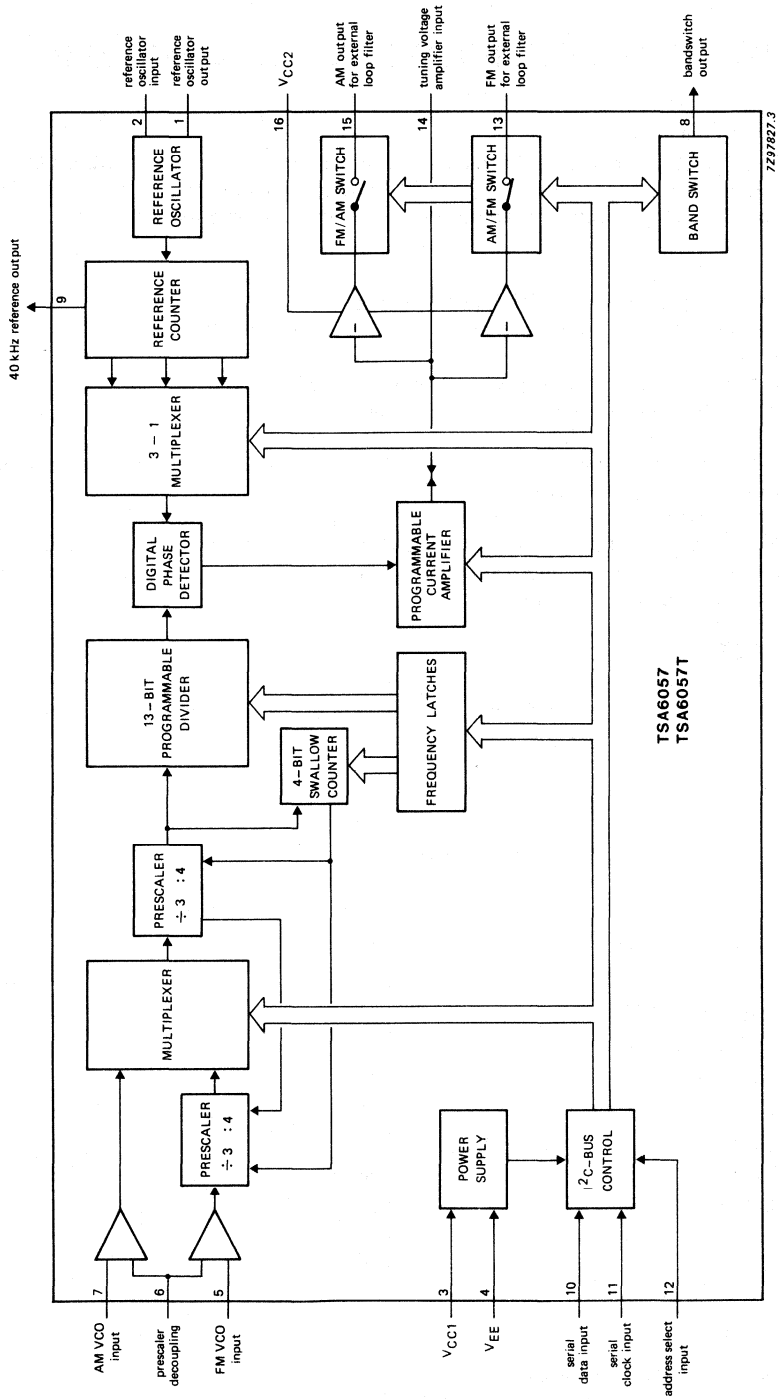


Fig.1 Block diagram.

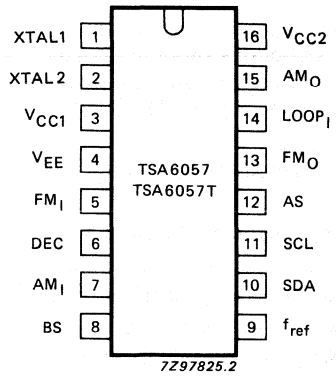


Fig.2 Pinning diagram.

PINNING

1	XTAL1	reference oscillator output
2	XTAL2	reference oscillator input
3	V_{CC1}	positive supply voltage
4	V_{EE}	ground
5	FM_I	FM VCO input
6	DEC	prescaler decoupling
7	AM_I	AM VCO input
8	BS	bandswitch output
9	f_{ref}	40 kHz reference output
10	SDA	serial data input (I²C-bus)
11	SCL	serial clock input (I²C-bus)
12	AS	address select input (I²C-bus)
13	FM_O	FM output for external loop filter
14	$LOOP_I$	tuning voltage amplifier input
15	AM_O	AM output for external loop filter
16	V_{CC2}	positive supply voltage

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TSA6057/6057T contains the following parts and facilities:

- Separate input amplifiers for the AM and FM VCO-signals.
- A prescaler with the divisors 3:4 on AM and 15:16 on FM, a multiplexer to select AM or FM and a 4-bit programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter. The reference frequency can be 1 kHz, 10 kHz or 25 kHz and is applied to the digital memory phase detector. The reference counter also outputs a 40 kHz reference frequency to pin 9 for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100).
- A programmable current amplifier (charge pump) which consists of a 5 μA and a 450 μA current source. This allows adjustment of loop gain, thus providing high current-high speed tuning and low current-stable tuning.
- A one input – two output tuning voltage amplifier. One output is connected to the external AM loop filter and the other output to the external FM loop filter. Under software control, the AM output is switched to a high impedance state by the FM/AM switch in the FM position and the FM output is switched to a high impedance state by the AM/FM switch in the AM position. The outputs can deliver a tuning voltage of up to 10.5 V.
- An I²C-bus interface with data latches and control logic. The I²C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I²C-bus specification is available on request.
- A software-controlled bandswitch output.

FUNCTIONAL DESCRIPTION (continued)

Controls

The TSA6057/6057T is controlled via the 2-wire I²C-bus. For programming there is one module address, a logic 0 R/W bit, a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address select input AS (pin 12) makes it possible to operate two TSA6057s in one system.

The auto increment facility of the I²C-bus allows programming of the TSA6057/6057T within one transmission (address + subaddress + 4 data bytes).

- The TSA6057/6057T can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is shown in Fig.3 and are described in sections (a) to (f).

(a) The bits S0 to S16 (DB0: D7-D1; DB1: D7-D0; DB2: D1-D0) together with bit FM/AM (DB2: D5) are used to set the divisor of the input frequency at inputs AM_I (pin 7) or FM_I (pin 5). If the system is in lock the following is valid:

FM/$\overline{AM}$	input frequency (f_i)	input
0	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S13 \times 2^{13} + S14 \times 2^{14}) \times f_{ref}$	AM_I
1	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S15 \times 2^{15} + S16 \times 2^{16}) \times f_{ref}$	FM_I

Where

The minimum dividing ratio for AM mode is $2^6 = 64$
The minimum dividing ratio for FM mode is $2^8 = 256$

(b) The bit CP is used to control the charge pump current (DB0: D0).

CP	current
0	low
1	high

(c) The bits REF1 and REF2 are used to set the reference frequency applied to the phase detector (DB2: D7-D6).

REF1	REF2	frequency (kHz)
0	0	1
0	1	10
1	0	25
1	1	none

(d) The bit $\overline{FM}$/AM OPAMP controls the switch AM/FM; FM/AM in the tuning voltage amplifier output circuitry (DB2: D4).

$\overline{FM}$/AM OPAMP	switch FM/AM	switch AM/FM
1	closed	open
0	open	closed

(e) The bit BS controls the open collector bandswitch output (DB2: D2).

BS	bandswitch output
1	sink current
0	floating

(f) The data byte DB3 must be set to 0 . . . . . 0. It is also used for test purposes.

DEVELOPMENT DATA

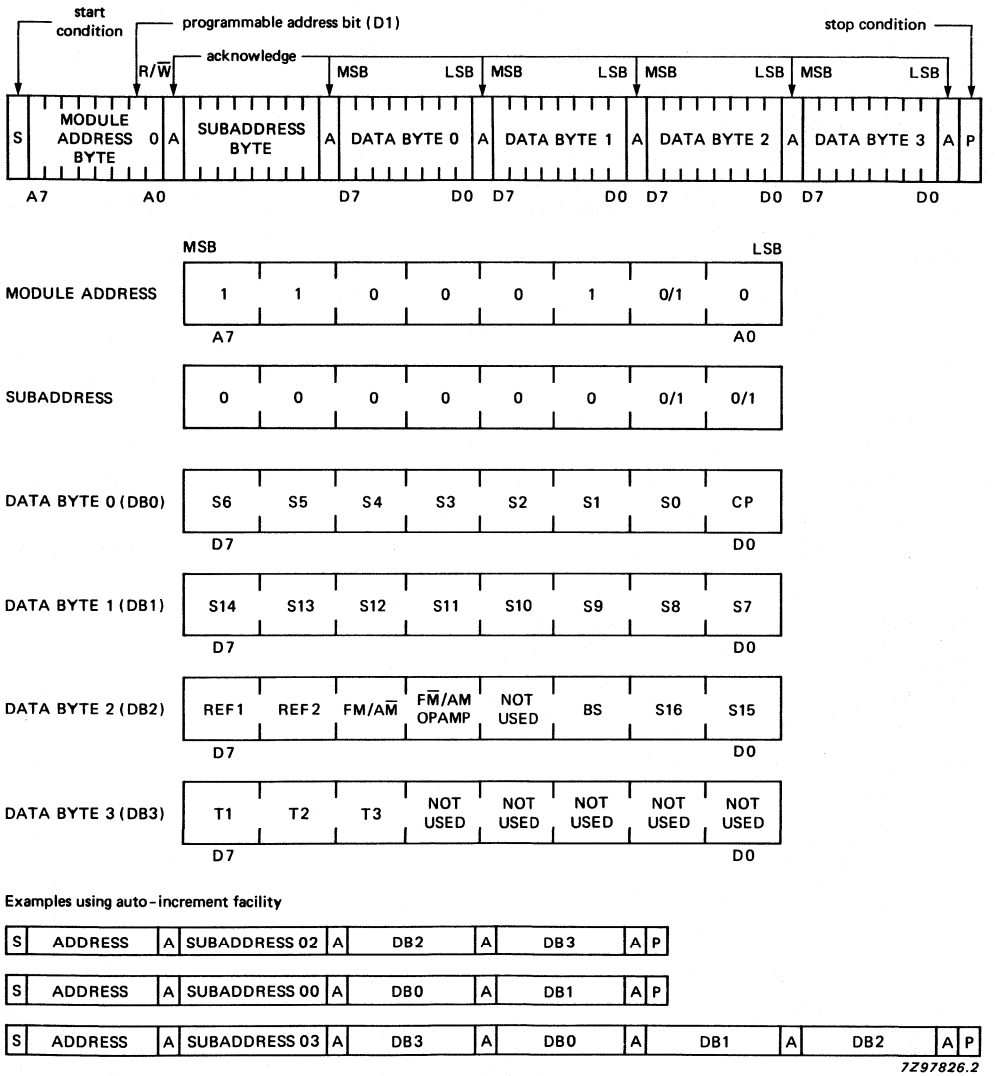


Fig.3 Bit organization.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	$V_{CC1} = V_{3-4}$	−0.3	5.5	V
Supply voltage (pin 16)	$V_{CC2} = V_{16-4}$	V_{CC1}	12.5	V
Total power dissipation	P_{tot}	−	0.85	W
Operating ambient temperature	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{CC1} = 5 V; V_{CC2} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_{CC1}	4.5	5.0	5.5	V
Supply voltage (pin 16)		V_{CC2}	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_{CC1}	12	20	28	mA
pin 16		I_{CC2}	0.7	1.0	1.3	mA
I²C-bus inputs (SDA; SCL)						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.5	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
SDA output	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	−	−	0.4	V
AS input						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.0	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
RF input (AM; FM)						
Max. input frequency on AM_I		f_{iAM}	30	−	−	MHz
Min. input frequency on AM_I		f_{iAM}	−	−	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	−	−	MHz
Min. input frequency on FM_I		f_{iFM}	−	−	30	MHz
Input voltage on AM_I (RMS value)	V_{iFM} = 0 V measured in Fig.4	$V_{iAM(rms)}$	30	−	500	mV
Input impedance AM_I						
resistance		R_{AM}	−	5.9	−	kΩ
capacitance		C_{AM}	−	2	−	pF

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
RF input (continued)						
Input voltage on FM_I (RMS value)	V_{iAM} = 0 V measured in Fig.4	$V_{iFM(rms)}$	20	–	300	mV
Input impedance FM_I						
resistance		R_{FM}	–	3.6	–	kΩ
capacitance		C_{FM}	–	2	–	pF
Oscillator (XTAL1; XTAL2)						
Crystal resonance resistance (4 MHz)	see Fig.5	R_{XTAL}	–	–	150	Ω
Programmable charge pump						
Output current to loop filter						
bit CP = logic 0		I_{chp}	3	5	7	μA
bit CP = logic 1		I_{chp}	400	500	600	μA
Ripple rejection	f_{ripple} = 100 Hz					
20 log $\Delta V_{CC1}/\Delta V_O$		RR	40	50	–	dB
20 log $\Delta V_{CC2}/\Delta V_O$		RR	40	50	–	dB
Bandswitch output (pin 8)						
Output voltage HIGH		V_{OH}	–	–	12	V
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.8	V
Output leakage current	V_{OH} = 12 V	I_{LO}	–	–	10	μA
Reference frequency output (pin 9)						
Output frequency	4 MHz crystal	f_{ref}	–	40	–	kHz
Output voltage HIGH	I_{source} = 5 μA	V_{OH}	1.2	1.4	1.7	V
Output voltage LOW		V_{OL}	–	0.1	0.2	V
Tuning voltage amplifier outputs						
AM output (pin 15)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
FM output (pin 13)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
Impedance of switched off output		$Z_{O(off)}$	5	–	–	MΩ
Input bias current (absolute value)		I_{bias}	–	1	5	nA

SENSITIVITY MEASUREMENT

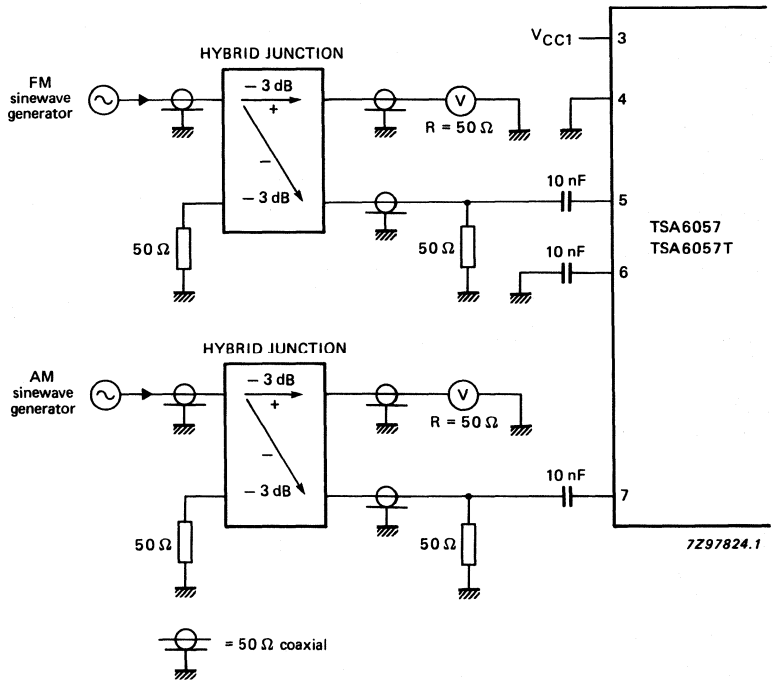


Fig.4 Prescaler input sensitivity.

APPLICATION INFORMATION

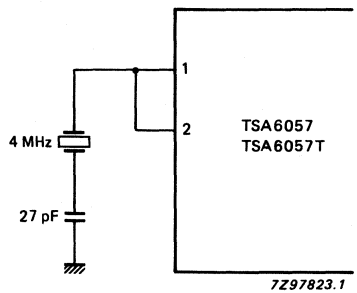


Fig.5 Crystal connection (4 MHz).

DEVELOPMENT DATA

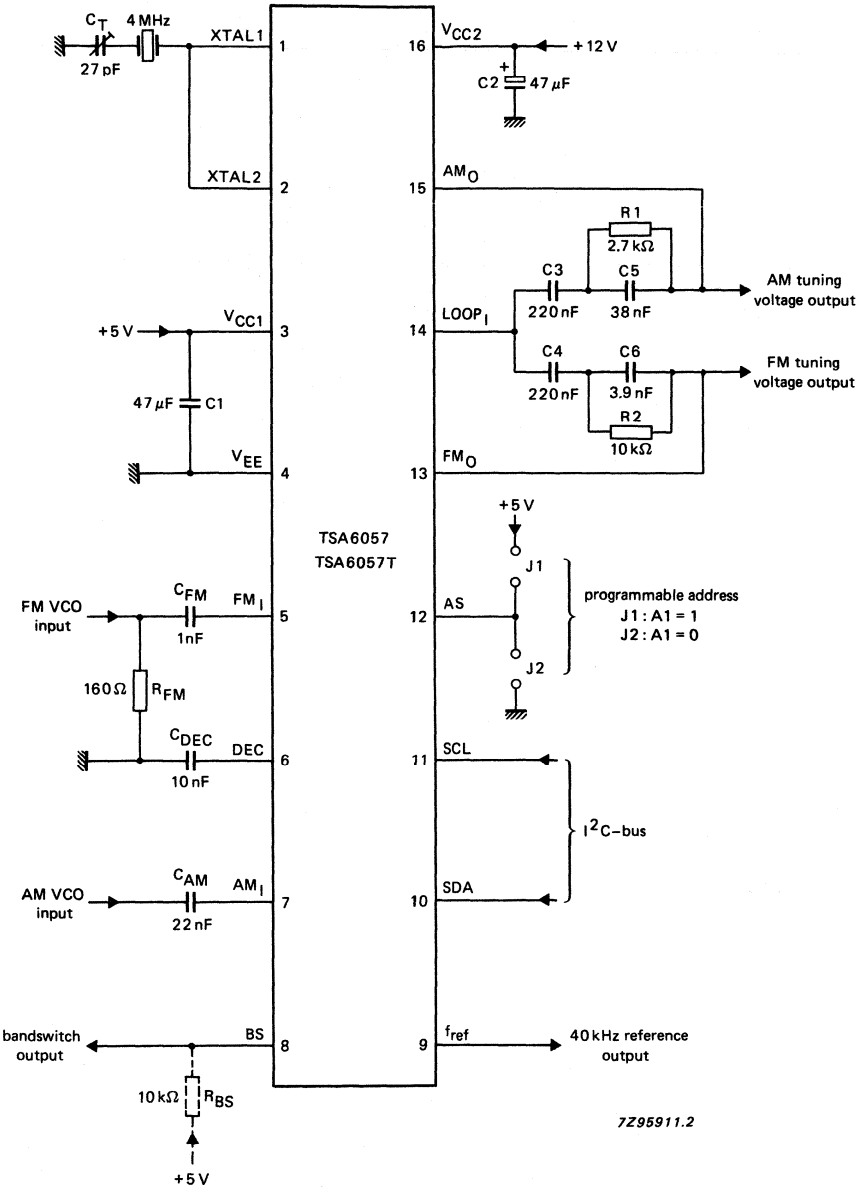


Fig.6 Application diagram

DATA PROCESSOR FOR CELLULAR RADIO (DPROC)

GENERAL DESCRIPTION

The UMA1000T is a low power CMOS LSI device incorporating the data transceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

Features

- Single chip solution to all the data handling and supervisory functions
- Configurable to both AMPS and TACS
- I^2C serial bus control
- All analogue interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Low current consumption
- Small physical size
- Minimum external peripheral components required

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 28)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 28) normal operation	I_{DD}	–	2	–	mA
Operating ambient temperature range	T_{amb}	−40	–	+ 70	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

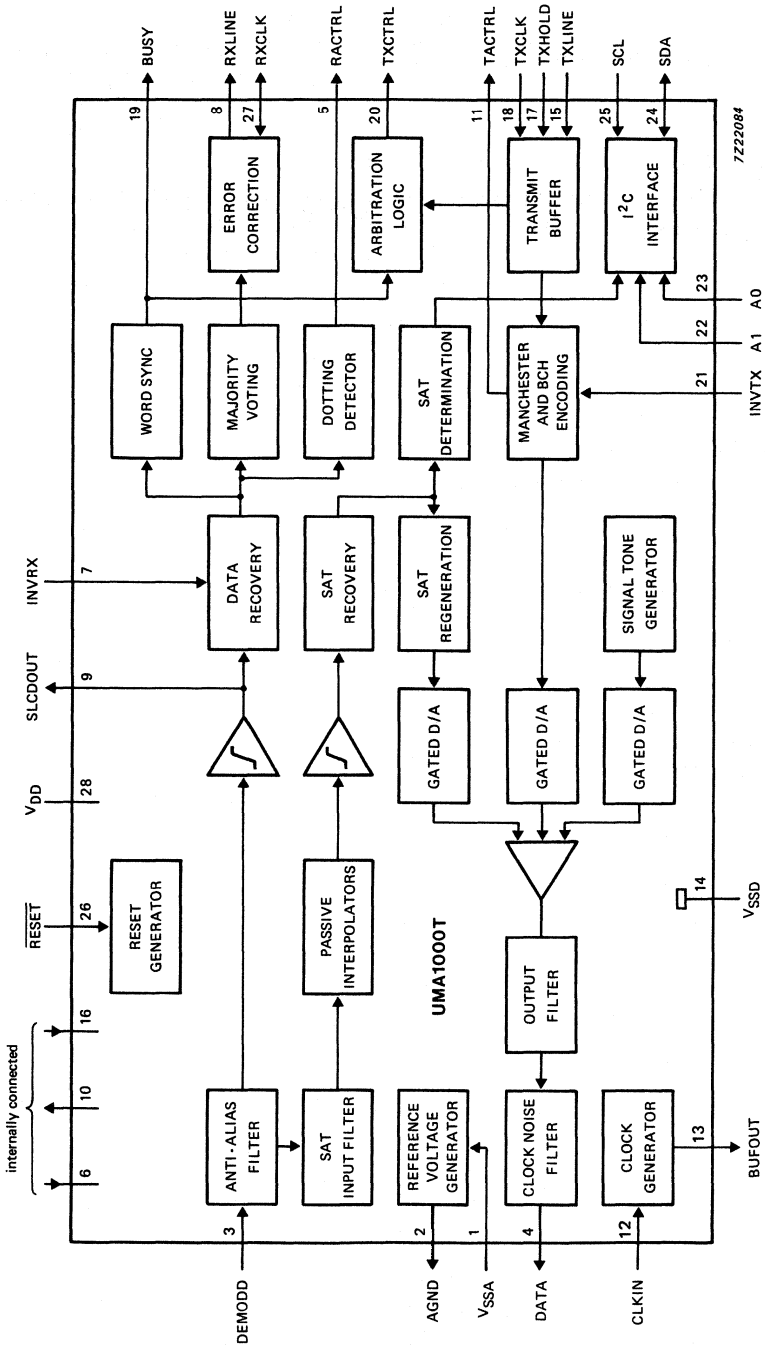


Fig. 1 Block diagram.

DEVELOPMENT DATA

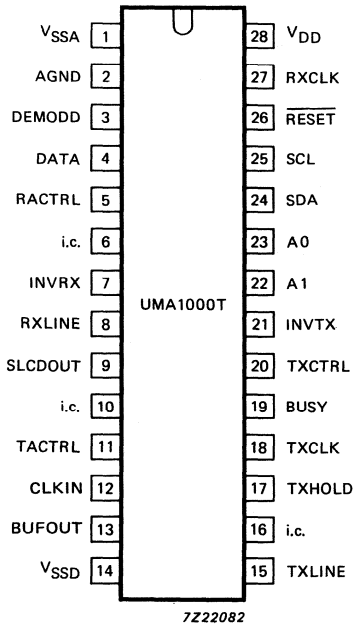


Fig. 2 Pinning diagram.

PINNING

1	V_{SSA}	analogue negative supply (0 V)	
2	AGND	2,5 V analogue reference ground	
3	DEMODD	received data signal input	
4	DATA	transmitted data signal output	
5	RACTRL	received audio control output	
6	i.c.	internally connected; must be connected to V_{SSD}	
7	INVRX	inverts sense of received data stream	
8	RXLINE	received data signal output	
9	SLCDOUT	sliced data	
10	i.c.	internally connected; must be left open -circuit	
11	TACTRL	transmitter audio control output	
12	CLKIN	1,2 MHz external master clock input	
13	BUFOUT	buffered output of internal clock oscillator	
14	V_{SSD}	digital ground	
15	TXLINE	transmitted data signal	
16	i.c.	internally connected, must be connected to V_{SSD}	
17	TXHOLD	holds off transmission of data	
18	TXCLK	transmitted data clock input	
19	BUSY	reverse control channel status putput	
20	TXCTRL	transmitter control output	
21	INVTX	inverts sense of transmitted data stream	
22	A1	address input 1	I^2C bus
23	A0	address input 0	I^2C bus
24	SDA	serial data input/output	I^2C bus
25	SCL	serial clock input	I^2C bus
26	$\overline{\text{RESET}}$	master reset input	
27	RXCLK	received data clock input	
28	V_{DD}	positive supply voltage (+ 5 V)	

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −40 to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage			V_{DD}	4,5	5,0	5,5 V
Supply current	normal operation	I_{DD}	–	2,0	–	mA
Digital inputs	note 1					
Input voltage LOW		V_{IL}	0	–	0,3 V_{DD}	V
Input voltage HIGH		V_{IH}	0,7 V_{DD}	–	V_{DD} + 0,3	V
Input capacitance		C_I	–	–	6	pF
Digital outputs	note 1					
Output voltage LOW	I_{sink} = 1 mA	V_{OL}	–	–	0,8	V
Output voltage HIGH	I_{source} = 1 mA	V_{OH}	V_{DD}−0,8	–	–	V
Open-drain outputs	note 2					
Output voltage LOW	I_{sink} = 2 mA	V_{OL}	–	–	0,8	V

Notes to the characteristics

1. All digital inputs and outputs of DPROC are compatible with standard CMOS devices and the following general characteristics apply.
2. Open-drain outputs have no internal pull-up resistors.

FUNCTIONAL DESCRIPTION

General

The UMA1000T (DPROC) is a single chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.
These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticable by the user. A data rate of 10 kbit/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig. 3.

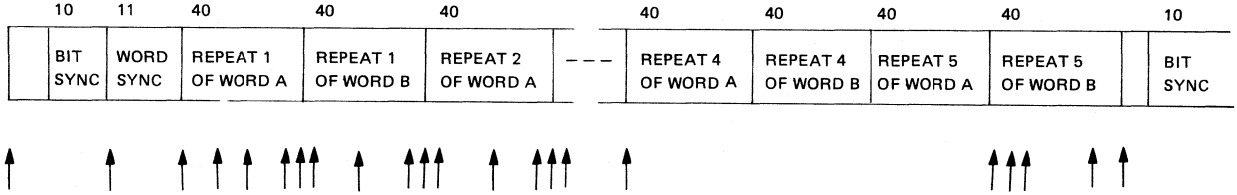
A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analagous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

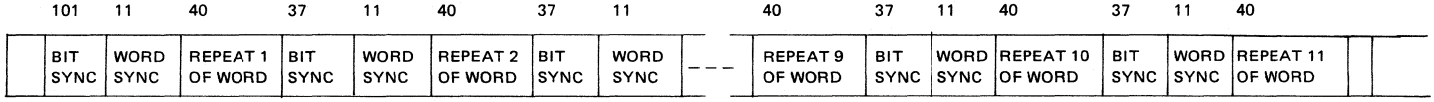
The key requirements of a hand held portable cellular set are:

- small physical size
- minimum number of interconnections (serial bus)
- low power consumption
- low cost

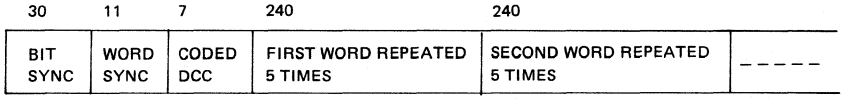
The DPROC is a member of our Cellular Radio chipset, based on the I^2C bus, which meets these requirements. A cellular radio system schematic using the chip set is shown in Fig. 4.



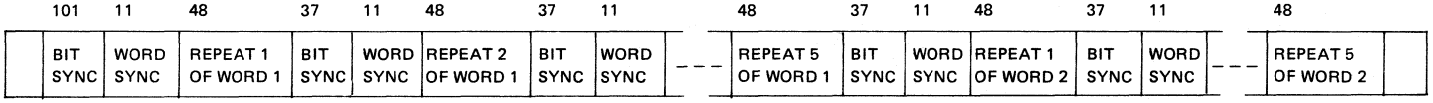
(a) forward control channel



(b) forward voice channel



(c) reverse control channel



(d) reverse voice channel

Fig. 3 Signalling formats.

DEVELOPMENT DATA

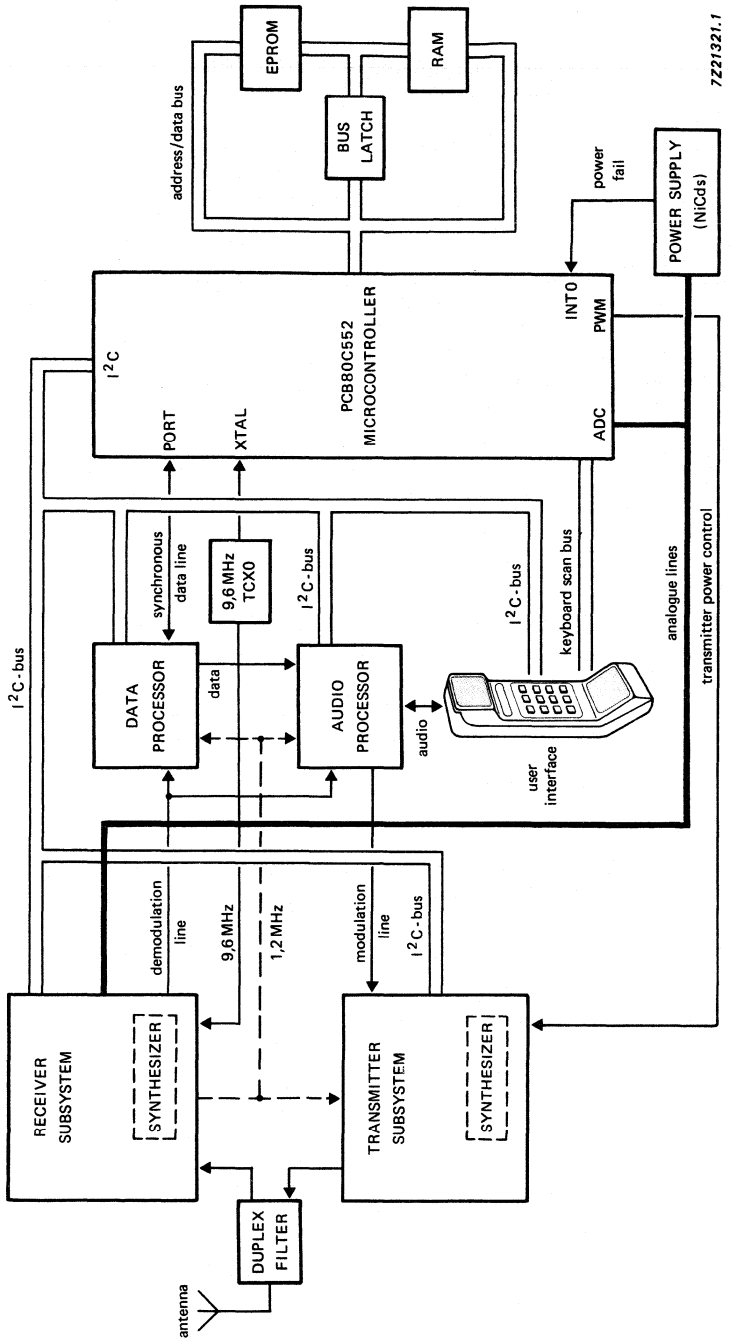


Fig. 4 Cellular radio system schematic.

EXTERNAL PIN DESCRIPTION

Supply (V_{DD}; V_{SSA}; V_{SSD}; AGND)

V_{DD} : Positive supply voltage for digital and analogue circuitry (± 5 V +10%)
V_{SSA} : Negative supply voltage for analogue circuitry (0 V)
V_{SSD} : Digital ground (0 V)
AGND: Internally generated reference ground used by internal analogue circuitry. Voltage level $(V_{DD} - V_{SSA})/2 \pm 2\%$.

Both V_{SSA} and V_{SSD} must be connected to common ground.

System clock (CLKIN; BUFOUT)

CLKIN is a digital input for the externally generated 1,2 MHz master clock. This signal should be accurate to 100 ppm and have a worst case of 60 : 40 mark-space ratio. BUFOUT is the buffered output of the clock oscillator and provides the option of generating the clock signal on chip by connecting a 1,2 MHz crystal between BUFOUT and CLKIN.

I^2C serial data link (SDA; SCL)

SDA is the bi-directional data line; SCL the clock input from an I^2C master. These constitute a typical I^2C link and conform to standard characteristics as defined in the I^2C bus specification.

- data rate: up to 100 kbit/s

Slave Address Select (A0; A1)

Selection of the device slave address is achieved by connecting A0 and A1 to either V_{SSD} or V_{DD}.

The slave address is defined in accordance with the I^2C specifications as shown in Fig. 5.

1	1	0	1	1	A1	A0	R/$\overline{W}$

Fig. 5 Device slave address.

Master reset ($\overline{RESET}$)

$\overline{RESET}$ is an asynchronous active LOW master reset input, with a minimum active pulse width of 2 μs used to reset certain logic within DPROC to a predefined state as illustrated in Tables 1 and 2. The device should be reset using this pin after power up.

Power-up state

DPROC will not respond reliably to any inputs (including $\overline{\text{RESET}}$) until 100 μs after the power supply has settled within the specified tolerance. The analogue sections of the device will have stabilized within 5 ms. No power-on-reset is provided, therefore before the device can enter normal operation $\overline{\text{RESET}}$ must be pulsed LOW. Following a device master reset the digital output pins and I^2C registers will have predefined states as illustrated in Tables 1 and 2.

Table 1 Predefined state of the digital output pins

output	state
RXLINE	HIGH
TXCTRL	HIGH
TACTRL	HIGH
RACTRL	HIGH
BUSY	HIGH

Table 2 Predefined state of the I^2C registers

register	bit							
	7	6	5	4	3	2	1	0
status	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	HIGH
control	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
SATD	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
TST	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

DEVELOPMENT DATA

Data Transfer Link (RXLINE; TXLINE; TXHOLD; TXCLK and RXCLK)

RXLINE, TXLINE, TXCLK and RXCLK provide a dedicated serial data link for the transfer of system data messages between DPROC and the system controller at variable rates of up to 200 kbits/s. TXHOLD allows the system controller to preload the DPROC transmit register with one word without the data being transmitted. DPROC then starts transmitting the instant TXHOLD is driven LOW.

- RXCLK : clock input from system controller
- RXLINE : data output from DPROC to system controller
- TXCLK : clock input from system controller
- TXLINE : open drain data bi-directional line to the system controller
- TXHOLD : (HIGH) holds off transmission of data
- data rate : up to 200 kbit/s

Note

A minimum mean data transfer rate for the received data of 2,1 kbits/s (AMPS) and 1,7 kbits/s (TACS) is required to ensure against loss of message words.

The format for received and transmitted data words is shown in Fig. 13 (a) and Fig. 13 (b) respectively. The receive and transmit data timing is illustrated in Fig. 14 (a) and Fig. 14 (b) respectively.

EXTERNAL PIN DESCRIPTION (continued)

Transmitter Control (TXCTRL)

TXCTRL is an open-drain output used to disable the transmitter during a Reverse Control Channel access failure.

- output level HIGH : RF enable
- output level LOW : RF disable

Transmitter Audio Enable (TACTRL)

TACTRL is an open-drain digital output signal used to blank the audio path and enable the data path to the modulator during data bursts on the Reverse Voice Channel.

- output level HIGH : audio enabled
- output level LOW : audio muted

Receiver Audio Enable (RACTRL)

RACTRL is an open-drain digital output used to blank the audio path to the earpiece when a sequence of dotting is detected.

RACTRL and TACTRL functions can be combined using one line.

- output level HIGH : audio enabled
- output level LOW : audio muted

Reverse Control Channel Status (BUSY)

BUSY is a digital output giving the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy-Idle bits and has the following logic levels:

- output level HIGH : channel busy
- output level LOW : channel idle

On a voice channel BUSY indicates channel idle.

Invert Receive Data (INVRX)

Enables an additional inverter in the receive data path. This allows RF demodulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC depends on the receiver local oscillator.

- input HIGH : data inverted
- input LOW : data normal

Invert Transmit Data (INVTX)

Enables an additional inverter in the transmit data path. This allows RF modulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator.

- input HIGH : data inverted
- input LOW : data normal

Transmitted Data Output (DATA)

Data is an analogue output which provides Manchester encoded and filtered data signal SAT and signalling tone. This signal should normally be AC coupled into the Audio/Data summer.

- DC level : analogue ground (AGND)
- signal level : 2 V (p-p) *
- signal tolerance : 2% + supply voltage variation (ΔV_{DD})
- minimum load impedance : 10 kΩ
- maximum load capacitance : 2 nF
- maximum output impedance : 50 Ω

Received Data Input (DEMODD)

Demodd inputs analogue data and SAT signals from the RF demodulator. This pin should normally be AC coupled.

- DC level : analogue ground (AGND)
- nominal data level : 250 mV (p-p)
- minimum data level: : 130 mV (p-p)
- input impedance : > 1 MΩ

Sliced Data Output (SLCDOUT)

Unbuffered output from data slicer. Normally used only for test purposes.
Should be left open-circuit for normal operation.

* Signal level with filtered data signal.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

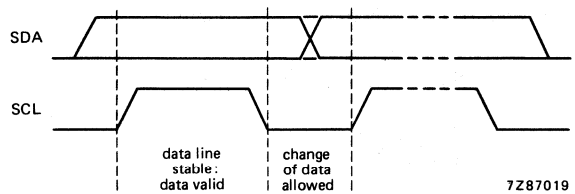


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

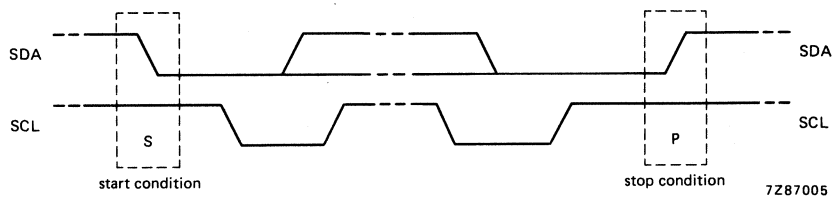


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

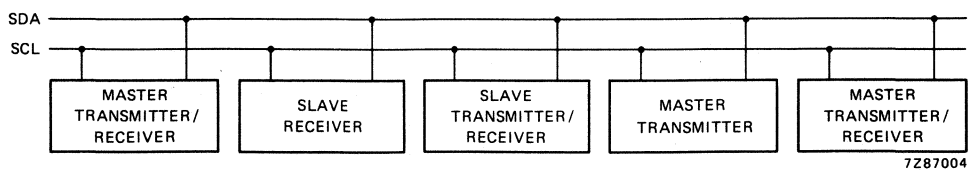


Fig. 8 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

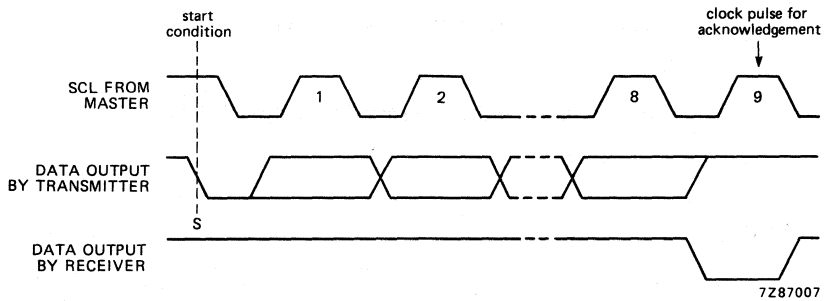


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

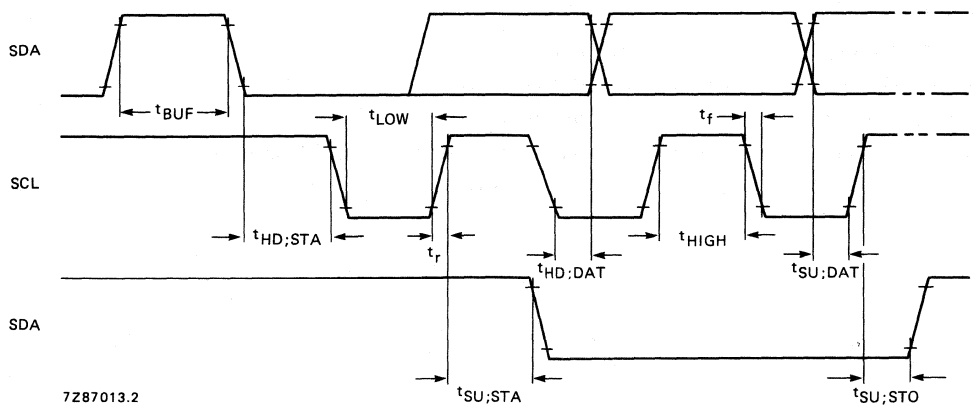


Fig. 10 Timing.

CHARACTERISTICS OF THE I²C BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS}.

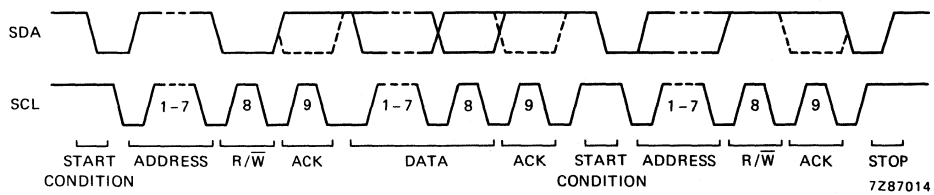


Fig. 11 Complete data transfer.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Max. number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

I²C REGISTERS

General

The I²C register block resides internally within the I²C interface block and contains various items of status and control information which are transferred to and from DPROC via the I²C bus. The block is organized into four 8-bit registers:

- Status Register — contains read only items
- Control Register
- SAT Programmable Phase Shift Register — contain write only items

Note

In normal operation the SAT delay register requires programming only after a device reset.

Table 3 Register map

register	bit							
	7	6	5	4	3	2	1	0
status	–	–	WSYNC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
control	–	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
SATD	<---------- SAT delay data ---------->							

S	DPROC ADR	R	A	STATUS	A	P

(a) read from DPROC status register

S	DPROC ADR	W	A	CONTROL	A	P

(b) write to DPROC control register

S	DPROC ADR	W	A	CONTROL	A	SAT DELAY	A	P

(c) write to all DPROC registers

Where:

S : START condition
W : read/write bit (logic 0 = write)
R : read/write bit (logic 1 = read)
A : acknowledge bit
P : STOP condition
DPROC ADR : slave address of DPROC

Fig. 12 I²C data format.

I^2C REGISTERS (continued)

Status Register

This is a read only register containing DPROC status information.

Measured SAT Colour Code (MSCC1; MSCC0)

MSCC1 and MSCC0 provide information about the current measured SAT colour code in accordance with Table 4.

Table 4 Measured SAT Colour Code

MSCC1	MSCC0	SAT frequency (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

Transmission In Progress (TXIP)

TXIP indicates whether DPROC is currently accessing the Reverse Control or Voice Channels.

- logic 1 : data transmission in progress
- logic 0 : transmission not in progress

Transmission Abort Status (TXABRT)

TXABRT indicates that a Reverse Control Channel Access Attempt has been aborted by DPROC without successful message transmission.

- logic 1 : transmission attempt aborted
- logic 0 : no access collision detected

Reverse Control Channel Status (BUSY)

BUSY gives the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy-Idle bits.

- logic 1 : channel busy
- logic 0 : channel idle

On a voice channel the BUSY bit defaults to the cleared state.

Note

This signal is also routed to the BUSY output pin.

Word Synchronization Indicator (WSYNC)

WSYNC indicates whether DPROC has acquired frame synchronization according to the Forward Control Channel format.

- logic 1 : frame synchronization acquired
- logic 0 : no frame synchronization

Control Register

This is a write only register containing DPROC control information.

SAT Path Enable (SATEN)

SATEN enables the SAT transponded signal to be output on external pin DATA.

- logic 1 : SAT tone enabled
- logic 0 : SAT tone inhibited

Signalling Tone (ST) Path Enable (STEN)

STEN enables the Signalling Tone to be output on external pin Data.

- logic 1 : ST enabled
- logic 0 : ST inhibited

Channel Format Select (FVC)

FVC selects the required channel format.

- logic 1 : Voice channel format
- logic 0 : Control channel format

Transmission Abort Permission (ABREN)

ABREN indicates whether DPROC has permission to abort data transmission and disable RF on the Reverse Control Channel following the detection of a channel access attempt collision.

- logic 1 : RF disable allowed
- logic 0 : RF disable inhibited

Message Transmission Abort (TXRST)

TXRST terminates a message being transmitted on the reverse channel. It is a monostable signal which when activated causes a reset of the message transmission circuitry and causes TXABRT and TXIP I^2C signals to be reset.

- logic 1 : reset active
- logic 0 : reset inactive

System Type Select (STS)

STS selects required system format.

- logic 1 : AMPS
- logic 0 : TACS

Serving System Select (SERV)

SERV selects which of the serving system data streams (A or B) is accepted.

- logic 1 : system A selected
- logic 0 : system B selected

SAT Programmable Delay Register (SATD)

SATD programs the value of phase shift which is applied to the SAT tones in the SAT Regeneration Block. This value will be determined and programmed into the System Controller during manufacture. The recovered SAT is delayed in time by approximately 0,8 μs x value in the register which corresponds to approximately 1,8 degrees x value in the register. The total phase shift is limited to 360 degrees.

DIGITAL CIRCUIT BLOCKS

General

The majority of the digital circuitry within the DPROC device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig. 1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Strobed Comparator Block, on which it performs the following functions:

- clock recovery
- Manchester decoding
- data regeneration

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable "bandwidth" to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1,2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a 1 otherwise it is latched as a 0.

SAT Processing

The Supervisory Audio Tone processing consists of the following functions:

- SAT recovery
- SAT determination
- SAT regeneration

SAT recovery

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.
The recovery is performed using a digital phase-locked-loop.

SAT determination

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I^2C status registers MSCC0 and MSCC1 as shown in Table 5.

Table 5 Status registers MSCC0, MSCC1; decoded SAT frequencies

register		SAT frequency band (Hz ± 4 Hz)	decoded SAT (Hz)
MSCC0	MSCC1		
1	1	< 5956	not valid
0	0	5956 to 5986	5970
0	1	5986 to 6014	6000
1	0	6014 to 6046	6030
1	1	> 6046	not valid

SAT regeneration

The SAT Regeneration Block generates a digital SAT stream from the recovered SAT stream for transponding back to the base station. The AMPS and TACS specifications require the SAT to be transponded with a maximum phase shift of 20 degrees between the point the modulated RF signal enters the mobile from the base station, and the point the modulated RF leaves the mobile. A variable phase compensation circuit is provided in DPROC to shift the recovered SAT through 0 to 360 degrees before being passed to the output summing network. The degree of phase shift is determined during manufacture of the set and the required additional phase shift is stored in non-volatile RAM and programmed via I^2C at each power-on cycle. The phase correction is performed by a counter delay method using signals which are phase locked to the recovered SAT.

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of 32 bits of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL for the duration of the burst.

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11 bit-Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC has achieved frame synchronization. In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode. On the Forward Voice Channel detection of the synchronization word indicates that the following 40 bits are valid data. Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

DIGITAL CIRCUIT BLOCKS (continued)

Majority Voting Block

The Majority Voting Block performs the following functions:

- identifying position and validity of frames in the received data stream
- extracting 5 repeats of each word from a valid frame
- performing a bit-wise majority decision on the five repeats of the data word

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searches for and extracted by DPROC. On the forward Voice Channel DPROC will extract the first five words that occur for which a correct synchronization word is found. These words can occur in any position in the frame. A serial majority vote is performed as the fifth word is being extracted.

Error Correction Block

The Error Correction Block performs the following functions:

- extraction of a valid message from the Majority-Voted Word
- computation of the S1 and S3 syndromes
- correction of up to one error in the word
- communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$$1 + X + X^6 \text{ and } 1 + X + X^2 + X^4 + X^6$$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC only corrects up to one error although the code used has a Hamming distance of five. The occurence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROC to the System Controller over RXLINE under control of a clock signal RXCLK generated by the System Controller.

Data Format

Each Received Data word consists of 4 bytes. The word format is shown in Fig. 13 (a). The sense and function of the fields is shown in Table 6.

Table 6 Received Data word

bit	title	sense	function
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occured on the serial link
0	stop	HIGH	identifies end of the word

Link Protocol

The Received Data protocol is described by the timing diagram Fig. 14 (a) and has the following parameters:

- maximum receive window (RWIN)
  Control Channel (TACS) = 47 ms
  Control Channel (AMPS) = 37 ms
- minimum clock period ($t_{CLK(min)}$ = 2 μs

Transmit Data Serial Interface

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

Data Format

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig. 13 (b). The sense and function of the fields is shown in Table 7.

Table 7 Transmit Data word

bit	title	sense	function
39	start	LOW	identifies start of word
38, 37	DCC	binary data	digital colour code
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word

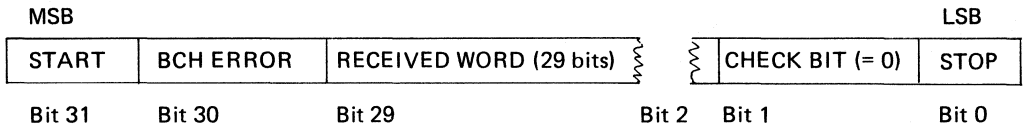
DIGITAL CIRCUIT BLOCKS (continued)

Transmit Data Serial Interface (continued)

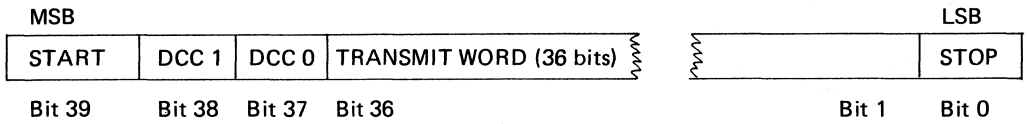
Link Protocol

Messages can be up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC to control the transfer of data words. The System Controller can abort the transmission of a message at any point by activating the I^2C signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 3). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig. 14 (b) and has the following parameters:

- maximum transmit window (TWIN)
  - Voice channel (TACS) = 60 ms
  - Voice channel (AMPS) = 48 ms
  - Control channel (TACS) = 29 ms
  - Control channel (AMPS) = 23 ms
- minimum clock period ($t_{CLK(min)}$) = = 2 μs
- minimum clock hold-off time (t_{WAIT}) = 10 μs

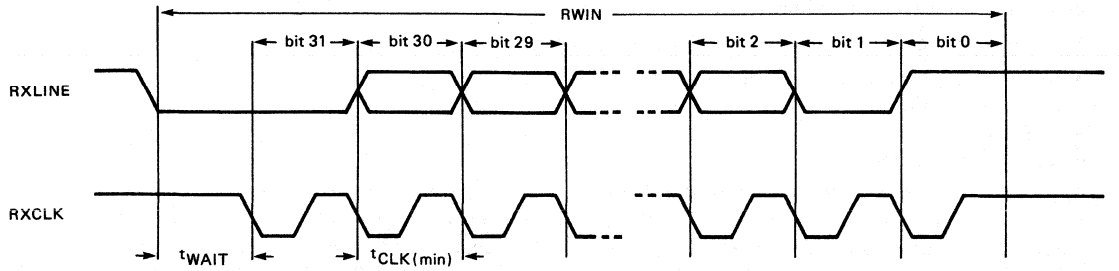


(a) received data word

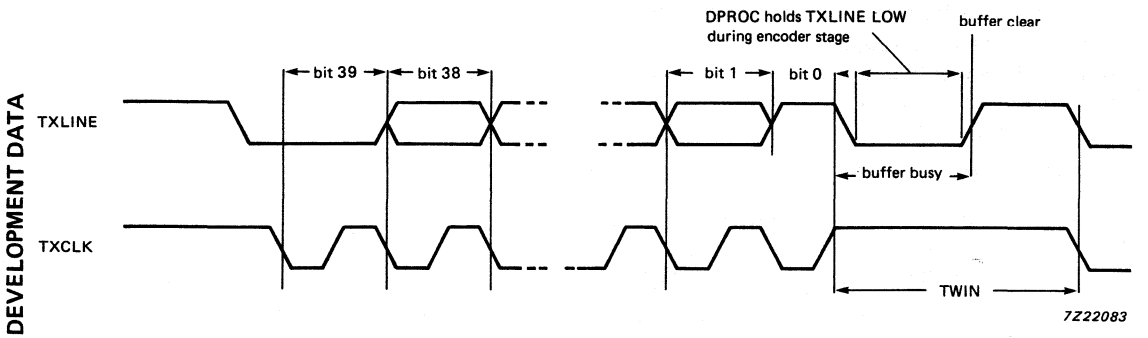


(b) transmit data word

Fig. 13 Data word formats.



(a) DPROC to microcontroller link; receive data timing



(b) Microcontroller to DPROC link; transmit data timing

Fig. 14 Data timing diagrams.

DEVELOPMENT DATA

DIGITAL CIRCUIT BLOCKS (continued)

BCH and Manchester Encoding Block

The functions performed by this circuit block include:

- reception of data from the System Controller
- parity generation
- message construction
- Manchester encoding

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48 bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.
The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code
- 48-bit code word

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 8.

Table 8 Digital Colour Code; 7-bit word

DCC1	DCC0	Coded DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0
		DCC1		DCC0			DCC1.EXOR.DCC0	

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

Reverse Control Channel Access Arbitration

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ORed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I^2C register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

DEVELOPMENT DATA

Initial State

- transmitter power off via I^2C
- DPROC transmit circuitry in power-up state
- TXCTRL line HIGH

Access Attempt Procedure

1. System Controller decides to send message (note 1).
2. System Controller drives TXCTRL low directly.
3. System Controller switches transmitter power on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets ABREN via I^2C (if required) allowing DPROC to control the transmitter.
5. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
6. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
7. System Controller transfers message to DPROC via serial link (note 1).
8. DPROC sets I^2C signal TXIP and starts sending message while monitoring Busy/Idle status.
9. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
10. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
11. On completion of entire message DPROC clears TXIP and 25 ms later the System Controller disables transmitter via I^2C.
12. System Controller finally sends TXRST to prepare DPROC for next transmission.

Note to the Access Attempt Procedure

At stage 1 the system controller may choose to preload DPROC with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC.

DIGITAL CIRCUIT BLOCKS (continued)

Abort Procedure

1. DPROC immediately disables transmitter output by driving TXCTRL low.
2. DPROC sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC for next transmission.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

ANALOGUE CIRCUIT BLOCKS

General

The analogue signal processing functions on DPROC are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by distributed RC active filters, passive interpolators and comparators.

The distributed RC sections, the Anti-Alias Filter and the Clock Noise Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolators increase the sampling rate from 300 kHz to 1,2 MHz. The sampled analogue signals from the Passive Interpolators are converted to sampled 2-state digital signals by the Strobed Comparators. The Gated Digital-to-Analogue converters and Analogue Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC output signals, and conversion to the sampled analogue domain.

These analogue sections of the device are shown in Fig. 1.

Reference Voltage Generator

The Reference Voltage Generator generates the analogue ground reference voltage (AGND) used internally within the DPROC device. To minimize noise AGND must be externally decoupled to V_{SSA} as shown in Fig. 15.

Anti-Alias Filter

The Anti-Alias Filter is placed before the SAT sampling block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Alias Filter is a continuous time-distributed RC-active low-pass filter.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the switched-capacitor filters. This reduces the coarseness of the zero crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Strobed Comparators

The Strobed Comparators form the analogue-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers wich convert the filtered sampled analogue signals into 2-state sampled digital signals containing only the zero-crossing information from the analogue signal.

ANALOGUE CIRCUIT BLOCKS (continued)

Gated Digital-to-Analogue and Analogue Summer

The Gated Digital-to-Analogue converters and Analogue Summer form the interface between the digital and analogue circuitry on the transmit path of DPROC. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal. The data streams are enabled by the I^2C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analogue conversion and sub-sampling operation is performed by the Gated Digital-to-Analogue converters and Analogue Summer. The relative signal weights applied in the summer (with respect to the data path) are shown in Table 9.

Table 9 Relative signal weights

signal	relative output level AMPS and TACS
ST	1,0
SAT	0,25
DATA	1,0

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC coupling from the DATA pin.

Clock Noise Filter

The filter is a non-critical continuous time-distributed RC-active low-pass filter used to remove any switching transient residues from the output signal.

APPLICATION INFORMATION

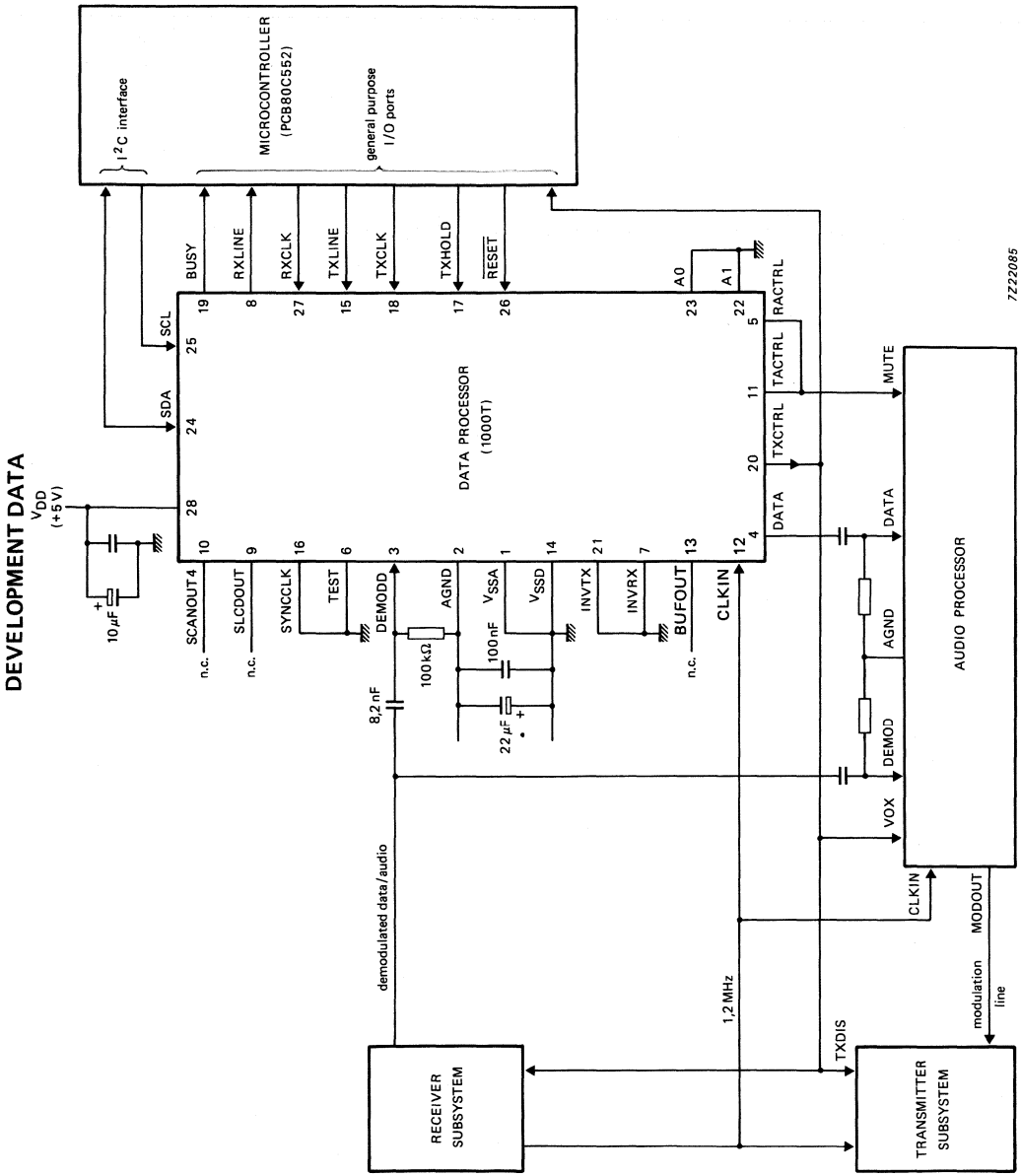


Fig. 15 DPROC application circuit.

LOW-POWER UNIVERSAL SYNTHESIZER FOR RADIO COMMUNICATION

DESCRIPTION

The UMA1010T is a low power universal synthesizer for radio communication. The IC is manufactured in bipolar technology and is designed to achieve 10 kHz to 100 kHz channel spacing in the frequency band of 400 MHz to 1 GHz.
The channel is selected via the standard I²C-two-line serial bus.
The UMA1010T has an integrated low-power prescaler (up to 1150 MHz), a low-noise 7.5 V amplifier for the loop filter and a programmable reference divider oscillator.
Power down circuitry enables the device to be idled.

Features

- Fully programmable RF divider from 400 MHz to 1150 MHz
- I²C-bus interface for two-line serial data transfer
- On-chip crystal oscillator from 3 MHz to 16 MHz; circuit can be used with a crystal or a tuned-circuit oscillator (TCXO)
- 4-bit crystal frequency divider that generates a reference frequency between 5 kHz and 50 kHz with a large number of crystal frequencies
- Digital comparator that provides a wide pull-in range
- High gain sample-and-hold phase comparator to achieve a low noise and a high reference rejection
- On-chip out-of-lock indication
- Two extra VCO control outputs
- Latched synthesizer alarm signal output
- Status register including out-of-lock and power failure indication
- On-chip power-on-reset presetting the registers
- Low-noise high-voltage operational amplifier allowing a large tuning range at the VCO
- Programmable phase comparator gain
- Asymmetric RF input
- Power down possibilities via the I²C-bus or the HPD pin
- Crystal frequency divide-by-eight output

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage ranges					
digital + 5 V	V_P	4.5	5.0	5.5	V
analogue + 7.5 V	V_{P1}	4.5	7.5	8.0	V
analogue + 5 V	V_{P2}	4.5	5.0	5.5	V
Operating currents					
V_P (digital) = 5 V	I_P	–	12	–	mA
V_{P1} (analogue) = 7.5 V	I_{P1}	–	1	–	mA
V_{P2} (analogue) = 5 V	I_{P2}	–	1	–	mA
Total current in power down mode	$I_P + I_{P1} + I_{P2}$	–	3.5	–	mA
RF input frequency range	f_{RFI}	400	–	1150	MHz
Crystal frequency range	f_{XTAL}	3	–	16	MHz

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

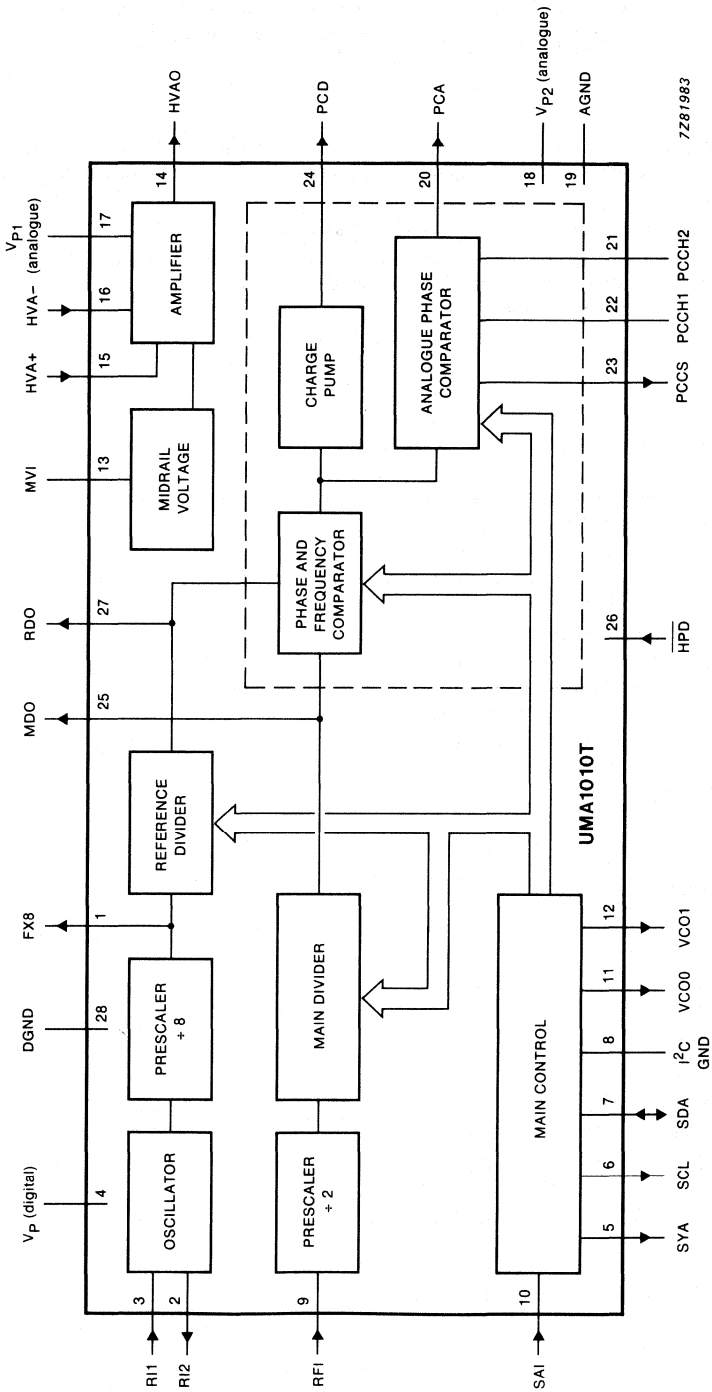


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

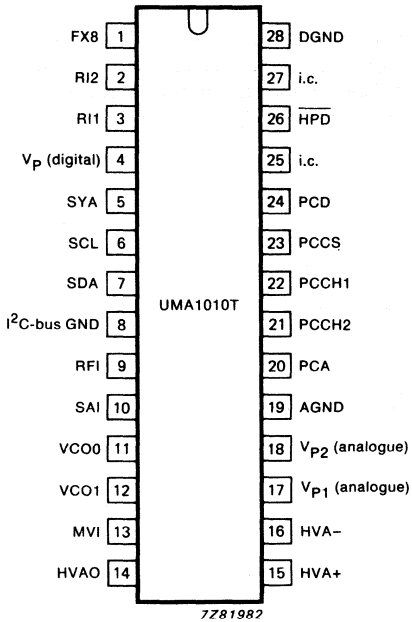


Fig. 2 Pinning diagram.

1	FX8	Output reference prescaler
2	RI2	Reference input 2
3	RI1	Reference input 1
4	V_P	Digital + 5 V supply
5	SYA	Synthesizer alarm
6	SCL	Serial clock line ⎫ I²C-bus
7	SDA	Serial data line; input/output ⎭ I²C-bus
8	I²C-bus GND	Ground for I²C-bus
9	RFI	RF input
10	SA1	Slave address select input
11	VCO0	Oscillator buffer switch output 0
12	VCO1	Oscillator buffer switch output 1
13	MV1	Mid-rail voltage (not buffered)
14	HVAO	Output high-voltage amplifier
15	HVA+	Non-inverting input high-voltage amplifier
16	HVA−	Inverting input high voltage amplifier
17	V_{P1}	Analogue +7.5 V supply
18	V_{P2}	Analogue +5 V supply
19	AGND	Analogue ground
20	PCA	Analogue phase comparator output
21	PCCH2	Phase comparator external hold capacitor node 2
22	PCCH1	Phase comparator external hold capacitor node 1
23	PCCS	Phase comparator external sampling capacitor node
24	PCD	Digital phase comparator output
25	i.c.	Internally connected
26	$\overline{HPD}$	Inverting hardware power-down input
27	i.c.	Internally connected
28	DGND	Digital ground

FUNCTIONAL DESCRIPTION

Power supply

V_P (digital) is the + 5 V supply which feeds the dividers, the control and the digital part of the comparator. V_{P1} (analogue) is the + 7.5 V supply for the amplifier output stage. The + 5 V analogue supply is V_{P2} (analogue) which should be very clean to prevent spurious signal on the VCO control voltage.

Main divider

The main divider is a fully programmable divider. The division ratio range is from 2048 to 262142 in steps of two. It is sufficient for 10 kHz channel spacing with an input of 1050 MHz. Due to the fixed divide-by-two prescaler, half of the ratio is programmed via the I^2C-bus in the Registers C, D and E (see Table 1).

Table 1 1/2 ratio in binary form

MSB														LSB
0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
C ◄					D			►	◄				E			►

The new programmed ratio is only updated after programming Register E.

Oscillator

To provide the reference frequency, two modes of operation exist:

- Use an external resonator connected between RI1 and RI2
- Use an external reference source as a TCXO on RI1

Reference divider

Table 2 Division ratios as a function of the program

	A0	0	1	0	1
	A1	0	0	1	1
A3	A2				
0	0	128	160	192	240
0	1	256	320	384	480
1	0	512	640	768	960
1	1	1024	1280	1536	1920

One eighth of the crystal frequency is available on pin 1 (FX8). It can be used as a reference frequency input for other circuits.

Phase comparator

The phase comparator includes two comparators:

- Digital 3-state comparator with charge pump output (PCD) which provides a wide pull-in range
- High-gain sample-and-hold analogue phase comparator output (PCA) gives the possibility of high performance.

The analogue phase comparator gives an "out-of-lock" indication when the loop phase error is outside its linear range or if one of its inputs is missing. In the event of one of these, PCA is 3-state and PCD pushes or pulls 300 μA for the duration of the phase error.

$$\text{PCD gain} = \frac{300\,\mu\text{A}}{2 \times \pi} \text{ (A/rad)}$$

Under "in-lock" condition PCD goes to 3-state and PCA becomes active. If the bit PCD select is set PCD remains active, this is used in systems which need minimum complexity. The sampling capacitor (CC) is connected between PCCS and GND. CC fixes the gain of the phase comparator.

$$\text{PCA gain} = \frac{300}{2 \times \pi \times CC \times f_{ref}} \text{ (V/rad)}$$

where CC is the sampling capacitor (nF)
and f_{ref} is the reference frequency (kHz).

The hold capacitor is connected between PCCH1 and PCCH2. The sample-and-hold is designed to suppress the reference frequency at the output of the phase comparator.

DEVELOPMENT DATA

Main control

Two formats for the I²C-bus protocol have been implemented on the UMA1010T:

- Burst mode, this includes subaddressing and selectable auto-increment for writing information to the synthesizer
- Single byte without subaddressing for reading the status register of the synthesizer

The status register contains information related to the synthesizer alarm (SYA) as shown in Table 3.

Table 3 Status register

MSB							LSB
0	0	0	00L	0	L00L	LPD	DI

Where: 00L = momentarily out of lock
L00L = latched out of lock
LPD = latched power dip
DI = disable interrupt

The alarm is generated by an "out-of-lock" or a power dip and is reset when the register is read. If one of these conditions occurs SYA is forced LOW.

I²C-BUS DEFINITION BIT ALLOCATION

The I²C-bus data format to write on the synthesizer has the following form:

START – address – subaddress – data 1 – data 2 – . . . – data n – STOP where:

address 1 1 0 0 0 0 SA1 R/$\overline{W}$

SA1 is logic level on pin SA1
R/$\overline{W}$ is read/not write

subaddress 0 0 0 DI AVI SB2 SB1 SB0

DI is disable interrupt, DI = 1 disables the alarm on SYA.
AVI is auto value increment, AVI = 1 allows increment of the register pointer.
SB3 – SB0 is register pointer, it indicates the register number where data 1 will be written. The pointer value is 0 for Register A up to 4 for Register E.

data n (n up to 5)

register	pointer	bit allocation								preset values		
		7	6	5	4	3	2	1	0	decimal	binary	hexa-decimal
A	000	PD	X	X	PCD	RD3	RD2	RD1	RD0	14	00001110	0E
B	001	VCO1	X	X	VCO0	X	X	X	X	16	00010000	10
C	010	X	0	X	X	1	PCG2	PCG1	MD16	173	10101101	A0
D	011	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	56	00111000	38
E	100	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	128	10000000	80

Register A is: PD (Power down), PD = 0 is normal operation.
PCD (PCD select), PCD = 1 PCD is always active.
RD3 . . . RD0 (reference division ratio), see Table 2 preset 1536

Register B is: VCO1 set VCO1 pin.
VCO0 set VCO0 pin, VCO0 is forced LOW during an "out-of-lock" indication.

Register C is: PCG2, PCG1, i.e. gain of the phase comparator;
preset + 2 dB
00 –6 dB
01 –2 dB
10 + 2 dB
11 + 6 dB
MD16, MSB of the main division ratio.

Register D is: MD15 to MD8, division ratio bit 15 to 8.

Register E is: MD7 to MD0, division ratio bit 7 to 0. Preset 160000.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges				
digital + 5 V	V_P	4.5	5.5	V
analogue + 8 V	V_{P1}	4.5	8.0	V
analogue + 5 V	V_{P2}	4.5	5.5	V
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−40	+ 125	°C
Total power dissipation				
V_P = 5 V	P_{tot}	–	70	mW
power down	P_{tot}	–	16	mW

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
SUPPLY						
Supply voltage ranges						
digital + 5 V		V_P	4.5	5	5.5	V
analogue + 7.5 V		V_{P1}	4.5	7.5	8.0	V
analogue + 5 V		V_{P2}	4.5	5	5.5	V
Supply current ranges						
digital + 5 V		I_P	–	10	–	mA
analogue + 7.5 V		I_{P1}	–	0.7	1	mA
analogue + 5 V		I_{P2}	–	3	–	mA
MAIN DIVIDER						
Division ratio	step = 2		2048	–	262142	
RF input (RFI)						
Frequency range		f_{RFI}	400	–	1150	MHz
Input voltage level (RMS value)		$V_{i(rms)}$	50	–	150	mV
Input impedance		R_{RFI}	–	*	–	Ω

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
MAIN CONTROL						
Serial clock input (SCL)						
Serial data input (SDA)						
Clock frequency		f_{CLK}	0	–	100	kHz
Input voltage HIGH		V_{IH}	3	–	--	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input current HIGH		I_{IH}	–	3	10	μA
Input current LOW		I_{IL}	–10	–5	–	μA
Input capacitance		C_I	–	*	–	pF
SDA sink current	V_{OL} = 0.4 V	I_{OL}	–	–	3	mA
Slave address select input (SA1)	note 1					
Input voltage HIGH		V_{IH}	3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.4	V
Sink current HIGH		I_{IH}	–	–	0.1	μA
Source current LOW		$-I_{IL}$	–	–	2	μA
Oscillator buffer switch output 0 (VCO0)	note 2					
Output voltage LOW		V_{OL}	–	–	0.2	V
Sink current LOW		I_{OL}	–400	–	–	μA
Oscillator buffer switch output 1 (VCO1)						
Output voltage LOW		V_{OL}	–	–	0.2	V
Sink current LOW		I_{OL}	–400	–	–	μA
Inverting hardware power down input ($\overline{\text{HPD}}$)	note 1					
Input voltage HIGH		V_{IH}	3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.4	V
Input current HIGH		I_{IH}	–	0.1	–	mA
Input current LOW		I_{IL}	–5	–2	–	μA
Synthesizer alarm (SYA)						
Input voltage LOW		V_{IL}	–	–	0.4	V
Input current LOW		I_{IL}	–400	–	–	μA

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
OSCILLATOR						
Reference input 1 (RI1)						
Frequency range		f_{ref1}	3	–	16	MHz
Input level (RMS value)	sinewave	$V_{ref1(rms)}$	0.1	–	2	V
Input level (peak-to-peak value)	square wave	$V_{ref1(p-p)}$	0.3	–	5	V
Reference input 2 (RI2)	note 3					
Frequency range		f_{ref2}	3	–	16	MHz
Output impedance		Z_o	–	–	2	kΩ
REFERENCE DIVIDER						
Division ratio			128	–	1920	
Input frequency range		f_i	3	–	16	MHz
Output frequency range		f_o	5	–	50	kHz
Output reference prescaler (FX8)	note 4					
Voltage output LOW		V_{OL}	–	–	0.4	V
Sink current LOW		V_{OL}	–	–	1.5	mA
Reference divider test output (RDO)	note 5					
Voltage output LOW		V_{OL}	–	–	0.4	V
Sink current LOW		V_{OL}	–	–	500	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
PHASE COMPARATOR						
Frequency range		f	5	–	50	kHz
Digital phase comparator output (PCD)	note 6					
Output source current		$-I_O$	–	–300	–	μA
Output sink current		I_O	–	300	–	μA
Output leakage current		I_{LO}	–	–	10	nA
Phase comparator external sampling capacitor node (PCCS)	note 7					
Capacitance to ground		C_{PCCS}	20	–	–	pF
Phase comparator external hold capacitor nodes 1 and 2 (PCCH1; PCCH2)						
Hold capacitor		C_{HOLD}	–	1	–	nF
Analogue phase comparator output (PCA)	note 8					
Output source current		$-I_O$	–500	–	–	μA
Output sink current		I_O	–	–	700	μA
Output leakage current	V_{PCA} = 2.5 V	I_{LO}	–	–	250	nA
Gain	RF = 5 kHz; note 9	G_v	–	–	500	V/rad
	RF = 25 kHz; note 9	G_v	–	–	200	V/rad
LOOP AMPLIFIER						
Mid-rail voltage; not buffered (MV1)						
AC decoupling		C_{MV1}	–	47	–	μF

parameter	conditions	symbol	min.	typ.	max.	unit
Non-inverting high voltage amplifier input (HVA+)	note 10					
AC decoupling		C_{HVA}	–	*	–	μF
Inverting high voltage amplifier input (HVA–)						
Input impedance		Z_i	–	*	–	kΩ
Input noise (0.3 to 3 kHz)		N_{af}	–	10	–	$nV/\sqrt{Hz}$
High voltage amplifier output (HVAO)						
Open loop voltage gain		G_{ol}	30	60	–	dB
Output voltage		V_O	2	–	$V_{P1}-0.4$	V
Unity gain bandwidth		$B_{G=1}$	–	2	–	MHz
Open loop output resistance		R_O	–	70	–	kΩ
Output current		I_O	–	350	–	μA

Notes to the characteristics

1. When left open is HIGH.
2. During out-of-lock the VCO0 pin is forced LOW.
3. If a TCXO is used this pin is to remain open or be used as a reference frequency.
4. This pin is an open-collector output of the reference frequency divided by eight.
5. This pin is an open-collector output.
6. This pin is active when out-of-lock is indicated and will be 3-state when the analogue phase comparator takes over after the in-lock indication.
7. The capacitor on this pin fixes the gain of the analogue phase comparator.
8. This pin will be 3-state when out-of-lock is indicated.
9. Gain is calculated with a phase comparator gain (PVG) programmed to 6 dB.
10. This pin is connected internally, via a buffer, to MVI.

DEVELOPMENT DATA

* Value to be fixed.

APPLICATION INFORMATION

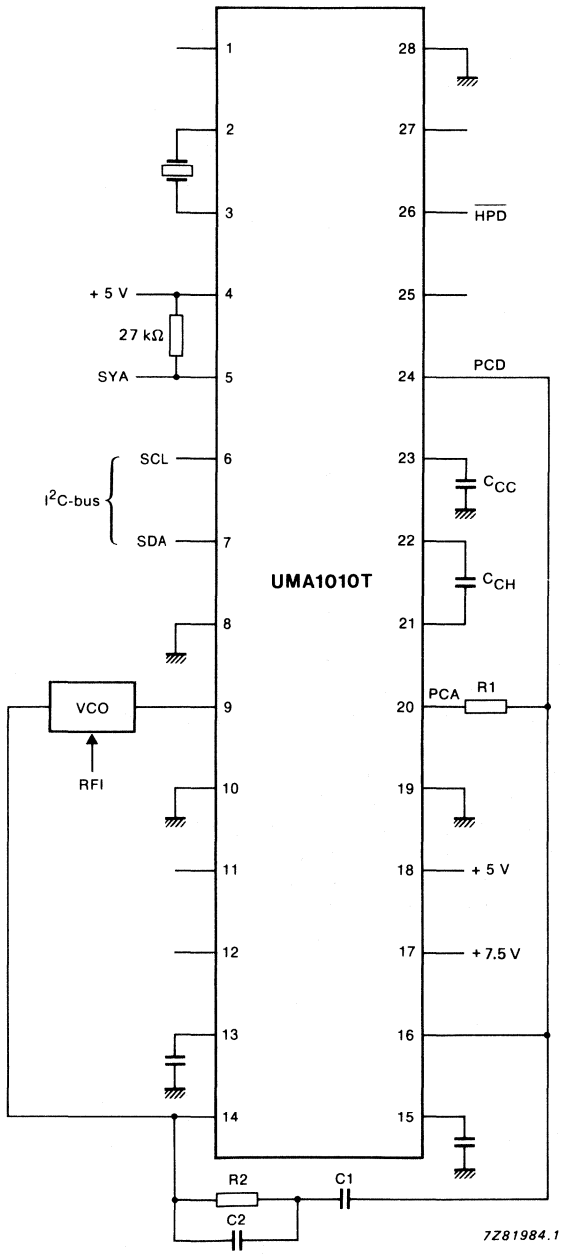


Fig. 3 Synthesizer application.

DEVELOPMENT DATA

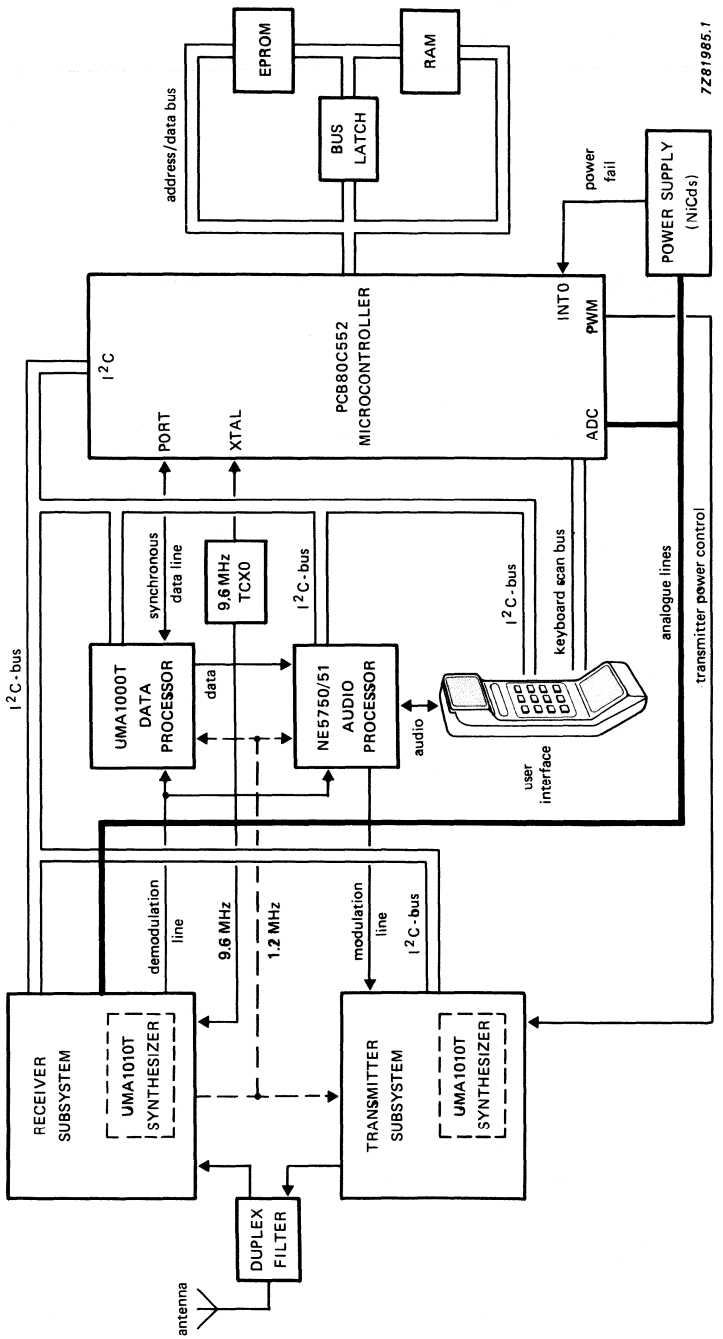


Fig. 4 Cellular radio system schematic.

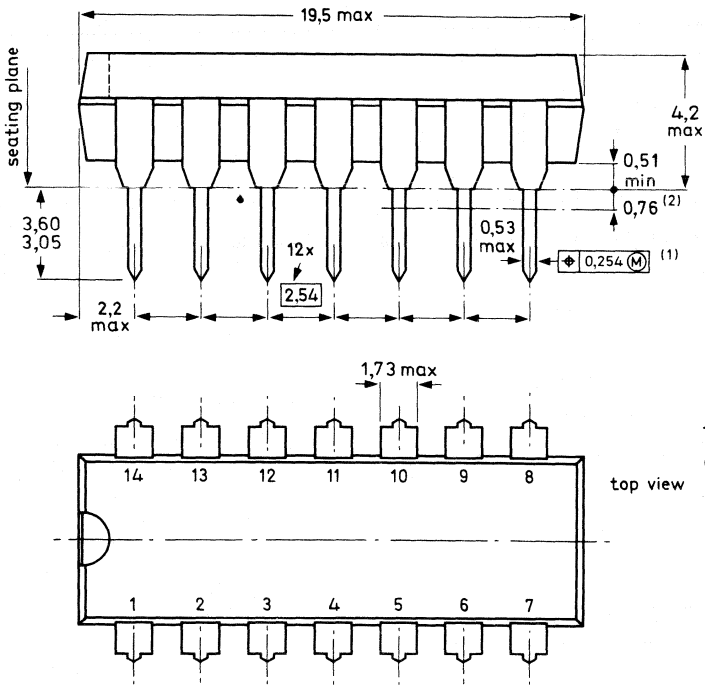
The UM1010T is a member of our Cellular Radio chipset, based on the I²C-bus, which meets the key requirements of a hand-held portable cellular set:

- small physical size
- minimum number of interconnections (serial bus)
- low power consumption
- low cost

PACKAGE INFORMATION

Package outlines
Soldering

14-LEAD DUAL IN-LINE; PLASTIC (SOT27)



Dimensions in mm

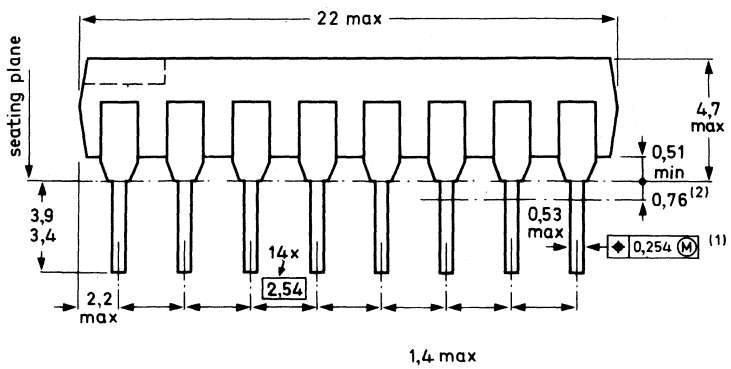
⊕ Positional accuracy.

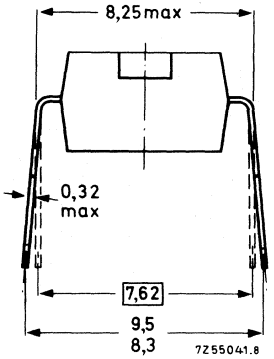
Ⓜ Maximum Material Condition.

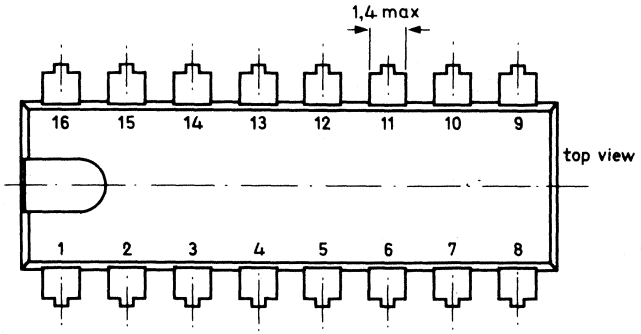
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)







Dimensions in mm

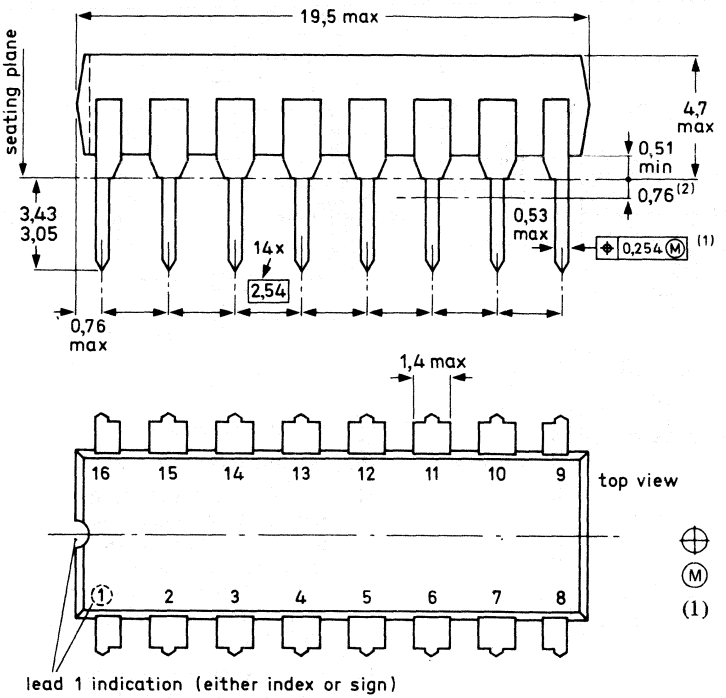
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT38Z)



⊕ Positional accuracy.

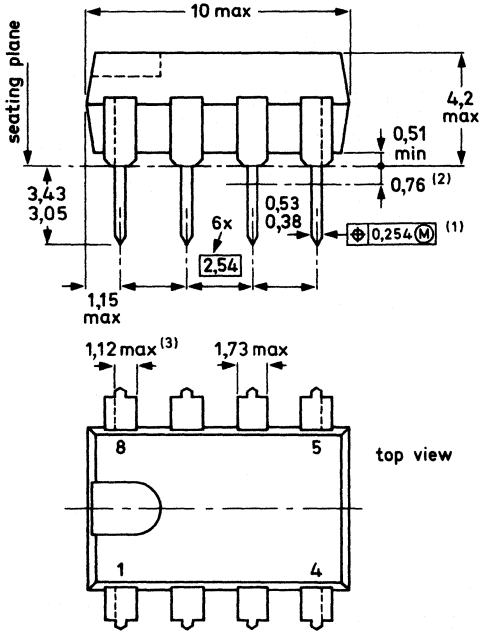
Ⓜ Maximum Material Condition.

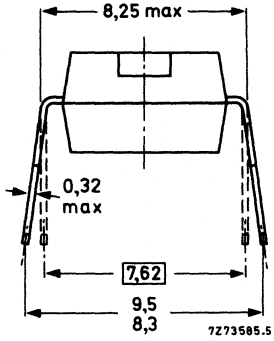
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

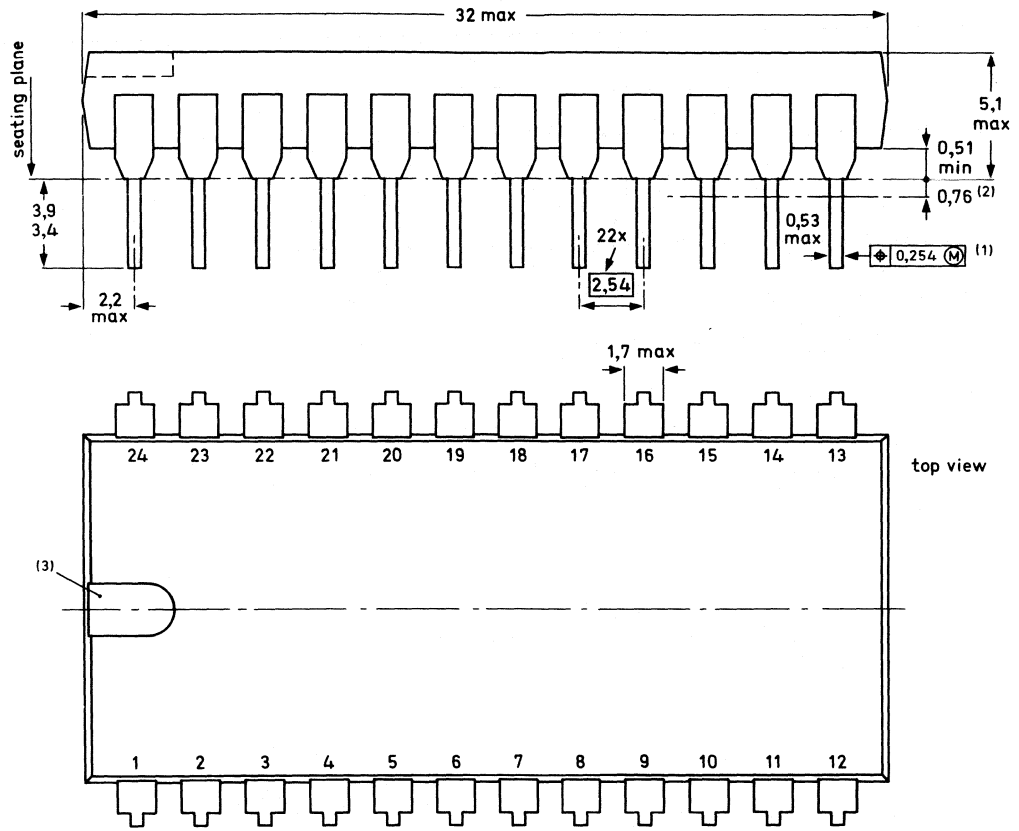
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

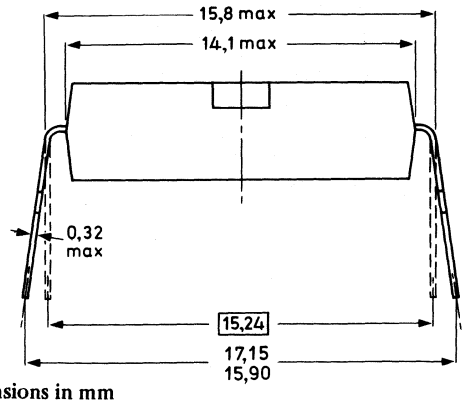
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT101A, B, F, G, L)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

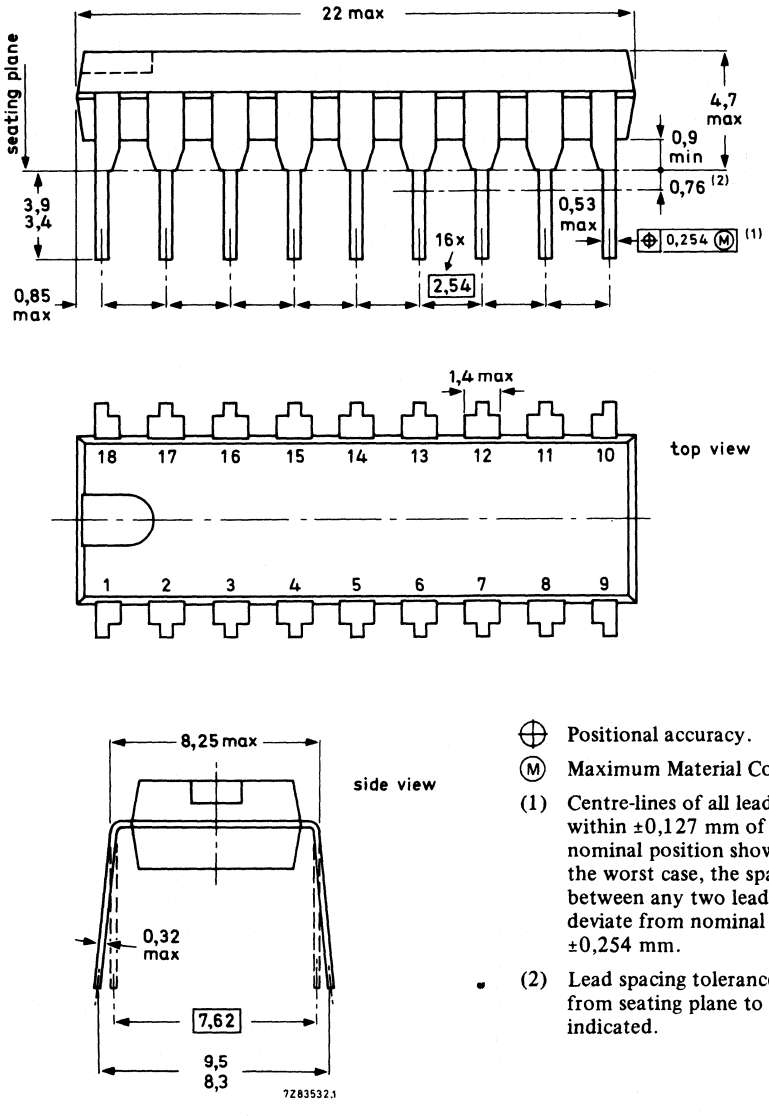
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102)



⊕ Positional accuracy.

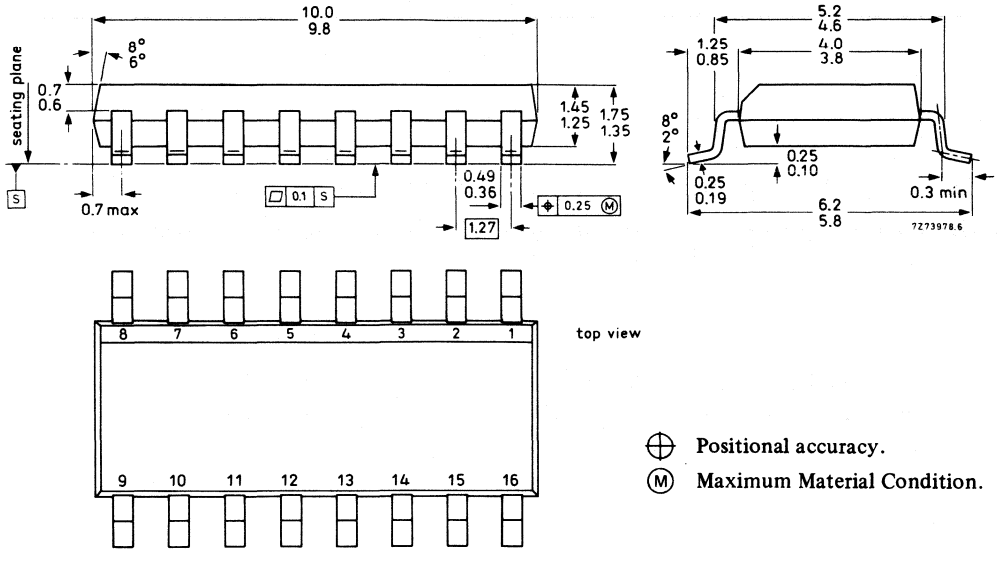
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16; SOT109A)

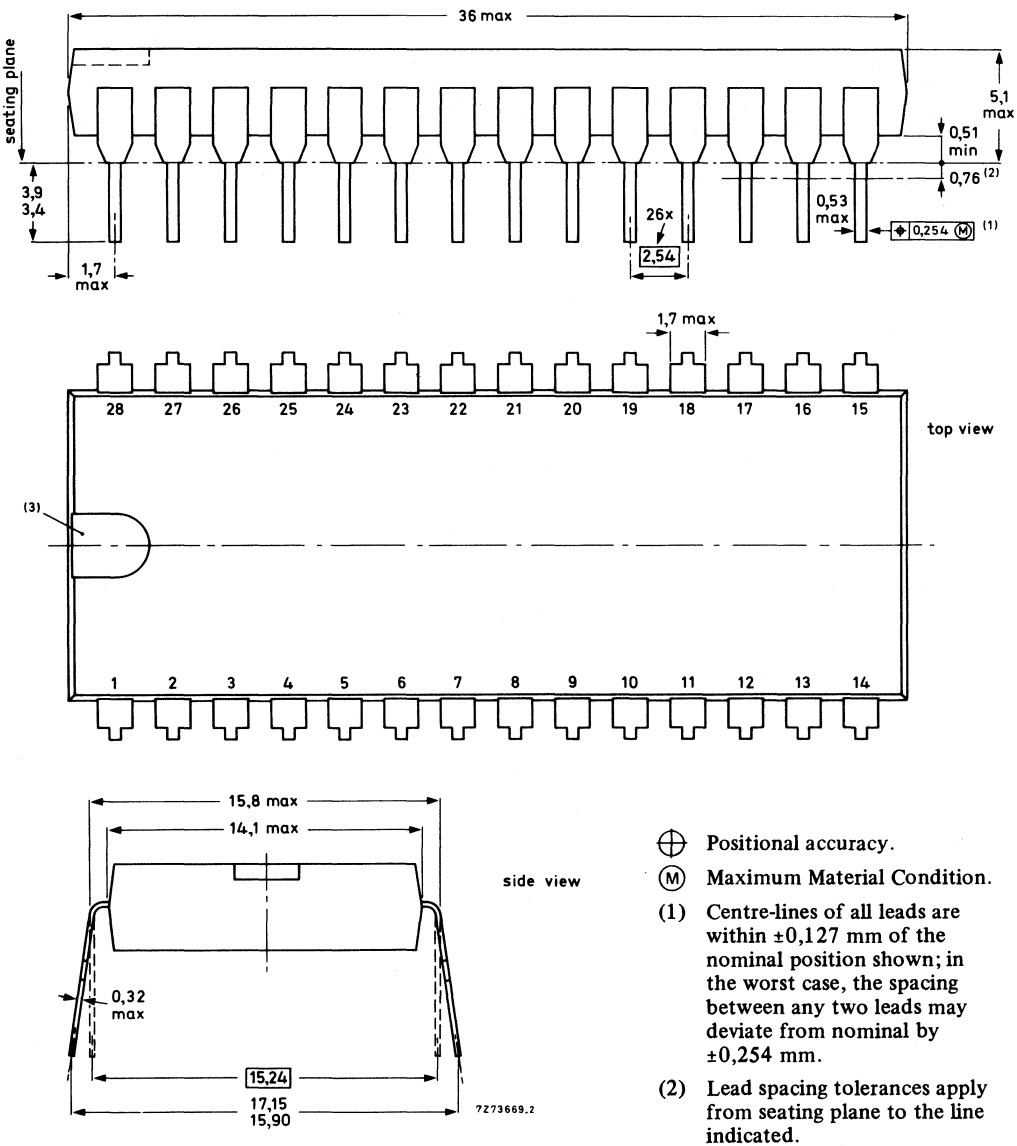


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

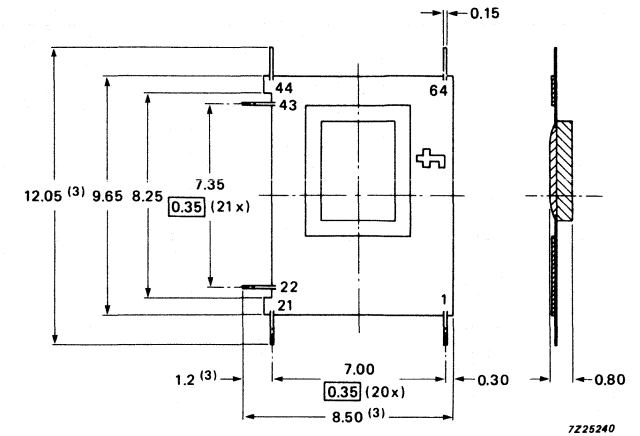
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

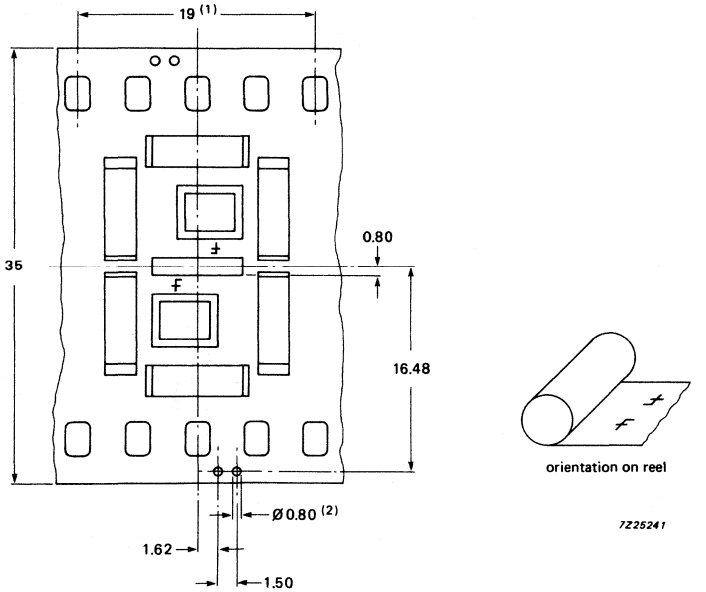
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

64-LEAD TAPE-AUTOMATED-BONDING (TAB) MODULE (SO119; SO121; SO122)

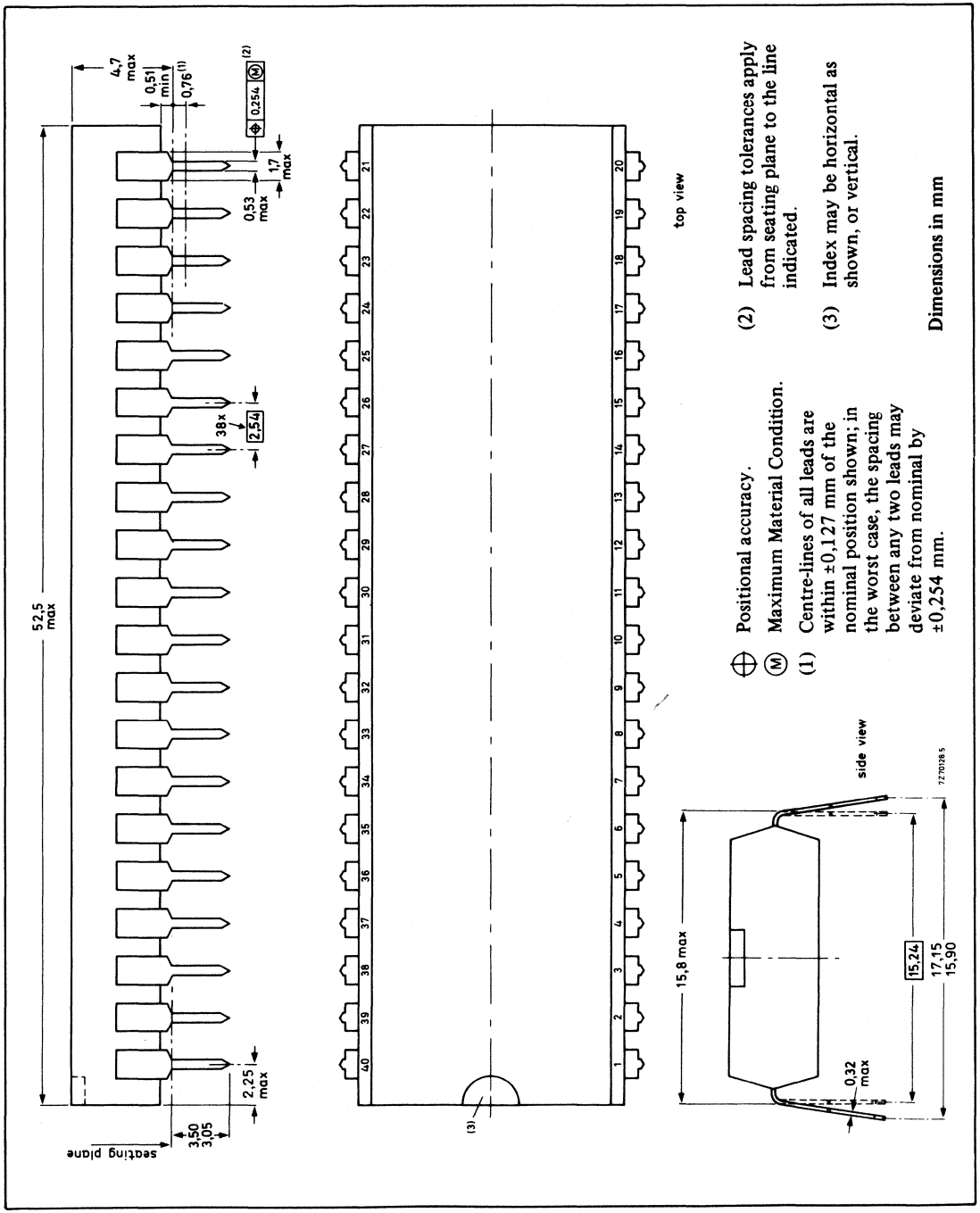




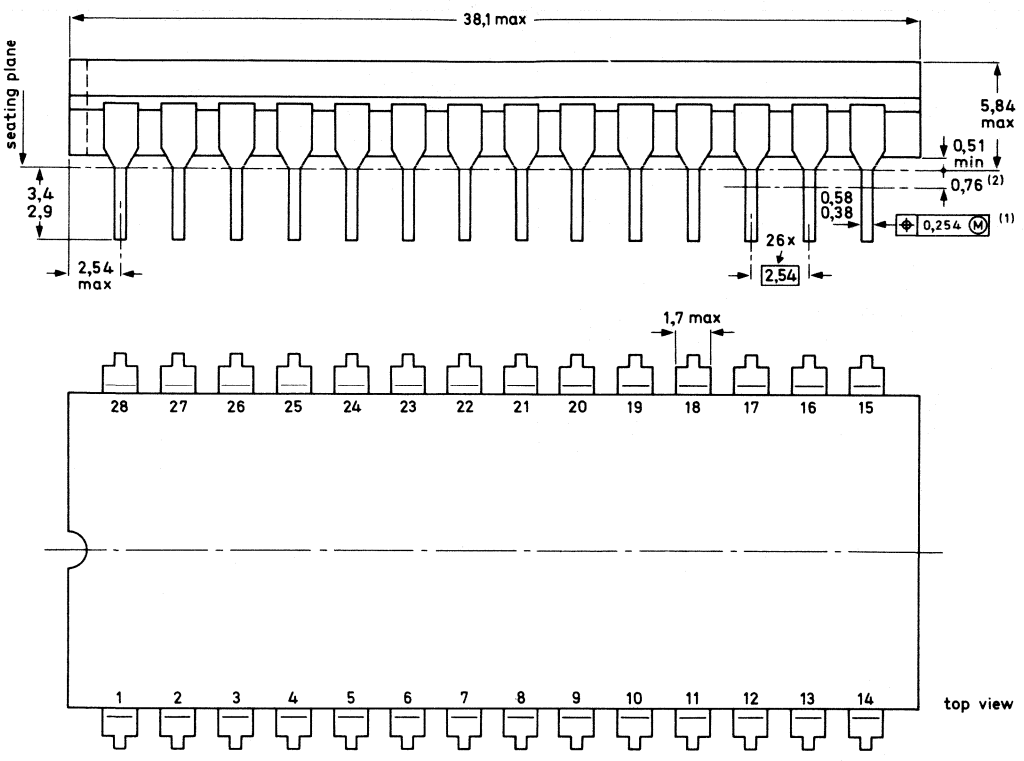
Dimensions in mm

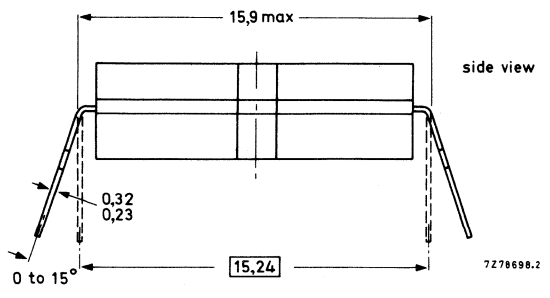
(1) 1 pattern = 4 perforation pitch intervals (contains two modules)
(2) Circuit-test holes
(3) Fixed by the user

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT135A)





⊕ Positional accuracy.

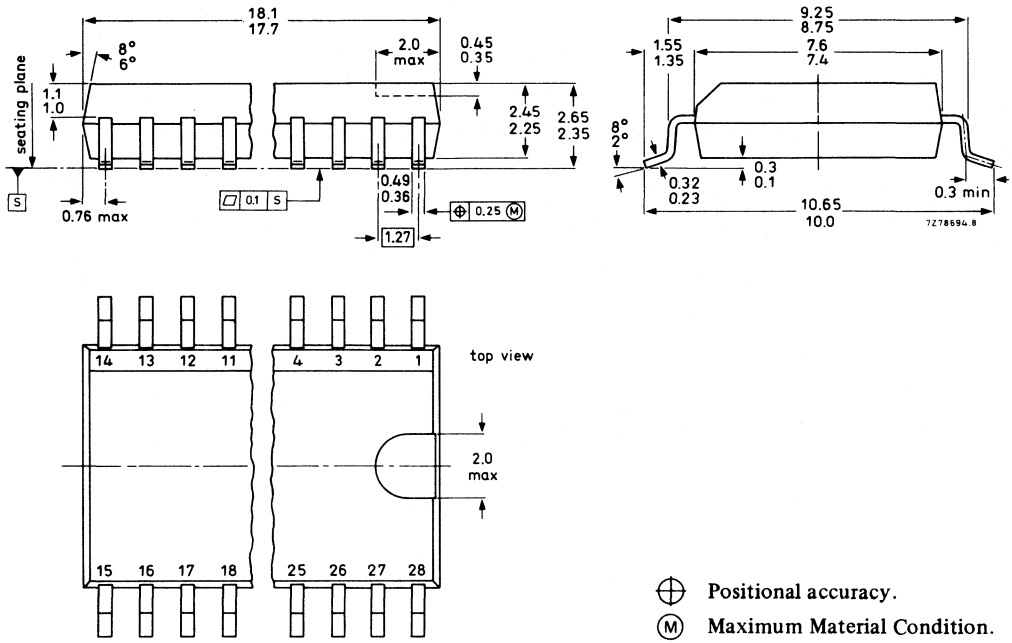
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

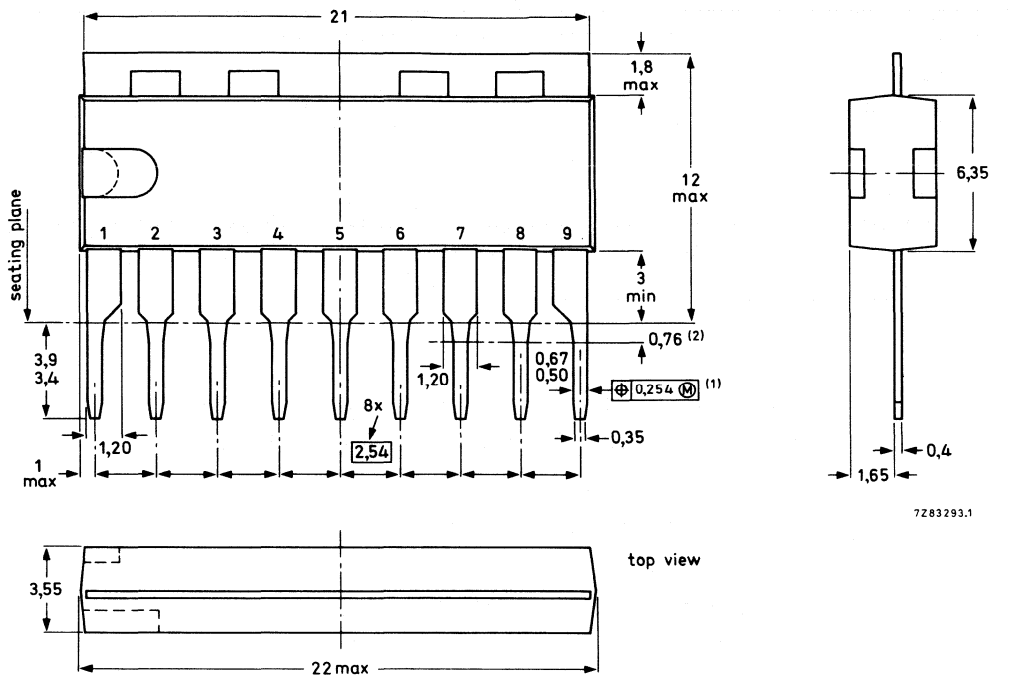
Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)



Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT142)



⊕ Positional accuracy.

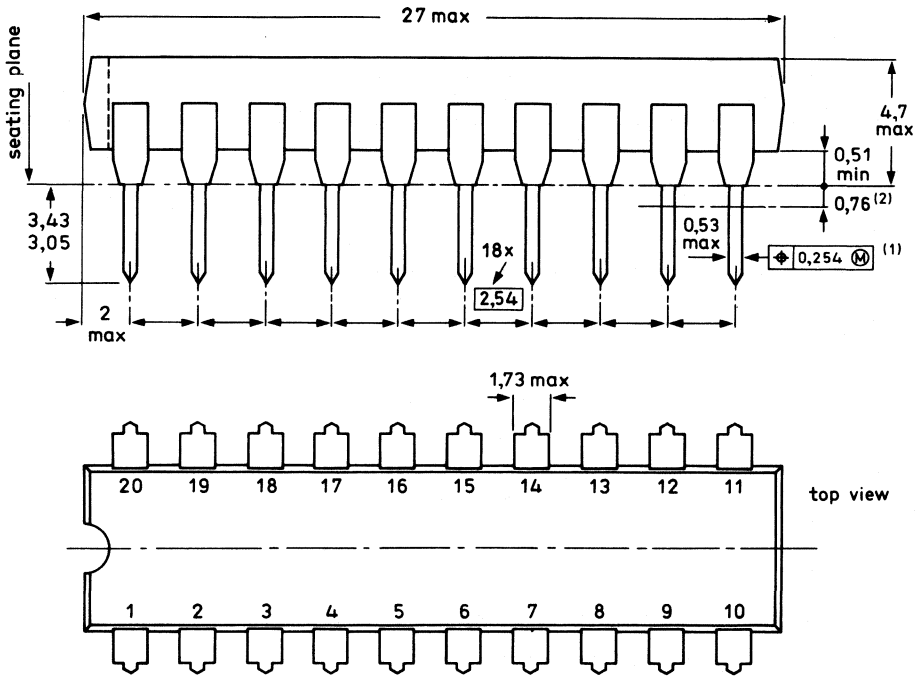
Ⓜ Maximum Material Condition.

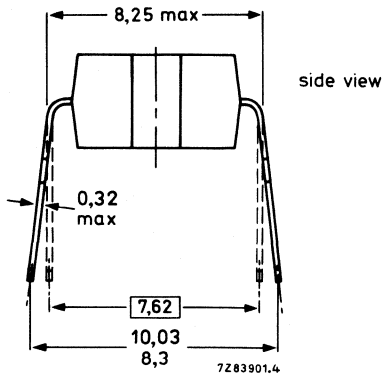
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT146)





⊕ Positional accuracy.

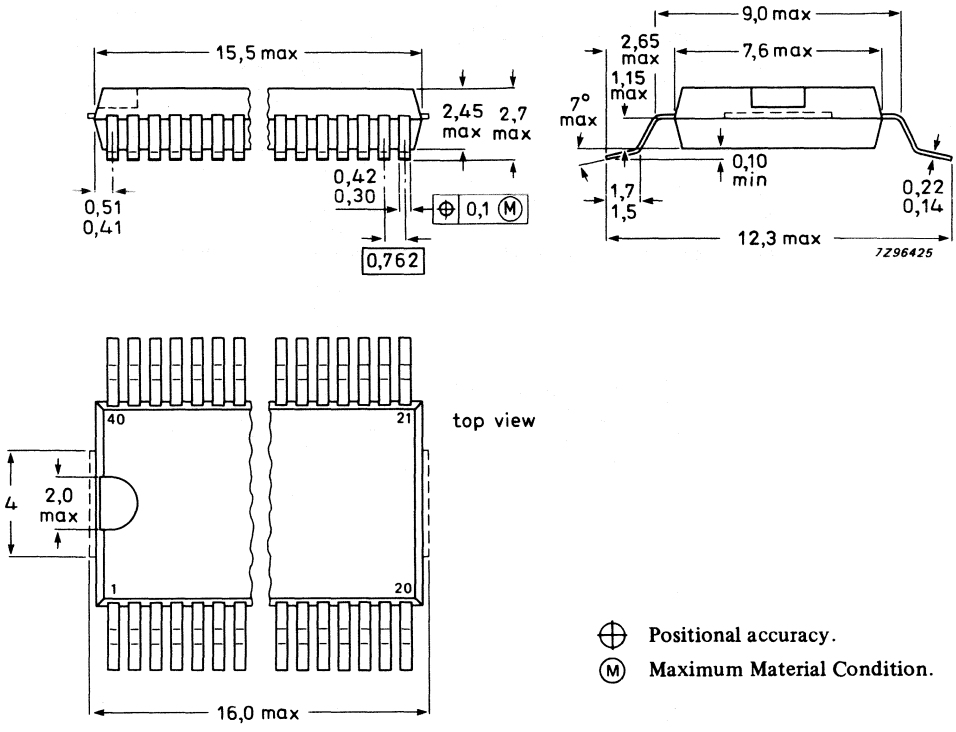
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

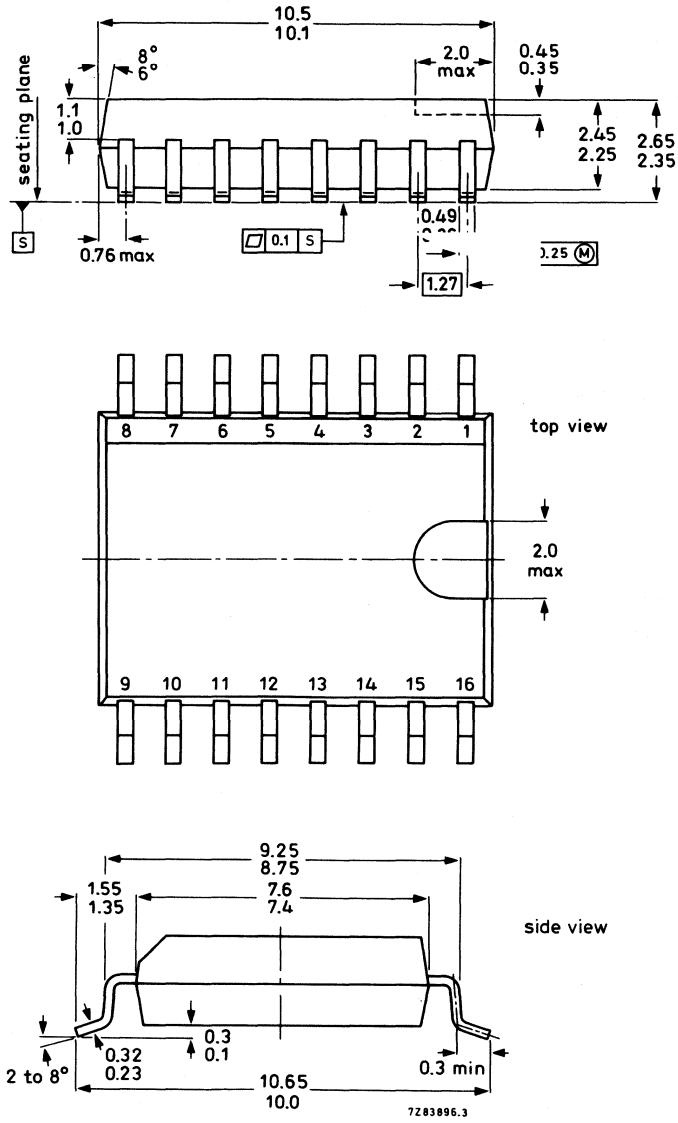
Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (VSO40; SOT158A)



Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

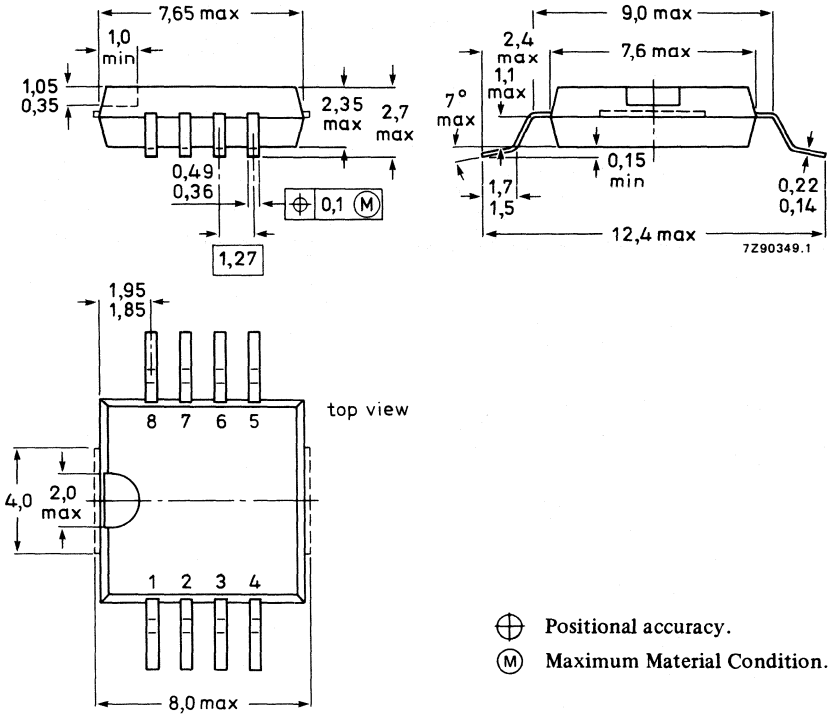


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

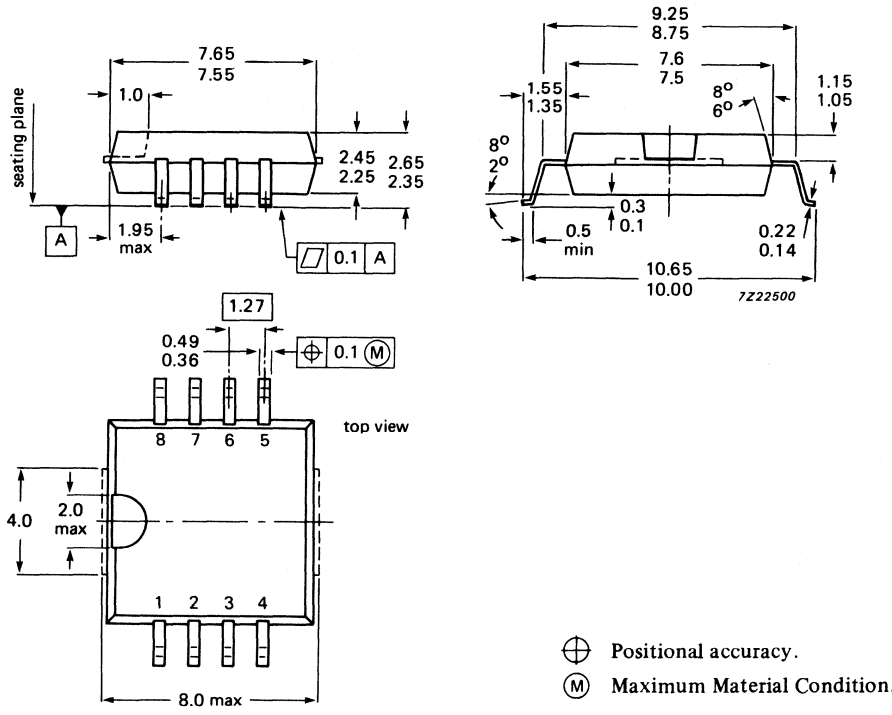
Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176A)



Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176C)

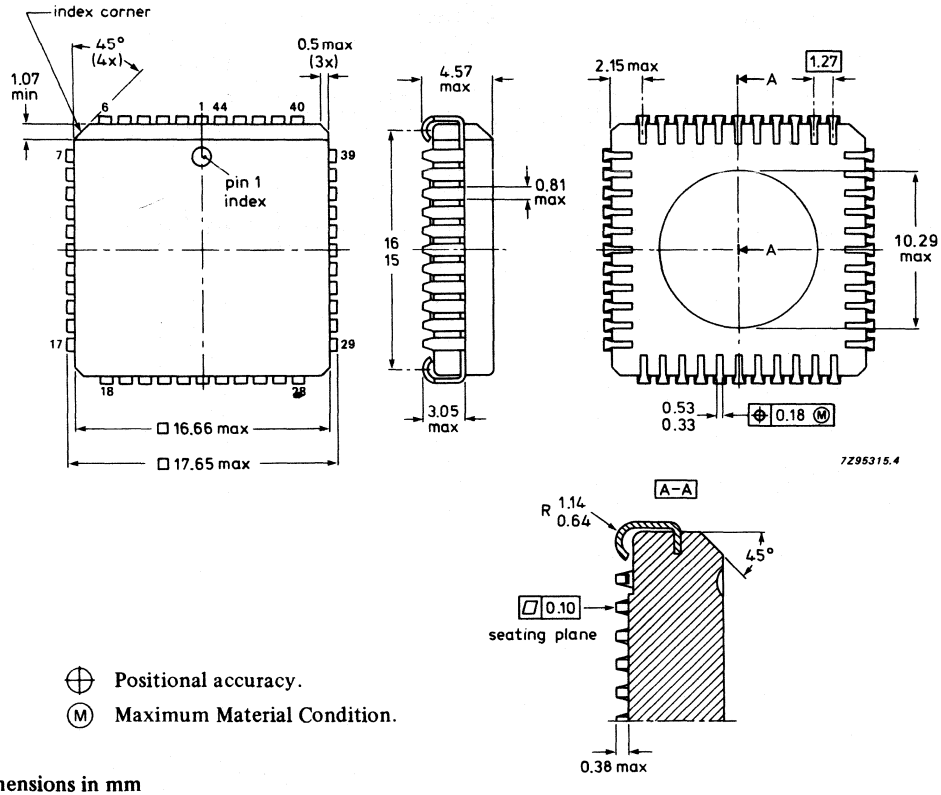


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

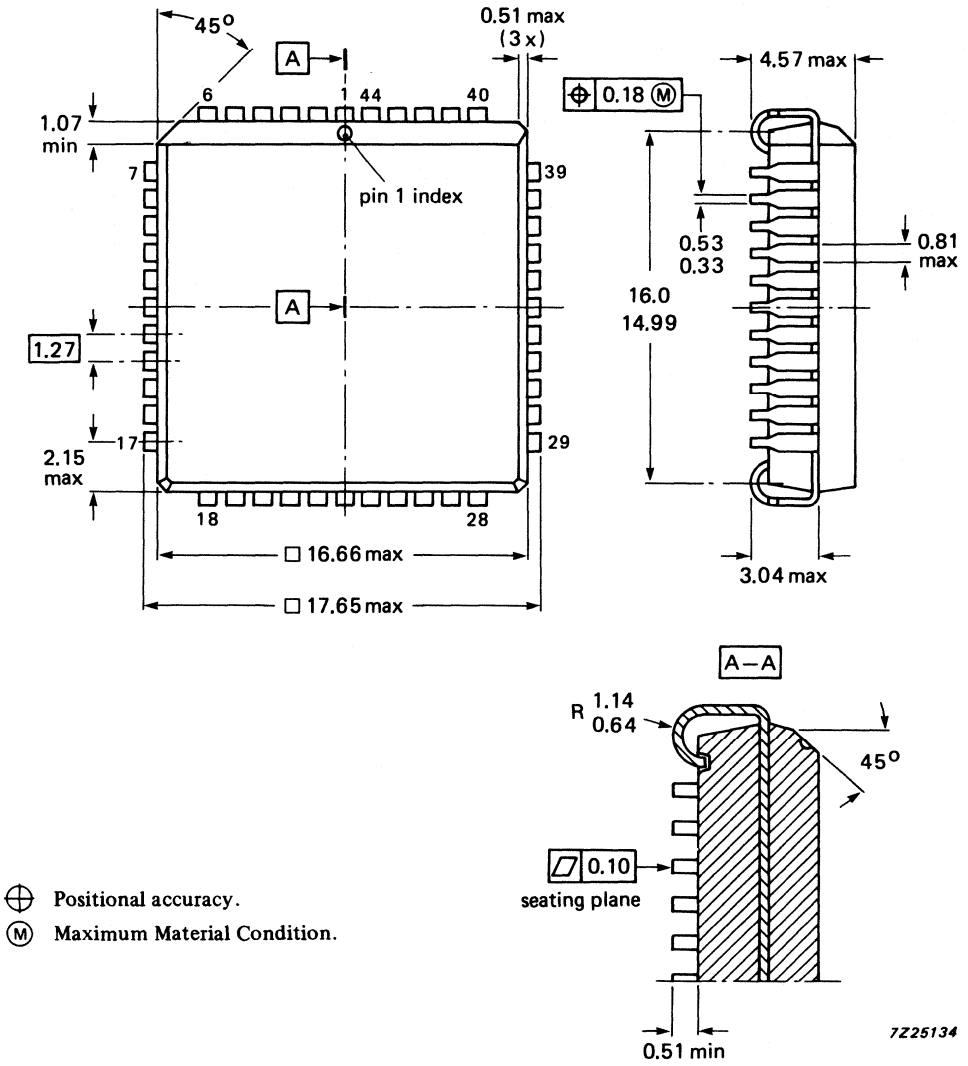
Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'PEDESTAL' VERSION (SOT187)



Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'POCKET' VERSION (SOT187AA)

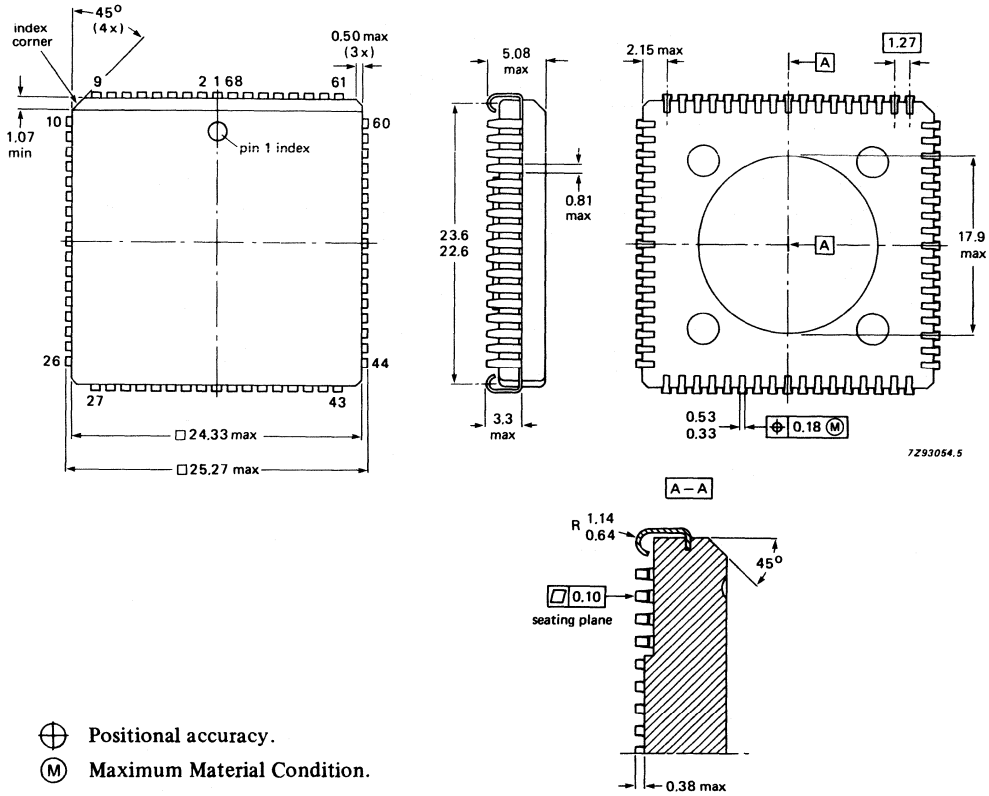


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'PEDESTAL' VERSION (SOT188)

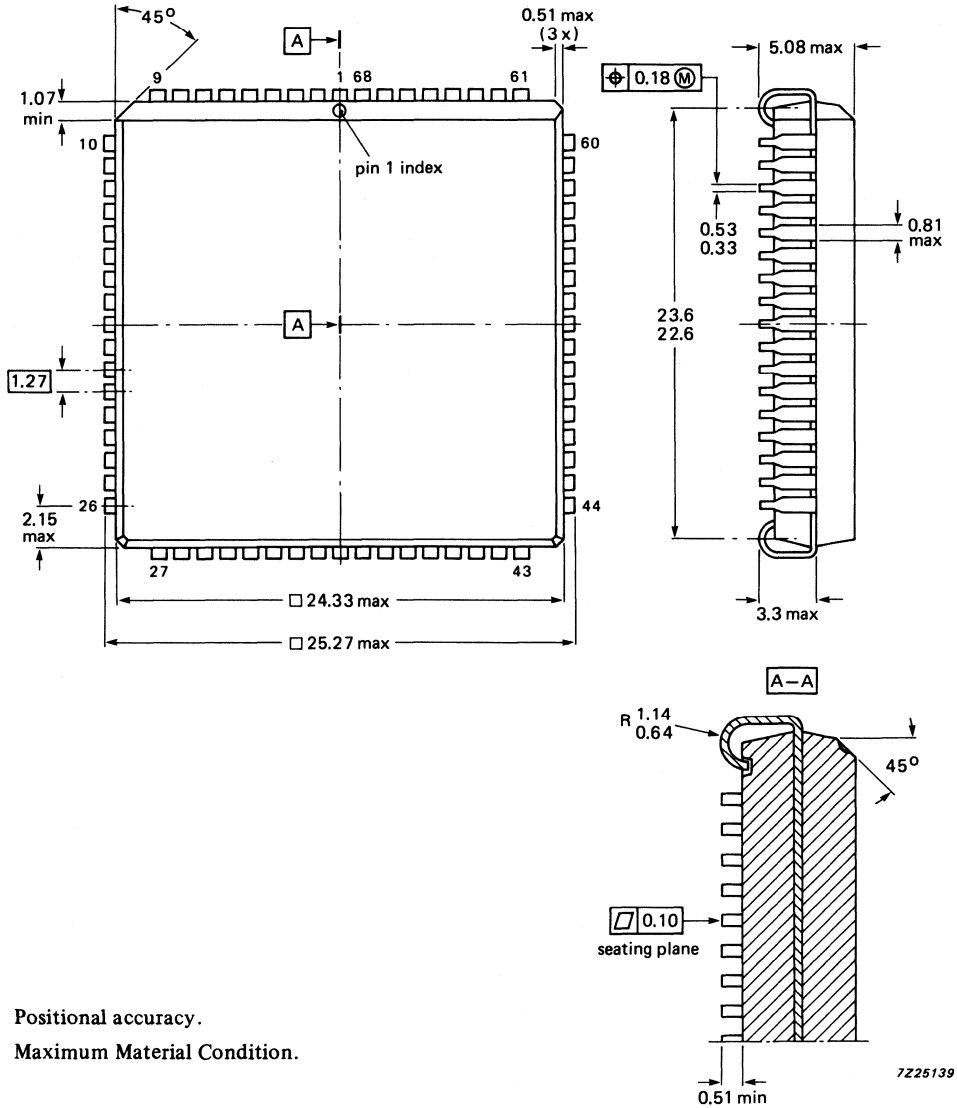


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'POCKET' VERSION (SOT188AA)

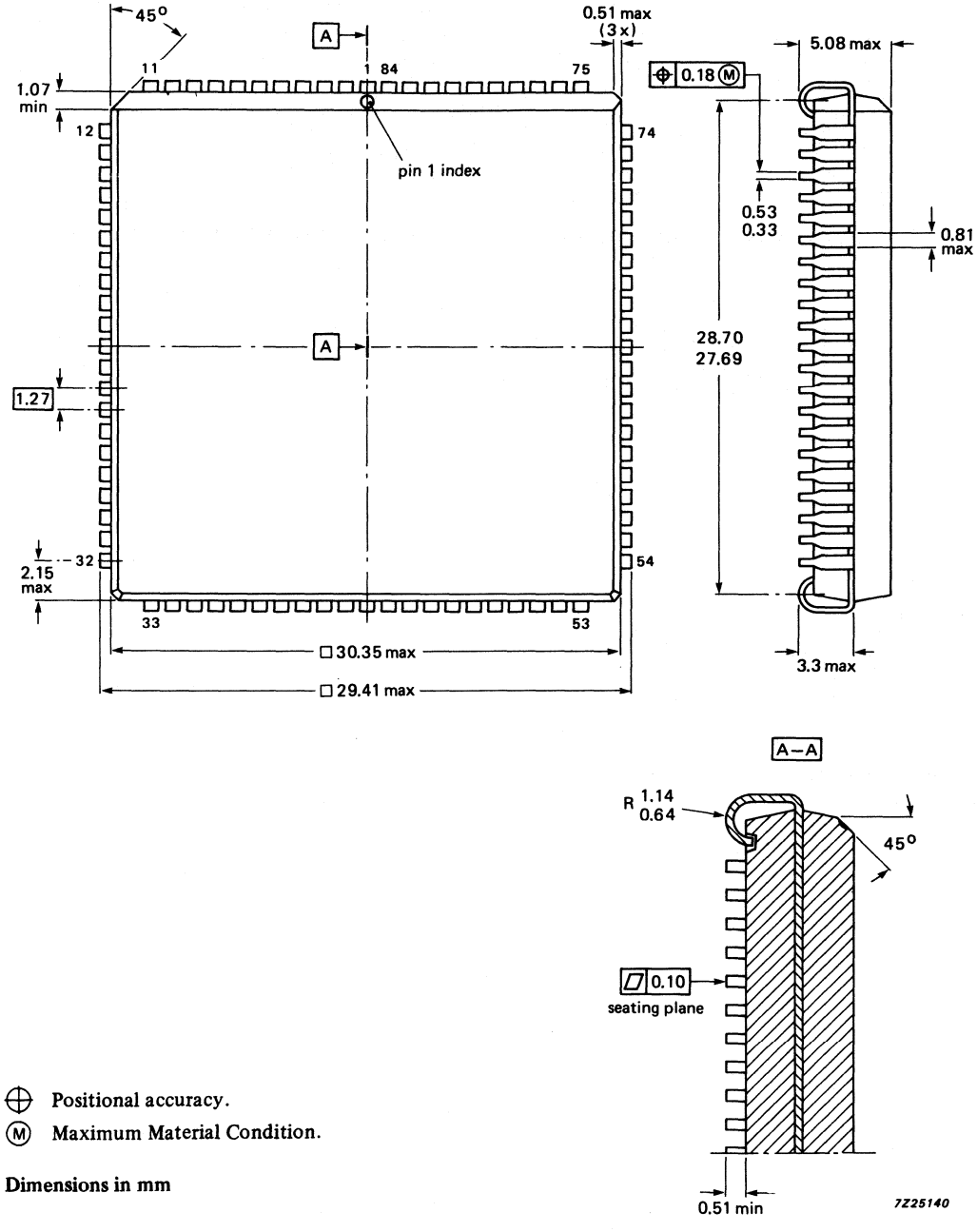


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

84-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'POCKET' VERSION (SOT189AA, AGA)

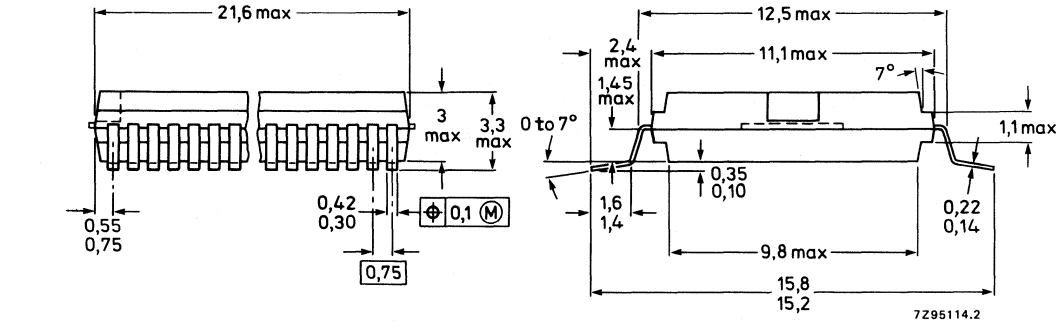


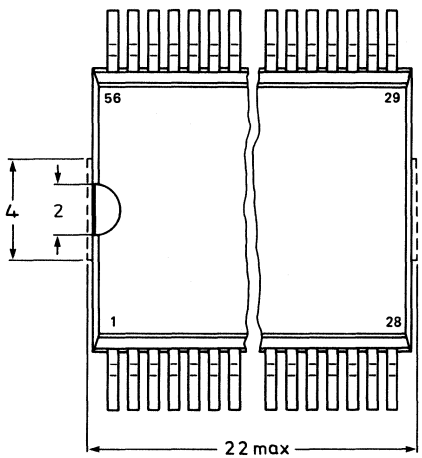
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

56-LEAD MINI-PACK; PLASTIC (VSO56; SOT190)





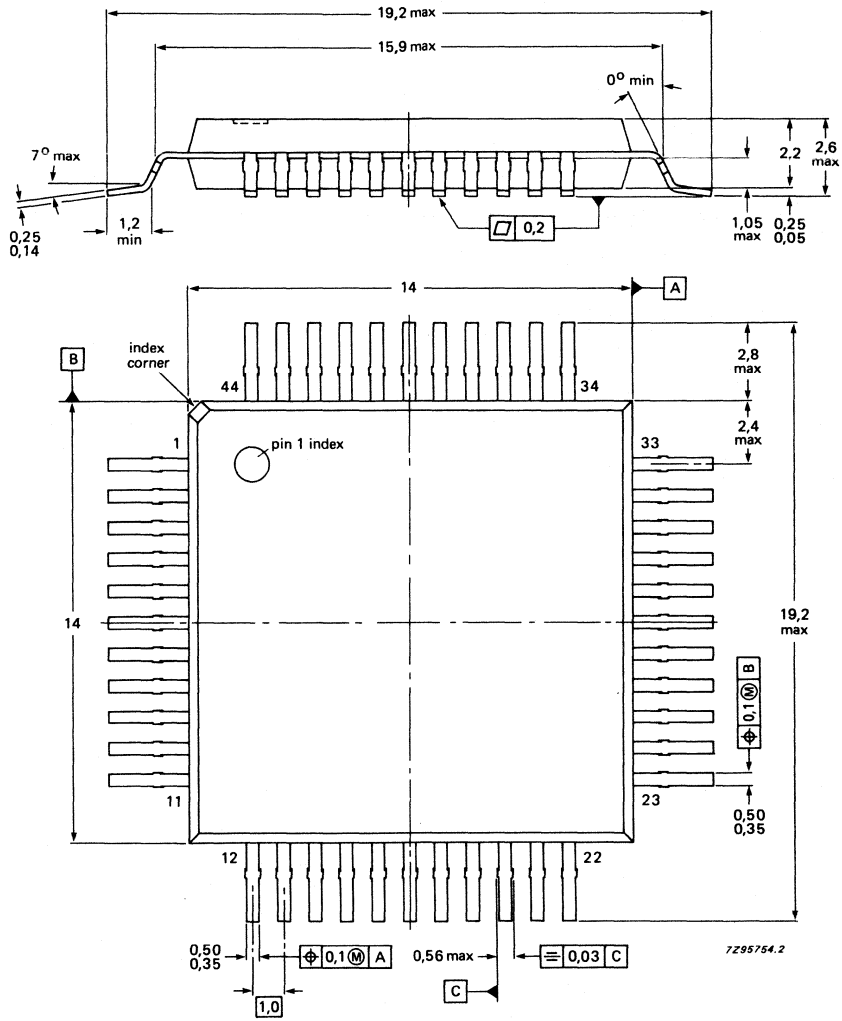
top view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

44-LEAD QUAD FLAT-PACK; PLASTIC (SOT205A)

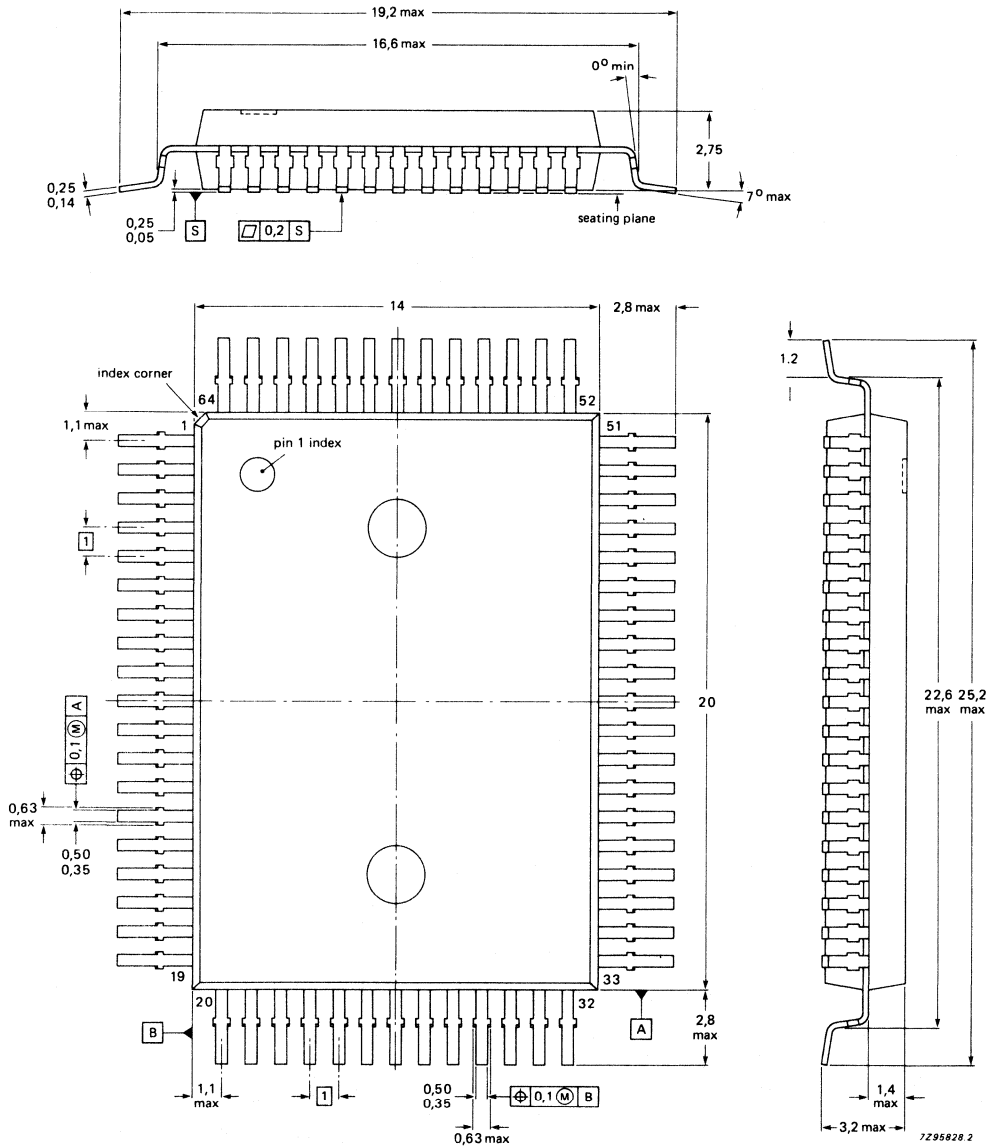


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

64-LEAD QUAD FLAT-PACK; PLASTIC (SOT-208)

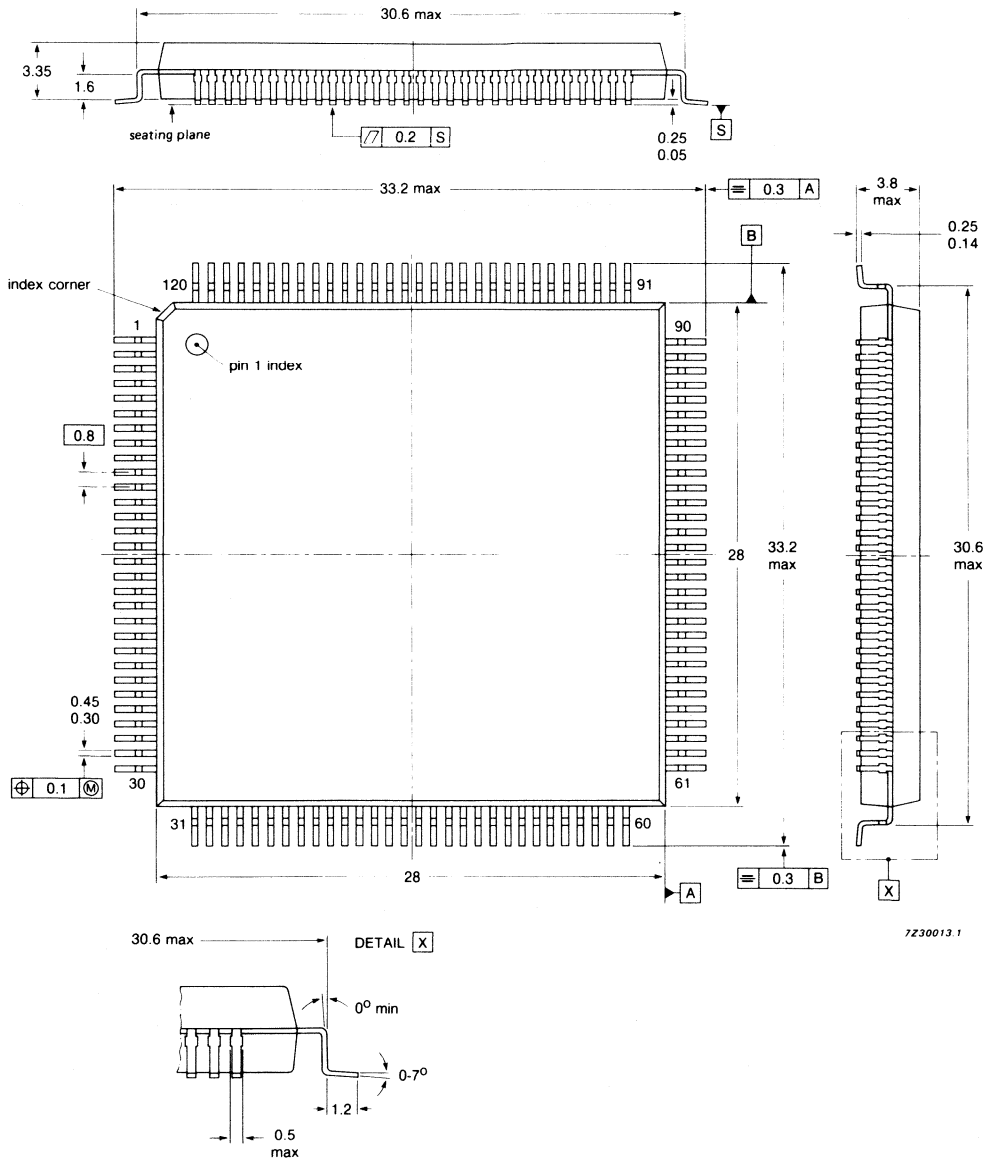


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

120-LEAD QUAD FLAT-PACK; PLASTIC (SOT220)



SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

SOLDERING TAB MODULES

1. Fluxing

(a) a flux that does not have to be removed,
or
(b) a water-soluble flux.

2. Soldering

The reflow soldering method using a pulse-heated soldering tool is usually suitable. Limit the soldering operation to 3 seconds at 250 °C at the leads.

3. Cleaning

Avoid cleaning if possible.

If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do not use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do not use solvents.

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages iii to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

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Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**not yet issued**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
Supplement to IC11	**Linear Products**
IC12	**I²C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** MMOS, CMOS
IC15	**FAST TTL logic series**
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IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

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current code	new code	handbook title
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S2a	**SC02***	**Power diodes**
S2b	**SC03***	**Thyristors and triacs**
S3	**SC04***	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07***	**Small-signal field-effect transistors**
S6	**SC08***	**RF power transistors**
	SC09	**RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8a	**SC11***	**Light emitting diodes**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14***	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**
S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
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T16	**DC02***	**Monochrome tubes and deflection units**
C2	**DC03***	**Television tuners, coaxial aerial input assemblies**
C3	**DC04***	**Loudspeakers**
C20	**DC05***	**Wire-wound components for TVs and monitors**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
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C11	**PA02***	**Varistors, thermistors and sensors**
C12	**PA03***	**Potentiometers, encoders and switches**
C7	**PA04***	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08***	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T1	*	**Power tubes for RF heating and communications**
T2a	*	**Transmitting tubes for communications, glass types**
T2b	*	**Transmitting tubes for communications, ceramic types**
T3	**PC01****	**High-power klystrons**
T4	*	**Magnetrons for microwave heating**
T5	**PC02****	**Cathode-ray tubes**
T6	**PC03****	**Geiger-Müller tubes**
T9	**PC04****	**Photo and electron multipliers**
T10	**PC05****	**Plumbicon camera tubes and accessories**
T11	**PC06****	**Microwave diodes and sub-assemblies**
T12	**PC07**	**Vidicon and Newvicon camera tubes and deflection units**
T13	**PC08**	**Image intensifiers**
T15	**PC09****	**Dry reed switches**
C8	**PC10**	**Variable mains transformers; annular fixed transformers**
	PC11	**Solid state image sensors and peripheral integrated circuits**

* These handbooks will not be reissued.
** Not yet issued with the new code in this series of handbooks.

MATERIALS

This series of data handbooks comprises:

current code	new code	handbook title
C4 C5	MA01*	**Soft Ferrites**
C16	MA02**	**Permanent magnet materials**
C19	MA03**	**Piezoelectric ceramics**

* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

** Not yet issued with the new code in this series of handbooks.

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